

## SIGRETIOS <br> DATA AnALOG - specificntions - APPLICATIONS <br> -military summary



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## Introduction

ค.
s one of the world's largest manufacturers of integrated circuits, Signetics designs, develops, manufactures and sells over 1600 different types of integrated circuits. Signetics produces digital and linear circuits, utilizing both bipolar and metal-oxide-semiconductor (MOS) manufacturing processes.
The Analog division is a major broad line supplier of both Signetics' original designs and industry standard devices. The NE535 High Performance Operational Amplifier, the NE555 Timer and the NE567 Phase Locked Loop are among Signetics' original products. Leading industry standard products available from Signetics include the LM124/224/324 Quad Operational Amplifier, the LM139/239/339 Quad Comparator, the $\mu$ A741 and MC1458 General Purpose Operational Amplifiers. The breadth of the Analog product line offers the designer, the component engineer, and the purchasing agent a varied approach to linear circuits ranging from the $\mu \mathrm{A} 741$ to the latest in high technology products-a microprocessor compatible digital-to-analog converter-the NE5018.
This broad analog circuit product line is backed by Signetics' industry image as a quality manufacturer to whom the servicing of the customer's needs is paramount. In order to continually improve this service capability, Signetics has, and will continue to implement, product development plans to include both original designs and leading industry standards. Examples of new products expected to be available within the next six months, but not included in this edition of the Analog manual are:

| TYPE | DESCRIPTION |
| :--- | :--- |
| NE530 | High Speed Operational Amplifier |
| NE5530 | Dual High Speed Operational Amplifier |
|  | (Dual 530) |
| NE503 | 1536-Bit Bucket Brigade |
| NE5533 | Dual 5534 |
| 79HV00 | High Breakdown 79XX |
| TDA2002 | Audio Amp |
| TDA2573 | TV Vertical Countdown |
| NE5034 | 8-Bit A/D Converter |
| NE588 | LED Display Driver - Source Outputs |
| NE589 | LED Display Driver - Source Outputs |
| NE5010 | 10-Bit D/A Converter |
| MC1399 | TV Color Processing Circuit |
| $\mu$ A79HV00 | Three Terminal Negative High Voltage |
|  | Regulator |

The 1977 Analog Data Manual is one in a series of four data manuals published by Signetics. This publication is intended to serve as a single technical reference for designing with linear circuits by presenting both data specifications and applications information in one manual.

The format of this year's edition differs from that of the 1976 Analog manual. Data specifications and applications material are presented in two sections indexed for ease of use. The Data Specifications portion is completely new data presented in standard data sheet format reflecting commercial and military grade availability. The Applications portion is updated and rewritten to reflect data on new products issued in the last year. In addition, a section on Military provides information on product availability and processing options.

## ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located on the back cover of this manual.

## Minimum Factory Order:

Commercial Product:
$\$ 1000$ per order
$\$ 50$ per line item per order
Military Product:
$\$ 250$ per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix $\left(-55^{\circ} \mathrm{C}\right.$ to $\left.+125^{\circ} \mathrm{C}\right)$ indicates only its operating temperature range and not its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

| PART NUMBER | CROSS REF PART NO. | PRODUCT FAMILY | PRODUCT DESCRIPTION |
| :---: | :---: | :---: | :---: |
| NE535N <br> $\mu \mathrm{A} 741 \mathrm{C}$ | MC1741SC <br> LM741CJ | ANA ANA | High Slew Rate OP-AMP General Purpose OP-AMP |
|  |  |  |  |

Table 1 PART NUMBER DESCRIPTION

| SUFFIX |  | PACKAGE DESCRIPTION2 |
| :---: | :---: | :---: |
| Old | New |  |
| A,AA | $N$ | 14-lead plastic DIL |
| A | $\mathrm{N}-14$ | 14-lead plastic DIL (Selected Analog products only) |
| B,BA | N | 16-lead plastic DIL |
| DA | DA | 2-lead TO-3 |
| DB | DB | 3-lead TO-5 |
| DC | DC | 4-lead TO-46 |
| DE | DE | 4-lead TO-72 |
| F | F | 14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL |
| I, IK | 1 | 14, 16, 18, 22, 28 and 4-lead ceramic DIL |
| K | K | 10-lead TO-100 |
| L | L | 10-lead high-profile TO-100 can |
| NA,NX | N | 24-lead plastic DIL |
| PN | PHA | $12+1$ GND pin DIL |
| Q,R | Q | 10, 14, 16 and 24-lead ceramic flat |
| S | S | 3-lead TO-92 plastic |
| SK | SK | Microprocessor kit |
| T,TA | T | 8 -lead TO-99 |
| U | U | Plastic power TO-220 |
| v | N | 8 -lead plastic DIL |
| W,WJ | W | 10, 14, 16 and 24-lead ceramic (Cerpac) flat |
| XA | N | 18-lead plastic DIL |
| XC | N | 20-lead plastic DIL |
| XC | N | 22-lead plastic DIL |
| XL, XF | N | 28-lead plastic DIL |


| PREFIX | DEVICE TEMPERATURE RANGE |
| :--- | :---: |
| N- | $0^{\circ}$ to $+70^{\circ} \mathrm{C}$ |
| S- | $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| NE- | $0^{\circ}$ to $+70^{\circ} \mathrm{C}$ |
| SE- | $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| SA | $-44^{\circ}$ to $+85^{\circ} \mathrm{C}$ |
| SU | $-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |

Table 3 DEVICE TEMPERATURE

| PREFIX | DEVICE FAMILY |
| :--- | :--- |
| CA | Linear Industry Standard |
| DM | Linear Industry Standard |
| JB | Mil ReI-Jan Qualified- |
|  | Old Designator |
| JM | Mil Rel-Jan Qualified- |
|  | New Designator |
| LH | Linear Industry Standard |
| LM | Linear Industry Standard |
| M | Mil ReI-Jan Processed |
| MC | Linear Industry Standard |
| PA | Linear Industry Standard |
| SD | Linear DMOS |
| SP | DTL Series |
| UA | Linear Industry Standard |
| ULN | Linear Industry Standard |

Table 4 FAMILY PREFIX

Table 2 PACKAGE DESCRIPTIONS

## SPECIAL PROCESSING

Signetics offers two major processing levels: Mil-Spec and Supr II. Following are brief descriptions of these processes. For further information in either product availability or process data, contact your local Signetics sales office.

## SUPR II

Signetics Upgraded Product Reliability (SUPR) program is designed to provide industrial manufacturers with integrated circuits of a higher level of quality and reliability than is available with standard commercial product. Improvements in quality and reliability will result in significant cost savings to the integrated circuit user. Signetics has maintained a quality and reliability leadership position via its SUPR-

DIP program (1972) and SUPR II program (1975). SUPR II is a two-level program. Level A boosts the AQL functional guarantee on all Signetics product families. Level B; for maximum reliability, includes an additional $100 \%$ burn-in to Mil std 883. Condition F.

## LEVEL A HIGHLIGHTS

- Thermal shock preconditioning (per Mil std 883)
- $100 \%$ dc testing
- $100 \%$ functional testing at $100^{\circ}$
- SEM wafer quality monitor
- Die and preseal visual inspection criteria (per Mil std 883)
The Analog division is continually expanding the availability list of products processed to SUPR II Levels A and B. For information concerning the SUPR II status
of products not shown in Table 5, contact your local Signetics sales office.

| DM8820 | LM319 | $\mu$ A723C |
| :--- | :--- | :--- |
| DM8830 | LM324 | $\mu$ A741C |
| DM8880 | LM339 | $\mu$ A747C |
| DM8880-1 | MC1458 | $\mu$ A748C |
| LM124 | MC3302 | $\mu$ A7805C |
| LM201H | $\mu$ A709C | $\mu$ A7812C |
| LM301A | $\mu$ A710C | 75450B |
| LM307 | $\mu$ A711C | 75451B |
| LM308 | NE555 | 75452B |
| LM309 | NE556 | 75453B |
| LM3111 | 75454B |  |
| MC1496 |  |  |

Table 5 PRODUCT PRESENTLY AVAILABLE TO LEVELS A AND B


## DATA SpECIfICATIONS

# OPERATIONAL AmpIIfIERS 

## DESCRIPTION

LF155, LF155A, LF255, LF355, LF355A (Low Supply Current)
LF156, LF156A, LF256, LF356, LF356A (Wide Band)
LF157, LF157A, LF257, LF357, LF357A (Wide Band)
The LF155, LF156, LF157 Series of operational amplifiers employ well matched, high voltage JFET input structures on the same monolithic chip as bipolar devices. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low noise.

## COMMON FEATURES

(LF155A/156A/157A)

- Low input bias current 30pA
- Low input offset current 3pA
- High input impedance $1012 \Omega$
- Low input offset voltage 1 mV
- Low $V_{\text {os }}$ temperature drift $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- Low input noise current $0.01 \mathrm{pA} / \sqrt{\mathrm{Hz}}$


## SPECIFIC FEATURES

- Settling time (0.01\%) $\quad 4 \mu \mathrm{~s} \quad 1.5 \mu \mathrm{~s}$
- High slew rate
- Wide bandwidth $5 \mathrm{v} / \mu \mathrm{s} \quad 12 \mathrm{v} / \mu \mathrm{s}$ $2.5 \mathrm{MHz} \quad 5 \mathrm{MHz}$
- Low input noise 20nV/ / Hz 12nV/ $\sqrt{\mathrm{Hz}}$
- LF155, LF156-military qualifications pending
LF157A
$\left(A_{V}=5\right)$

$1.5 \mu \mathrm{~s}$
$50 \mathrm{v} / \mu \mathrm{s}$
20 MHz
$12 \mathrm{nV} / \sqrt{\mathrm{Hz}}$

Settling time (0.01\%)

- High slew rate
- Wide bandwidth
- Low input noise
$12 n V / \sqrt{\mathrm{Hz}}$


## APPLICATIONS

- Precision high speed integrators
- Fast A/D, D/A converters
- High impedance buffers
- Wideband, low noise, low drift amplifier

PIN CONFIGURATION


## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Supply voltage |  |  |
| LF155A/6A/7A, LF155/6/7 | $\pm 22$ | V |
| LF255/6/7 | $\pm 22$ | V |
| LF355A/6A/7A, LF355/6/7 | $\pm 18$ | V |
| Power dissipation 1 TO-99 (T-package) |  |  |
| LF155A/6A/7A, LF155/6/7 | 670 | mW |
| LF255/6/7 | 570 | mW |
| LF355A/6A/7A, LF355/6/7 | 500 | mW |
| Operating temperature range |  |  |
| LF155A/6A/7A, LF155/6/7 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| LF255/6/7 | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| LF355A/6A/7A, LF355/6/7 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| TJ (Max) |  |  |
| LF155A/6A/7A, LF155/6/7 | 150 | ${ }^{\circ} \mathrm{C}$ |
| LF255/6/7 | 115 | ${ }^{\circ} \mathrm{C}$ |
| LF355A/6A/7A, LF355/6/7 | 100 | ${ }^{\circ} \mathrm{C}$ |
| Input voltage range 2 |  |  |
| LF155A/6A/7A, LF155/6/7 | $\pm 20$ | V |
| LF255/6/7 | $\pm 20$ | V |
| LF355A/6A/7A, LF355/6/7 | $\pm 20$ | V |
| Output short circuit duration |  |  |
| LF155A/6A/7A, LF155/6/7 | Continuous |  |
| LF255/6/7 | Continuous |  |
| LF355A/6A/7A, LF355/6/7 | Continuous |  |
| Storage temperature range |  |  |
| LF155A/6A/7A, LF155/6/7 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| LF255/6/7 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| LF355A/6A/7A, LF355/6/7 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering, 10sec.) | 300 | ${ }^{\circ} \mathrm{C}$ |
| LF155A/6A/7A, LF155/6/7 | 300 | ${ }^{\circ} \mathrm{C}$ |
| LF255/6/7 | 300 | ${ }^{\circ} \mathrm{C}$ |
| LF355A/6A/7A, LF355/6/7 | 300 | ${ }^{\circ} \mathrm{C}$ |

## NOTES

1. The TO-99 package must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$ junction to ambient or $25^{\circ} \mathrm{C} / \mathrm{W}$ junction to case
2. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. (See notes on following page.)

| PARAMETER |  | TEST CONDITIONS | LF155A/6A/7A |  |  | LF355A/6A/7A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage |  | $\mathrm{R}_{\mathrm{S}}=50 \Omega$ |  | 1 | $\begin{gathered} 2 \\ 2.5 \end{gathered}$ |  | 1 | $\begin{gathered} 2 \\ 2.3 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| $\Delta \mathrm{V}_{\mathrm{os}} / \Delta \mathrm{T}$ <br> $\Delta T C / \Delta V_{\text {os }}$ | Avg. TC of input offset voltage <br> Change in average TC2 with $V_{\text {os }}$ adjust | $\begin{aligned} & R_{s}=50 \Omega \\ & R_{s}=50 \Omega \end{aligned}$ |  | $\begin{gathered} 3 \\ 0.5 \end{gathered}$ | 5 |  | $\begin{gathered} \hline 3 \\ 0.5 \end{gathered}$ | 5 | $\begin{aligned} & \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ & { }^{\mu} /{ }^{\circ} \mathrm{C} \\ & \text { per } \mathrm{mV} \end{aligned}$ |
| los | Input offset current 1,3 | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}} \leq \mathrm{T}_{\text {high }} \\ & \hline \end{aligned}$ |  | 3 | $\begin{aligned} & 10 \\ & 10 \\ & \hline \end{aligned}$ |  | 3 | $\begin{gathered} 10 \\ 1 \end{gathered}$ | $\begin{aligned} & \hline \mathrm{pA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| IB | Input bias current 1,3 | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}} \leq \mathrm{T}_{\text {high }} \\ & \hline \end{aligned}$ |  | 30 | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ |  | 30 | $\begin{gathered} 50 \\ 5 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{pA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| RIN | Input resistance | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 1012 |  |  | 1012 |  | $\Omega$ |
| Avol | Large signal voltage gain | $\begin{gathered} V_{\mathrm{s}}= \pm 15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{O}}=\frac{ \pm 10 \mathrm{~V}, R_{\mathrm{L}}=2 \mathrm{k} \Omega}{} \begin{array}{l} \text { Over temp. } \end{array} . \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| Vo | Output voltage swing | $\begin{gathered} V_{\mathrm{S}}= \pm 15 \mathrm{~V}, R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, R_{\mathrm{L}}=2 \mathrm{k} \Omega \\ \hline \end{gathered}$ | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 12 \end{aligned}$ |  | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 12 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| $\mathrm{V}_{\text {cm }}$ | Input common mode Voltage range | $\mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V}$ | $\pm 11$ | $\begin{array}{\|c} \hline+15.1 \\ -12 \\ \hline \end{array}$ |  | $\pm 11$ | $\begin{aligned} & +15.1 \\ & -12 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| CMRR PSRR | Common-mode rejection ratio Supply volt. rej. ratio4 |  | $\begin{aligned} & 85 \\ & 85 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & 85 \\ & 85 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. (See notes on following page.)

| PARAMETER |  | TEST CONDITIONS | LF155/6/7 |  |  | LF255/6/7 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage |  | $\mathrm{R}_{\mathrm{S}}=50 \Omega$ |  | 3 | $\begin{aligned} & 5 \\ & 7 \end{aligned}$ |  | 3 | $\begin{gathered} 5 \\ 6.5 \end{gathered}$ | $\begin{aligned} & m V \\ & m V \end{aligned}$ |
| $\begin{aligned} & \Delta \mathrm{V}_{\mathrm{OS}} / \Delta \mathrm{T} \\ & \Delta \mathrm{TC} / \Delta \mathrm{V}_{\mathrm{OS}} \end{aligned}$ | Avg. TC of input offset voltage <br> Change in average TC2 with $\mathrm{V}_{\text {os }}$ adjust | $\begin{aligned} & R_{\mathrm{s}}=50 \Omega \\ & \mathrm{R}_{\mathrm{s}}=50 \Omega \end{aligned}$ |  | $\begin{gathered} 5 \\ 0.5 \end{gathered}$ |  |  | $\begin{gathered} 5 \\ 0.5 \end{gathered}$ |  | $\begin{gathered} \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \text { per } \mathrm{mV} \end{gathered}$ |
| los | Input offset current1,3 | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J} \leq \mathrm{T}_{\text {high }} \\ & \hline \end{aligned}$ |  | 3 | $\begin{aligned} & 20 \\ & 20 \\ & \hline \end{aligned}$ |  | 3 | $\begin{gathered} 20 \\ 1 \end{gathered}$ | $\begin{aligned} & \mathrm{pA} \\ & \mathrm{nA} \end{aligned}$ |
| IB | Input bias current ${ }^{1,3}$ | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J} \leq \mathrm{T}_{\text {high }} \\ & \hline \end{aligned}$ |  | 30 | $\begin{array}{\|c\|} \hline 100 \\ 50 \\ \hline \end{array}$ |  | 30 | $\begin{gathered} 100 \\ 5 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{pA} \\ & \mathrm{nA} \end{aligned}$ |
| Rin | Input resistance | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 1012 |  |  | 1012 |  | $\Omega$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\ \text { Over temp. } \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| V | Output voltage swing | $\begin{aligned} & V_{\mathrm{s}}= \pm 15 \mathrm{~V}, R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, R_{\mathrm{L}}=2 \mathrm{k} \Omega \\ & \hline \end{aligned}$ | $\begin{aligned} & \pm 12 \\ & \pm 10 \\ & \hline \end{aligned}$ | $\begin{array}{\|l}  \pm 13 \\ \pm 12 \\ \hline \end{array}$ |  | $\begin{array}{r}  \pm 12 \\ \pm 10 \\ \hline \end{array}$ | $\begin{array}{r}  \pm 13 \\ \pm 12 \\ \hline \end{array}$ |  | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| VCM | Input common mode Voltage range | $\mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V}$ | $\pm 11$ | $\begin{array}{r} \hline+15.1 \\ -12 \\ \hline \end{array}$ |  | $\pm 11$ | $\begin{array}{r} \hline+15.1 \\ -12 \\ \hline \end{array}$ |  | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| CMRR PSRR | Common-mode rejection ratio Supply volt. rej. ratio4 |  | $\begin{aligned} & 85 \\ & 85 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & 85 \\ & 85 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LF355/6/7 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| V os | Input offset voltage |  | $\mathrm{R}_{\mathrm{s}}=50 \Omega$ |  | 3 | $\begin{aligned} & 10 \\ & 13 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| $\begin{aligned} & \Delta V_{\mathrm{os}} / \Delta \mathrm{T} \\ & \Delta \mathrm{TC} / \Delta \mathrm{V}_{\mathrm{os}} \end{aligned}$ | Avg. TC of input offset voltage Change in average TC2 with Vos adjust | $\begin{aligned} & \mathrm{R}_{\mathrm{s}}=50 \Omega \\ & \mathrm{R}_{\mathrm{s}}=50 \Omega \end{aligned}$ |  | 5 <br> 0.5 |  | $\begin{gathered} \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \text { per } \mathrm{mV} \\ \hline \end{gathered}$ |
| los | Input offset current ${ }^{1,3}$ | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J} \leq \mathrm{T}_{\text {high }} \end{aligned}$ |  | 3 | $\begin{gathered} 50 \\ 2 \end{gathered}$ | $\begin{aligned} & \mathrm{pA} \\ & \mathrm{nA} \end{aligned}$ |
| IB | Input bias current ${ }^{1,3}$ | $\begin{aligned} & T_{J}=25^{\circ} \mathrm{C} \\ & T_{J} \leq T_{\text {high }} \\ & \hline \end{aligned}$ |  | 30 | $\begin{gathered} 200 \\ 8 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{pA} \\ & \mathrm{nA} \end{aligned}$ |
| RIN Avol | Input resistance Large signal voltage gain | $\begin{gathered} T_{J}=25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \end{gathered}$ <br> Over temp. | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | $\begin{aligned} & 1012 \\ & 200 \end{aligned}$ |  | $\begin{gathered} \Omega \\ \mathrm{V} / \mathrm{mV} \\ \mathrm{~V} / \mathrm{mV} \end{gathered}$ |
| Vo | Output voltage swing | $\begin{gathered} \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ \mathrm{~V}_{\mathrm{s}}= \pm 15 \mathrm{~V}, R_{\mathrm{L}}=2 \mathrm{k} \Omega \end{gathered}$ | $\begin{array}{r}  \pm 12 \\ \pm 10 \\ \hline \end{array}$ | $\begin{array}{r}  \pm 13 \\ \pm 12 \\ \hline \end{array}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| VCM | Input common mode Voltage range | $V_{s}= \pm 15 \mathrm{~V}$ | $\pm 10$ | $\begin{array}{r} +15.1 \\ -12 \\ \hline \end{array}$ |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| CMRR PSRR | Common-mode rejection ratio Supply volt. rej. ratio ${ }^{4}$ |  | $\begin{aligned} & 80 \\ & 80 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | $\begin{gathered} \text { LF155A/355A } \\ \text { LF155/255 } \\ \hline \end{gathered}$ |  |  | LF355 |  |  | LF156A/LF156/256 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Supply current |  | 2 | 4 |  | 2 | 4 |  | 5 | 7 | mA |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | LF356A/LF356 |  |  | LF157A/LF157/257 |  |  | LF357A/LF357 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Supply current |  | 5 | 10 |  | 5 | 7 |  | 5 | 10 | mA |

NOTES

1. These specifications apply for $\pm 15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V},-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \pm 125^{\circ} \mathrm{C}$ and $\mathrm{T}_{\mathrm{HIGH}}=$ $+125^{\circ} \mathrm{C}$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V},-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ and $\mathrm{THIGH}=85^{\circ} \mathrm{C}$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{s}} \leq \pm 20 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}$ and $\mathrm{T}_{\mathrm{HIGH}}=+70^{\circ} \mathrm{C}$, and for the LF355/6/7 these specifications apply for $V_{S}= \pm 15 \mathrm{~V}$ and $0^{\circ} \mathrm{C} \leq T_{A} \leq+70^{\circ} \mathrm{C}$. $\mathrm{V}_{\mathrm{OS}}, \mathrm{I}_{\mathrm{B}}$ and los are measured at $\mathrm{V}_{\mathrm{CM}}=0$.
2. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount $\left(0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents are junction leakage currents which approximately double for every $10^{\circ} \mathrm{C}$ increase in the junction temperature, $\mathrm{T}_{\mathrm{J}}$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_{j}=T_{A}+\theta_{j A} P d$ where $\theta_{j A}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
4. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified. 1


AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V}$ unless otherwise specified. 1


## AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V}$ unless otherwise specified. 1

| PARAMETER |  | TEST CONDITIONS | LF157/257 |  |  | LF357 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| SR | Slew rate |  | LF157A/LF157: $\mathrm{AV}^{\text {a }}=5$ | 30 | 50 |  |  | 50 |  | $\mathrm{V} / \mu \mathrm{s}$ |
| GBW <br> $t_{s}$ | Gain bandwidth product Settling time ${ }^{5}$ to $0.01 \%$ |  |  | $20$ $1.5$ | . |  | $20$ $1.5$ |  | $\mathrm{MHz}$ $\mu \mathrm{S}$ |
| $e_{n}$ <br> $i_{n}$ <br> Cin | Equiv. input noise volt. <br> Equiv. input noise current <br> Input capacitance | $\begin{gathered} R_{\mathrm{s}}=100 \Omega \\ \mathrm{f}=100 \mathrm{~Hz} \\ \mathrm{f}=1000 \mathrm{~Hz} \\ \mathrm{f}=100 \mathrm{~Hz} \\ \mathrm{f}=1000 \mathrm{~Hz} \end{gathered}$ |  | $\begin{gathered} 15 \\ 12 \\ \\ 0.01 \\ 0.01 \\ 3 \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 15 \\ 12 \\ \\ 0.01 \\ 0.01 \\ 3 \end{gathered}$ |  | $\left\|\begin{array}{c} n V / \sqrt{H z} \\ n V / \sqrt{H z} \\ \\ p A / \sqrt{H z} \\ p A / \sqrt{H z} \\ p F \end{array}\right\|$ |

NOTE
5. Settling time is defined here, for a unity gain inverter connection using $2 \mathrm{k} \Omega$ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within $0.01 \%$ of its final value from the time a 10 V step input is applied to the inverter. For the LF157, $\mathrm{Av}=-5$, the feedback resistor from output to input is $2 k \Omega$ and the output step is 10 V (See Settling Time Test Circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS (curves are for LF155, LF156 and LF157 unless otherwise specified.)


TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL AC PERFORMANCE CHARACTERISTICS


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)


SETTLING TIME TEST CIRCUIT


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A v=-5$
- FET used to isolate the probe capacitance
- Output $=10 \mathrm{~V}$ step
- $A v=-5$ for LF157

LARGE SIGNAL INVERTER OUTPUT, V OUT (FROM SETTLING TIME CIRCUIT)

LF155

$2 \mu \mathrm{~s} / \mathrm{DIV}$

LF156


1 $\mu \mathrm{s} / \mathrm{DIV}$

LF157


1 $\mu \mathrm{s} / \mathrm{DIV}$

## APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.
Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative commonmode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs ex-
ceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore
essentially independent of supply voltage:

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## TYPICAL CIRCUIT CONNECTIONS



## DRIVING CAPACITIVE LOADS



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L} \max \leq 0.01 \mu \mathrm{~F}$.
Overshoot $\leq 20 \%$
Setting time (ts) $\geq 5 \mu \mathrm{~s}$

LF157. A LARGE POWER BW AMPLIFIER


For distortion < $1 \%$ and a 20 V p-p Vout swing power bandwidth is: 500 kHz .

## TYPICAL APPLICATIONS

> HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER


- $V_{\text {OUT }}=\frac{R 3}{R}\left[\frac{2 R 2}{R 1}+1\right] \Delta V, V-+2 V \leq V_{\text {iN }}$ Common-Mode $\leq V+$
- System Vos adjusted via A2 Vos adjust
- Trim R3 to boost up CMRR to 120 dB .


HIGH ACCURACY SAMPLE AND HOLD


- By closing the loop through A2 the Vout accuracy will be determined uniquely by A1. No Vos adjust required for A2.
- $T_{A}$ can be estimated by same considerations as previously but, because of the added on propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold.
- R1, $\mathrm{C}_{\mathrm{c}}$ : additional compensation
- Use LF156 for
$\Delta$ Fast settling time
$\Delta$ Low Vos


TYPICAL APPLICATIONS (Cont'd)


INVERTING UNITY GAIN FOR LF157


$$
\mathrm{R} 1 \mathrm{C} 1 \geq \frac{1}{(2 \pi)(5 \mathrm{MHZ})}
$$

$R 1=\frac{\mathrm{R} 2}{4}$
Avilde) $\approx-1$
$\mathrm{f}-3 \mathrm{~dB} \approx 5 \mathrm{MHz}$

WIDE BW LOW NOISE, LOW DRIFT AMPLIFIER


- Power BW: $\mathrm{fmax}^{\text {max }}=\frac{\mathrm{Sr}_{r}}{2 \pi / \mathrm{p}} \cong 240 \mathrm{kHz}$
- Parasitic input capacitance $\mathrm{C} 1 \cong(3 \mathrm{pF}$ for LF155, LF156, and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 $\cong$ R1C1.



## DESCRIPTION

The LM101, LM201, LM101A, LM201A, and LM301A are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

The LH2101A, LH2201A, LH2301A are dual amplifier using two LM101A type devices in the same hermetic package. All electrical specifications are the same as the single amplifiers.

## FEATURES

- Short circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch up
- LM101, LM101A Mil std 883A,B,C available
- LM101A Mil std 38510 (JAN) planned, Mil std M38510 processing available


## PIN CONFIGURATIONS



## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Supply Voltage |  |  |
| LH2101A, LH2201A, LM101, | $\pm 22$ | V |
| LM201, LM101A, LM201A | $\pm 18$ |  |
| LM301A, LH2301A | 500 | mW |
| Power dissipation1 | $\pm 30$ | V |
| Differential input voltage | $\pm 15$ | V |
| Input voltage2 | Indefinite |  |
| Output short circuit duration | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| LM101, LM101A, LH2101A | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| LM201A, LH2201A | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| LM201, LM301A, LH2301A | 300 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. Absolute maximum rating holds for all packages. The maximum junction temperature is $150^{\circ} \mathrm{C}$ for the LM101 and $100^{\circ} \mathrm{C}$ for the LM201. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{S} \leq+20 \mathrm{~V}$ unless otherwise specified.*

| PARAMETER |  | TEST CONDITIONS | LM101 |  |  | LM201 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{v}_{\text {os }}$ | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \mathrm{C}_{1}=30 \mathrm{pF} \\ \text { Over temp. } \end{gathered}$ |  | 1.0 | $\begin{aligned} & 5.0 \\ & 6.0 \\ & \hline \end{aligned}$ |  | 2.0 | $\begin{gathered} 7.5 \\ 10 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| $\mathrm{V}_{\text {OS }}$ | Drift | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 50 \Omega, \mathrm{C}_{1}=30 \mathrm{pF} \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \end{gathered}$ |  | $\begin{aligned} & 3.0 \\ & 6.0 \\ & \hline \end{aligned}$ |  |  | $\begin{gathered} \hline 6 \\ 10 \end{gathered}$ |  | $\begin{aligned} & \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ & \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{aligned}$ |
| los | Offset current | $\begin{gathered} \mathrm{C}_{1}=30 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=\text { high, } \mathrm{C}_{1}=30 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=10 \mathrm{w} \\ \text { Over temp. } \\ \mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \\ \hline \end{gathered}$ |  | $\begin{gathered} 40 \\ 10 \\ 100 \end{gathered}$ | $\begin{aligned} & 200 \\ & 200 \\ & 500 \end{aligned}$ |  | $\begin{gathered} 100 \\ \\ 50 \\ 150 \end{gathered}$ | $\begin{aligned} & 500 \\ & \\ & 400 \\ & 750 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $\mathrm{I}_{\text {BIAS }}$ | Input current | $\begin{gathered} \mathrm{C}_{1}=30 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}, \mathrm{C}_{1}=30 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 120 \\ & 280 \end{aligned}$ | $\begin{gathered} 500 \\ 1500 \end{gathered}$ |  | $\begin{aligned} & 250 \\ & 320 \\ & \hline \end{aligned}$ | $\begin{array}{r} 1500 \\ 2000 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{\text {CM }}$ | Common mode voltage range | Over temp., $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{C}_{1}=30 \mathrm{pF}$ | $\pm 12$ |  |  | $\pm 12$ |  |  | V |
| CMRR | Common mode rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \mathrm{C}_{1}=30 \mathrm{pF}$, over temp. | 70 | 90 |  | 65 | 90 |  | dB |
| RIN | Input resistance | $\mathrm{C}_{1}=30 \mathrm{pF}$ | 0.3 | 0.8 |  | 0.1 | 0.4 |  | $\mathrm{M} \Omega$ |
| $\mathrm{A}_{\text {VOL }}$ | Large signal voltage gain | $\begin{gathered} R_{L} \geq 2 k \Omega, \\ \text { VouT } \pm 10 \mathrm{~V}, V_{S}= \pm 15 \mathrm{~V} \\ \\ \text { Over temp. } \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \\ & \hline \end{aligned}$ | 160 |  | $\begin{aligned} & 20 \\ & 15 \\ & \hline \end{aligned}$ | 150 |  | $\begin{array}{\|l\|} \hline \mathrm{V} / \mathrm{mV} \\ \mathrm{~V} / \mathrm{mV} \end{array}$ |
|  | Supply current | $\mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}$ |  | 1.8 | 3.0 |  | 1.8 | 3.0 | mA |

*NOTE
Unless otherwise specified, all specifications for LM301A are $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq+20 \mathrm{~V}$ unless otherwise specified.*

| PARAMETER |  | TEST CONDITIONS | $\begin{aligned} & \text { LM101A/LM201A/ } \\ & \text { LH2101A/LH2201A } \\ & \hline \end{aligned}$ |  |  | LM301A/LH2301A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{v}_{\mathrm{os}}$ | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega, \mathrm{C}_{1}=30 \mathrm{pF} \\ \text { Over temp. } \end{gathered}$ |  | 0.7 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ |  | 2.0 | $\begin{aligned} & 7.5 \\ & 10 \end{aligned}$ | $\begin{aligned} & m V \\ & m V \end{aligned}$ |
| $\mathrm{V}_{\text {OS }}$ | Drift | $\mathrm{R}_{\mathrm{S}}=0 \Omega$, over temp. |  | 3.0 | 1.5 |  | 6.0 | 30 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| los | Offset current | $C_{1}=30 \mathrm{pF}$ <br> Over temp. |  | 1.5 | $\begin{aligned} & 10 \\ & 20 \end{aligned}$ |  | 3 | $\begin{aligned} & 50 \\ & 70 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Ios | Drift | $\begin{gathered} +25^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq \mathrm{T}_{\text {MAX }}, \mathrm{C}_{1}=30 \mathrm{pF} \\ \text { TMIN } \leq \mathrm{T}_{A} \leq+25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 0.01 \\ & 0.02 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.2 \end{aligned}$ |  | $\begin{aligned} & \hline 0.01 \\ & 0.02 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 0.3 \\ & 0.6 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} /{ }^{\circ} \mathrm{C} \\ & \mathrm{nA} /{ }^{\circ} \mathrm{C} \end{aligned}$ |
| $\mathrm{I}_{\text {BIAS }}$ | Input current | $\mathrm{C}_{1}=30 \mathrm{pF}$ Over temp. |  | 30 | $\begin{gathered} 75 \\ 100 \end{gathered}$ |  | 70 | $\begin{aligned} & 250 \\ & 300 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Common mode voltage range |  | $\pm 15$ |  |  | $\pm 12$ |  |  | V |
| CMRR | Common mode rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega$, $\mathrm{C}_{1}=30 \mathrm{pF}$, over temp. | 80 | 96 |  | 70 | 90 |  | dB |
| $\mathrm{R}_{\text {IN }}$ | Input resistance | $\mathrm{C}_{1}=30 \mathrm{pF}$ | 1.5 | 4 |  | 0.5 | 2 |  | $\mathrm{M} \Omega$ |
| $\mathrm{A}_{\mathrm{VOL}}$ | Large signal voltage gain | $\begin{aligned} & \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \text { VOUT } \pm 10 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ & \\ & \text { Over temp. } \end{aligned}$ | $\begin{aligned} & 50 \\ & 25 \\ & \hline \end{aligned}$ | 160 |  | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 160 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Supply current | $\begin{aligned} & \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \end{aligned}$ |  | 1.8 | 3.0 |  | 1.8 | 3.0 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

*NOTE
Unless otherwise specified, all specifications for LM301A are $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$.

## TYPCIAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS

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TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


GUARANTEED PERFORMANCE CHARACTERISTICS


INPUT VOLTAGE RANGE


## COMPENSATION CIRCUITS



## TYPICAL APPLICATIONS



NOTE: Pin numbers shown refer to $T$ or $N$ package only.


NOTE: Pin numbers shown refer to $T$ or $N$ package only.

## DESCRIPTION

The LM107/207/307 is a general purpose internally compensated operational amplifier. Advanced processing techniques provide input currents which are an order of magnitude lower than the $\mu \mathrm{A} 709$. Standard pin out allows plug in replacement for the $\mu \mathrm{A} 709$, LM101, LM101A, and the $\mu \mathrm{A} 741$.

## FEATURES

- 3 mV max offset voltage over temp
- 100nA max input current over temp
- 20nA max input offset current over temp
- Offsets guaranteed over common mode range
- Input/output short circuit protected
- Mil std 883A,B,C available


## PIN CONFIGURATIONS




EQUIVALENT SCHEMATIC


## GENERII PURPOSE OPERITIONHI MMPIIER

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Supply voltage |  |  |
| LM107 | $\pm 22$ | V |
| LM307 | $\pm 18$ | V |
| Power dissipation | 500 | V |
| Differential input voltage | $\pm 30$ | V |
| Input voltage | $\pm 15$ |  |
| Output short circuit duration | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| LM107 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| LM207 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| LM307 | 300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM107/LM207 |  |  | LM3074 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos <br> Vos | Offset voltage <br> Drift |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \text { over temp. } \\ \mathrm{RS}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega \text {, over temp. } \\ \mathrm{R}_{\mathrm{S}}=0 \Omega \text {, over temp. } \end{gathered}$ |  | $0.7$ $3.0$ | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ $15$ |  | 2.0 6.0 | $\begin{aligned} & 7.5 \\ & 10 \\ & 30 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV} \\ \mathrm{mV} \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| los <br> los | Offset current Drift | Over temp. $\begin{aligned} & 25^{\circ} \mathrm{C} \leq T_{A} \leq T \max \\ & T \min \leq T_{A} \leq 25^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{array}{\|l\|} \hline 1.5 \\ \\ 0.01 \\ 0.02 \end{array}$ | $\begin{aligned} & 10 \\ & 20 \\ & 0.1 \\ & 0.2 \end{aligned}$ |  | $\begin{gathered} 3 \\ 0.01 \\ 0.02 \end{gathered}$ | $\begin{aligned} & 50 \\ & 70 \\ & 0.3 \\ & 0.6 \end{aligned}$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{nA} \\ \mathrm{nA} /{ }^{\circ} \mathrm{C} \\ \mathrm{nA} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| IBIAS | Input current | Over temp. |  | 30 | $\begin{gathered} 75 \\ 100 \\ \hline \end{gathered}$ |  | 70 | $\begin{aligned} & 250 \\ & 300 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $V_{C M}$ | Common mode voltage range | $\begin{aligned} & V_{S}= \pm 20 \mathrm{~V}, \text { over temp. } \\ & V_{S}= \pm 15 \mathrm{~V}, \text { over temp. } \end{aligned}$ | $\pm 15$ |  |  | $\pm 12$ |  |  | V |
| CMRR | Common mode rejection ratio | RS $\leq \pm 10 \mathrm{k}$, over temp. $\mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k}$, over temp. | 80 | 96 |  |  | 70 | 90 | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| RIN | Input resistance |  | 1.5 | 4 |  | 0.5 | 2 |  | $\mathrm{M} \Omega$ |
| Avol | Large signal voltage gain | $\begin{array}{\|l\|} \hline R_{L} \geq 2 \mathrm{k} \Omega, V_{\text {OUT }} \pm 10 \mathrm{~V}, V_{S}= \pm 15 \mathrm{~V} \\ R_{L} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {OUT }} \pm 10 \mathrm{~V}, \mathrm{~V}_{S}= \pm 15 \mathrm{~V}, \text { over temp. } \\ \hline \end{array}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 160 |  | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 160 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Supply current | $T_{\text {A }}=+125^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}$ |  | 1.2 | 2.5 |  |  |  | mA |

NOTES

1. The maximum junction temperature of the $L M 1 X X$ is $150^{\circ} \mathrm{C}$, while that of the $L M 2 X X$ is $100^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short-circuit is allowed for case temperatures to $70^{\circ} \mathrm{C}$ and ambient temperatures to $55^{\circ} \mathrm{C}$.
4. All specifications shown for LM 307 are $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$.

## TYPICAL APPLICATIONS

INVERTING AMPLIFIER

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The LM108/108A series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible in most cases, to eliminate offset adjustments.

The LH2108 series are hybrids featuring two LM108A type dice in the same hermetic package. The electrical parameters are the same as the single amplifier.

## PIN CONFIGURATIONS



| FEATURES | LM108/208 | LM308 | LM108A/208A/ <br> 308A |
| :--- | :--- | :--- | :--- |
| Maximum input bias current | 3.0nA over temp. | 7.0nA <br> over temp. | 3.0nA over temp. <br> Offset current <br> than <br> $1.0 n \mathrm{~A}$ |
| Less than 400pA <br> Less than <br> Supply current (even in saturation) | $300 \mu \mathrm{~A}$ | $300 \mu \mathrm{~A}$ | $300 \mu \mathrm{~A}$ |
| Guaranteed drift characteristics |  |  | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Offset voltage guaranteed <br> Low current error |  |  |  |
| LM108, 208, 308, 108A Mil std 883A, <br> B,C available <br> LM108A Mil std M38510 (JAN) planned <br> LH2108A series-military qualification <br> pending |  |  |  |

EQUIVALENT SCHEMATIC


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING |  | UNIT |
| :---: | :---: | :---: | :---: |
|  | $\begin{gathered} \text { LH2108/LH2208 } \\ \text { LH2108A/LH2208A } \\ \text { LM108A/208A/ } \\ \text { 108/208 } \end{gathered}$ | $\begin{gathered} \text { LM308A/308 } \\ \text { LH2308A/LH2308 } \end{gathered}$ |  |
| Supply voltage | $\pm 20$ | $\pm 18$ | V |
| Power dissipation1,4 | 500 | 500 | mW |
| Differential input current2 | $\pm 10$ | $\pm 10$ | mA |
| Input voltage3 | $\pm 15$ | $\pm 15$ | V |
| Output short-circuit duration | Continuous | Continuous |  |
| Operating temperature range |  |  |  |
| LM108, LH2108 | -55 to +125 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| LM208, LH2208 | -25 to +85 |  | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering 10sec) | +300 | +300 | ${ }^{\circ} \mathrm{C}$ |

## NOTES

1. The maximum junction temperature of the LM108/108A is $150^{\circ} \mathrm{C}$, while that of the LM208/208A is $100^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient, or $45^{\circ} \mathrm{C} / \mathrm{W}$, junction to case. The thermal resistance of the dual-in-line package is $100^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
4. The maximum junction temperature of the LM308 is $85^{\circ} \mathrm{C}$. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient, or $45^{\circ} \mathrm{C} / \mathrm{W}$, junction to case. The thermal resistance of the dual-in-line package is $100^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient.

DC ELECTRICAL CHARACTERISTICS $\quad \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V}$ unless otherwise specified. 1,2

| PARAMETER |  | TEST CONDITIONS | LM108/LH2108 |  |  | LM208/LH2208 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ |  | . 7 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ |  | 0.7 | $\begin{aligned} & 2.0 \\ & 3.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos | Drift | $\mathrm{R}_{\mathrm{S}}=0 \Omega$, over temp. |  | 3.0 | 15 |  | 3.0 | 15 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| los | Offset current | Over temp. |  | 0.05 | $\begin{aligned} & 0.2 \\ & 0.4 \end{aligned}$ |  | 0.05 | $\begin{aligned} & 0.2 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| los | Drift | Over temp. |  | 0.5 | 2.5 |  | 0.5 | 2.5 | $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{I}_{\text {BIAS }}$ | Input current | Over temp. |  | 0.8 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ |  | 0.8 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | $\mathrm{nA}$ |
| $\mathrm{V}_{\text {CM }}$ | Common mode voltage range | Over temp. | $\pm 13.5$ |  |  | $\pm 13.5$ |  |  | V |
| CMRR | Common mode rejection ratio | $R_{S} \leq 10 k \Omega$, over temp. RS $\leq 10 \mathrm{k} \Omega,-25 \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ | 85 | 100 |  | 85 | 100 |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Rin | Input resistance |  | 30 | 70 |  | 30 | 70 |  | $\mathrm{M} \Omega$ |
| Vout | Output voltage swing | $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$, over temp. | $\pm 13$ | $\pm 14$ |  | $\pm 13$ | $\pm 14$ |  | V |
| Icc | Supply current | $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ |  | $\begin{gathered} 0.3 \\ 0.15 \end{gathered}$ |  | $\begin{aligned} & 0.6 \\ & 0.4 \end{aligned}$ | $\begin{gathered} \hline 0.3 \\ 0.15 \end{gathered}$ | $\begin{aligned} & 0.6 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| PSRR | Supply voltage rejection ratio | Rs $\leq 10 \mathrm{k} \Omega$, over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. | 80 | 96 |  | 80 | 96 |  | dB |
|  | Average temperature Coefficient of input Offset voltage ${ }^{2}$ | $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. |  | 3.0 | 15 |  | 3.0 | 15 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
|  | Coefficient of input Offset current | Over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{s}} \leq \pm 15 \mathrm{~V}$ |  | 0.5 | 2.5 |  | 0.5 | 2.5 | pA/ ${ }^{\circ} \mathrm{C}$ |

## NOTES

1. The maximum junction temperature of the LM 1 XX is $150^{\circ} \mathrm{C}$, while that of the LM 2 XX is $200^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. The LM 108 A has a guaranteed offset voltage less than 0.5 mV at $25^{\circ} \mathrm{C}$ and 1.0 mV for $-55^{\circ} \mathrm{C} \leq 125^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$. The average temperature coefficient of input offset voltage is guaranteed to be less than $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ for these same conditions.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V}$ unless otherwise specified. 1,2

| PARAMETER |  | TEST CONDITIONS | LM308/LH2308 |  |  | LM108A/LH2108A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \text { over temp. } \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V} \\ \mathrm{RS} \leq 10 \mathrm{k} \Omega, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}, \\ \text { over temp. } \end{gathered}$ |  | 2.0 | $\begin{aligned} & 7.5 \\ & 10 \end{aligned}$ |  | 0.3 | $\begin{aligned} & 0.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos | Drift | $\begin{gathered} \mathrm{R}_{\mathrm{S}}=0 \Omega, \text { over temp. } \\ \mathrm{RS}_{\mathrm{S}}=0 \Omega, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}, \\ \text { over temp. } \end{gathered}$ |  |  | 10 |  | 1.0 | 5.0 | $\begin{aligned} & \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ & \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{aligned}$ |
| los | Offset current | Over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$ <br> $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. |  | 0.2 | $\begin{gathered} 1 \\ 1.5 \\ \hline \end{gathered}$ |  | 0.05 | $\begin{aligned} & 0.2 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \hline \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| Ios | Drift | Over temp. <br> $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. |  | 2.0 | 10 |  | 0.5 | 2.5 | $\begin{aligned} & \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ & \mathrm{pA} /{ }^{\circ} \mathrm{C} \end{aligned}$ |
| IbIAS | Input current | Over temp. $\begin{gathered} \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \text {, over temp. } \end{gathered}$ |  | 1.5 | $\begin{aligned} & 7.0 \\ & 10 \\ & \hline \end{aligned}$ |  | 0.8 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Common mode voltage range | Over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. | $\pm 14 \mathrm{~V}$ |  |  | $\pm 13.5$ |  |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| CMRR | Common mode rejection ratio | Rs $\leq 10 \mathrm{k} \Omega$, over temp. $\mathrm{Rs} \leq 10 \mathrm{k} \Omega, \pm 5 \mathrm{~V} \leq \mathrm{V} \leq \pm 15 \mathrm{~V}$, over temp. | 80 | 100 |  | 96 | 110 |  | dB <br> dB |
| Rin | Input resistance |  | 10 | 40 |  | 30 | 70 |  | $\mathrm{M} \Omega$ |
| Vout | Output voltage swing | $R_{L}=10 k \Omega$, over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. | $\pm 13$ | $\pm 14$ |  | $\pm 13$ | $\pm 14$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| Icc | Supply current | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ |  | 0.3 | 0.8 |  | $\begin{gathered} 0.3 \\ 0.15 \end{gathered}$ | $\begin{aligned} & 0.6 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| PD | Power consumption | $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$ |  | 9.0 | 24 |  |  |  | mW |
| PSRR | Supply voltage rejection ratio | Rs $\leq 10 \mathrm{k} \Omega$, over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. | 80 | 96 |  | 96 | 110 |  | $\begin{aligned} & \hline \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
|  | Average temperature Coefficient of input Offset voltage2 Coefficient of input Offset current | $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. <br> Over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$ |  | $\begin{aligned} & 6.0 \\ & 2.0 \end{aligned}$ | 30 <br> 10 |  | 1.0 0.5 | 5.0 2.5 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br> $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br> $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br> $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ <br> $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |

NOTES

1. The maximum junction temperature of the LM1XX is $150^{\circ} \mathrm{C}$, while that of the LM 2 XX is $200^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. The LM108A has a guaranteed offset voltage less than 0.5 mV at $25^{\circ} \mathrm{C}$ and 1.0 mV for $-55^{\circ} \mathrm{C} \leq 125^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$. The average temperature coefficient of input offset voltage is guaranteed to be less than $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ for these same conditions.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V}$ unless otherwise specified. 1,2

| PARAMETER |  | TEST CONDITIONS | LM208A/LH2208A |  |  | LM308A/LH2308A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{s}} \leq 10 \mathrm{k} \Omega \\ \mathrm{Rs} \leq 10 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ |  | 0.3 | $\begin{aligned} & \hline 0.5 \\ & 1.0 \end{aligned}$ |  | 0.3 | $\begin{aligned} & 0.5 \\ & .75 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos | Drift | $\mathrm{R}_{\mathrm{S}}=0 \Omega$, over temp. |  | 1.0 | 5.0 |  | 1.0 | 5.0 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| los | Offset current | Over temp. |  | 0.05 | $\begin{aligned} & 0.2 \\ & 0.4 \end{aligned}$ |  |  | $\begin{gathered} 1 \\ 1.5 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| los | Drift | Over temp. |  | 0.5 | 2.5 |  | 2.0 | 10 | $\mathrm{PA} /{ }^{\circ} \mathrm{C}$ |
| İIAS | Input current | Over temp. |  | 0.8 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ |  | 1.5 | $\begin{aligned} & 7.0 \\ & 10 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| VCM | Common mode voltage range | Over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. | $\pm 13.5$ |  |  | $\pm 14$ |  |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| CMRR | Common mode rejection ratio | $R_{S} \leq 10 \mathrm{k} \Omega,-25 \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ <br> Rs $\leq 10 \mathrm{k} \Omega, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{s}} \leq \pm 15 \mathrm{~V}$, over temp. | 96 | 110 |  | 96 | 110 |  | $\begin{aligned} & d B \\ & d B \end{aligned}$ |
| Rin | Input resistance | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\text {S }} \leq \pm 15 \mathrm{~V}$ | 30 | 70 |  | 10 | 40 |  | $\begin{aligned} & \mathrm{M} \Omega \\ & \mathrm{M} \Omega \end{aligned}$ |
| Vout | Output voltage swing | $R_{L}=10 \mathrm{k} \Omega$, over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. | $\pm 13$ | $\pm 14$ |  | $\pm 13$ | $\pm 14$ |  | $\mathrm{V}$ |
| Icc | Supply current | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline 0.3 \\ 0.15 \end{gathered}$ | $\begin{aligned} & 0.6 \\ & 0.4 \end{aligned}$ |  | 0.3 | 0.8 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| PD | Power consumption | $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{s}} \leq \pm 15 \mathrm{~V}$ |  |  |  |  | 9.0 | 24 | mW |
| PSRR | Supply voltage rejection ratio | $R_{S} \leq 10 \mathrm{k} \Omega$, over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. | 96 | 110 |  | 96 | 110 |  | $\begin{aligned} & \hline \mathrm{dB} \\ & \mathrm{~dB} \\ & \hline \end{aligned}$ |
|  | Average temperature Coefficient of input Offset voltage ${ }^{2}$ Coefficient of input Offset current | $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$, over temp. <br> Over temp. $\pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}$ |  | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | $5.0$ $2.5$ |  | $\begin{aligned} & 1.0 \\ & 2.0 \end{aligned}$ | 5.0 10 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br> $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br> $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ <br> $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |

NOTES

1. The maximum junction temperature of the LM1XX is $150^{\circ} \mathrm{C}$, while that of the LM2XX is $200^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. The LM108A has a guaranteed offset voltage less than 0.5 mV at $25^{\circ} \mathrm{C}$ and 1.0 mV for $-55^{\circ} \mathrm{C} \leq 125^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$. The average temperature coefficient of input offset voltage is guaranteed to be less than $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ for these same conditions.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM108/LH2108 |  |  | LM208/LH2208 |  |  | LM308/LH2308 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Avol | Large signal voltage gain ${ }^{\text {1 }}$ |  | $R \mathrm{~L} \geq 10 \mathrm{k} \Omega$ Over temp. $\begin{gathered} V_{S}=15 \mathrm{~V}, \mathrm{~V}_{\text {OuT }}= \pm 10 \mathrm{~V}, \\ R_{\mathrm{L}} \geq 10 \mathrm{k} \\ \text { Over temp. } \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 300 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 300 |  | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 300 |  | $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ |

NOTE

1. The maximum junction temperature of the LM1XX is $150^{\circ} \mathrm{C}$, while that of the LM2XX is $200^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \pm 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM108A/LH2108A |  |  | LM208A/LH2208A |  |  | LM308A/LH2308A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Avol | Large signal voltage gain ${ }^{1}$ |  | $R_{L} \geq 10 \mathrm{k} \Omega$ Over temp. $\begin{gathered} V_{S}=15 \mathrm{~V}, \mathrm{~V} \text { out }= \pm 10 \mathrm{~V}, \\ \mathrm{R}_{\mathrm{L}} \geq 10 \mathrm{k} \\ \text { Over temp. } \end{gathered}$ | $\begin{aligned} & 80 \\ & 40 \end{aligned}$ | 300 |  | $\begin{aligned} & 80 \\ & 40 \end{aligned}$ | 300 |  | $\begin{aligned} & 80 \\ & 60 \end{aligned}$ | 300 |  | $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ |

NOTE

1. The maximum junction temperature of the $L M 1 X X$ is $150^{\circ} \mathrm{C}$, while that of the $L M 2 X X$ is
$200^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices must be derated based on the
thermal resistance of the package as given in the package information section.

TYPICAL PERFORMANCE CHARACTERISTICS LM108/208


TYPICAL PERFORMANCE CHARACTERISTICS LM108/208 (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS LM308


TYPICAL PERFORMANCE CHARACTERISTICS LM308 (Cont'd)


## VOLTAGE FOLLOWER PULSE RESPONSE





## TEST LOAD CIRCUITS

STANDARD COMPENSATION


## DESCRIPTION

The LM124/SA534 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.
The LM158 series consists of two operational amplifiers designed as above. Operation from dual supplies is also possible for both series and the low power supply current drain is independent of the magnitude of the power supply voltage.

## FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain-(100dB)
- Wide bandwidth (unity gain) -1 MHz (temperature compensated)
- Wide power supply range

Single supply-( 3 Vdc to 30 Vdc ) or dual supplies-( $\pm 1.5 \mathrm{Vdc}$ to $\pm 15 \mathrm{Vdc}$ )

- Very low supply current drainessentially independent of supply voltage ( $1 \mathrm{~mW} / \mathrm{op}$ amp at +5 Vdc )
- Low input biasing current-(45nAdc temperature compensated)
- Low input offset voltage-( 2 mVdc ) and offset current-(5nAdc)
- Differential input voltage range equal to the power supply voltage
- Large output voltage-(0Vdc to V+— 1.5 Vdc swing)
- LM124 Mil std 883A,B,C available


## UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
The unity gain cross frequency is temperature compensated.

The input bias current is also temperature compensated.

## EQUIVALENT SCHEMATIC



## PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| V+ | Supply voltage | 32 or $\pm 16$ | Vdc |
|  | Differential input voltage | 32 | Vdc |
|  | Input voltage | -0.3 to +32 | Vdc |
|  | Power dissipation ${ }^{1}$ |  |  |
|  | T package | 680 | mW |
|  | N package | 570 | mW |
|  | F package | 900 | mW |
|  | Output short-circuit to GND |  | $\cdots$ |
|  | 1 amplifier2 | Continuous |  |
|  | Input current ( $\mathrm{V}_{\text {IN }}<-0.3 \mathrm{~V}$ ) 3 | 50 | mA |
|  | Operating temperature range |  |  |
|  | LM324A, LM324, LM358 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
|  | LM224A, LM224, LM258 | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
|  | SA534 | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
|  | LM124A, LM124, LM158 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
|  | Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
|  | Lead temperature (soldering, 10sec) | 300 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. For operating at high temperatures, all devices must be derated based on a $+125^{\circ} \mathrm{C}$ maximum junction temperature and a thermal resistance of $175^{\circ} \mathrm{C} / \mathrm{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. LM124/224 and LM158/258 can be derated based on a $150^{\circ} \mathrm{C}$ maximum junction temperature.
2. Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $\mathrm{V}+$. At values of supply voltage in excess of +15 Vdc continuous shortcircuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM124A |  |  | LM224A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| vos <br> Vos | Offset voltage ${ }^{1}$ <br> Drift |  | $\begin{gathered} \mathrm{R}_{\mathrm{s}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \text {, over temp. } \\ \mathrm{RS}_{\mathrm{S}}=0 \Omega \text {, over temp. } \end{gathered}$ |  | $\begin{aligned} & 1 \\ & 7 \end{aligned}$ | $\begin{gathered} 2 \\ 4 \\ 20 \end{gathered}$ |  | $\begin{aligned} & 1 \\ & 7 \end{aligned}$ | $\begin{gathered} 3 \\ 4 \\ 20 \end{gathered}$ | $\begin{array}{\|c\|} \mathrm{mV} \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{array}$ |
| IbIAS | Input current ${ }^{2}$ | $\begin{gathered} \operatorname{liN}(+)-\operatorname{liN}(-) \\ \operatorname{liN}(+)-\operatorname{liN}(-), \text { over temp. } \end{gathered}$ |  | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ | $\begin{gathered} 50 \\ 100 \end{gathered}$ |  | $\begin{aligned} & 40 \\ & 40 \end{aligned}$ | $\begin{gathered} 80 \\ 100 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $\begin{aligned} & \hline \text { los } \\ & \text { los } \end{aligned}$ | Offset current <br> Drift | $\begin{array}{r} \operatorname{lin}(+)-\operatorname{liN}(-) \\ \operatorname{lin}(+)-\operatorname{lin}(-), \text { over temp. } \\ \text { over temp. } \\ \hline \end{array}$ |  | $\begin{aligned} & 2 \\ & 10 \end{aligned}$ | $\begin{aligned} & 10 \\ & 30 \\ & 200 \end{aligned}$ |  | $\begin{aligned} & 2 \\ & 10 \end{aligned}$ | $\begin{gathered} 15 \\ 30 \\ 200 \end{gathered}$ | $\begin{array}{c\|} \hline \mathrm{nA} \\ \mathrm{nA} \\ \mathrm{pA} /{ }^{\circ} \mathrm{C} \end{array}$ |
| $\mathrm{V}_{\mathrm{CM}}$ <br> CMRR | Common mode voltage range ${ }^{3}$ <br> Common mode rejection ratio | $\begin{gathered} \mathrm{V}+=30 \mathrm{~V} \\ \mathrm{~V}+=30 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{gathered} 0 \\ 0 \\ 70 \end{gathered}$ | 85 | $\begin{array}{\|c\|} \hline \mathrm{V}+-1.5 \\ \mathrm{~V}+-2 \end{array}$ | $\begin{gathered} \hline 0 \\ 0 \\ 70 \end{gathered}$ | 85 | $\begin{array}{\|c} \hline v+-1.5 \\ v+-2 \end{array}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~dB} \end{gathered}$ |
| Vout Vor Vol | Output voltage swing | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}+=+30 \mathrm{~V} \text {, over temp. } \\ \mathrm{R}_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \text { over temp } \\ \mathrm{R}_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \mathrm{~V}+=5 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| Icc | Supply current | $R_{L}=\infty, V_{C C}=30 \mathrm{~V}$, over temp. <br> $R_{L}=\infty$, on all op amps, over temp. |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} \hline 3 \\ 1.2 \end{gathered}$ |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{\mathrm{O}} \text { swing), } \\ \mathrm{R} \geq 2 \mathrm{k} \Omega \\ \mathrm{~V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{\mathrm{O}} \text { swing) }, \\ \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \text { over temp. } \\ \hline \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Amplifier-to-amplifier coupling ${ }^{4}$ | $\begin{gathered} \mathrm{f}=1 \mathrm{kHz} \text { to } 20 \mathrm{kHz}, \\ \text { input referred } \end{gathered}$ |  | -120 |  |  | -120 |  | dB |
| PSRR |  | RS $\leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | 65 | 100 |  | dB |
|  | Output current Source <br> Sink | ```\(\mathrm{V}_{\mathrm{IN}}+=+1 \mathrm{Vdc}, \mathrm{V}_{\mathrm{IN}^{-}}=0 \mathrm{Vdc}\), \(\mathrm{V}+=15 \mathrm{Vdc}\) \(\mathrm{V}_{\mathrm{IN}^{+}}=+1 \mathrm{Vdc}, \mathrm{V}_{\mathrm{IN}^{-}}=0 \mathrm{Vdc}\), \(\mathrm{V}+=15 \mathrm{Vdc}\), over temp. \(\mathrm{V}_{\mathrm{N}^{-}}=+1 \mathrm{Vdc}, \mathrm{V}_{\mathrm{IN}^{+}}=0 \mathrm{Vdc}\), \(\mathrm{V}+=15 \mathrm{Vdc}\) \(\mathrm{V}_{\mathrm{IN}^{-}}=+1 \mathrm{Vdc}, \mathrm{V}_{\mathrm{IN}^{+}}=0 \mathrm{Vdc}\), \(\mathrm{V}+=15 \mathrm{Vdc}\), over temp. \(\mathrm{V}_{\mathrm{IN}}-=+1 \mathrm{Vdc}, \mathrm{V}_{\mathrm{O}}=200 \mathrm{mV}\)``` | $\begin{aligned} & 20 \\ & 10 \\ & 10 \\ & 10 \\ & 10 \\ & 12 \\ & \hline \end{aligned}$ | 40 <br> 20 <br> 20 <br> 15 <br> 50 |  | $\begin{gathered} 20 \\ 10 \\ 10 \\ 5 \\ 12 \\ \hline \end{gathered}$ | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | mA <br> mA <br> mA <br> mA <br> $\mu \mathrm{A}$ |
| Isc | Short circuit current ${ }^{4}$ |  |  | 40 | 60 |  | 40 | 60 | mA |
|  | Differential input voltage6 |  |  |  | V+ |  |  | V+ | V |

NOTES

1. $\mathrm{V}_{\mathrm{O}} \cong 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}}=0 \Omega$ with $\mathrm{V}+$ from 5 V to 30 V and over full input common mode range ( $\mathrm{OVdc}+$ to $\mathrm{V}+-1.5 \mathrm{~V}$ ).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5$, but either or both inputs can go to +32 V without damage.
4. Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $\mathrm{V}+$. At values of supply voltage in excess of +15 Vdc continous shortcircuits can 'exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to +32 Vdc without damage.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM324A |  |  | LM124/LM224/LM158/LM258 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos <br> Vos | Offset voltage ${ }^{1}$ <br> Drift |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \text { over temp. } \\ \mathrm{R}_{S}=0 \Omega \text {, over temp. } \end{gathered}$ |  | $2$ $7$ | $\begin{gathered} 3 \\ 5 \\ 30 \\ \hline \end{gathered}$ |  | $\begin{gathered} \pm 2 \\ 7 \\ \hline \end{gathered}$ | $\begin{aligned} & \pm 5 \\ & \pm 7 \end{aligned}$ | $\begin{array}{\|c\|} \hline \mathrm{mV} \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \hline \end{array}$ |
| IBIAS | Input current ${ }^{2}$ | $\begin{gathered} \operatorname{lin}(+)-\operatorname{lin}(-) \\ \operatorname{lin}(+)-\operatorname{lin}(-), \text { over temp. } \\ \hline \end{gathered}$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 100 \\ & 200 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 150 \\ & 300 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{los} \\ & \mathrm{los} \\ & \hline \end{aligned}$ | Offset current Drift | $\begin{array}{r} \operatorname{lin}(+)-\operatorname{lin}(-) \\ \operatorname{lin}(+)-\operatorname{lin}(-), \text { over temp. } \\ \text { over temp. } \\ \hline \end{array}$ |  | $\begin{gathered} 5 \\ 10 \end{gathered}$ | $\begin{array}{r} 30 \\ 75 \\ 300 \\ \hline \end{array}$ |  | $\begin{aligned} & \pm 3 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} \pm 30 \\ \pm 100 \end{gathered}$ | $\begin{array}{\|c\|} \hline \mathrm{nA} \\ \mathrm{nA} \\ \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ \hline \end{array}$ |
| $V_{\text {CM }}$ <br> CMRR | Common mode voltage range ${ }^{3}$ <br> Common mode rejection ratio | $\begin{gathered} \mathrm{V}+=30 \mathrm{~V} \\ \mathrm{~V}+=30 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{gathered} \hline 0 \\ 0 \\ 65 \end{gathered}$ | 85 | $\begin{array}{\|c\|} \hline \mathrm{V}+-1.5 \\ \mathrm{~V}+-2 \end{array}$ | $\begin{gathered} \hline 0 \\ 0 \\ 70 \end{gathered}$ | 85 | $\begin{gathered} v+-1.5 \\ v+-2 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~dB} \end{gathered}$ |
| Vout <br> VOH <br> VoL | Output voltage swing | $\begin{gathered} R_{L}=2 k \Omega, V+=+30 \mathrm{~V} \text {, over temp. } \\ R_{L} \leq 10 k \Omega \text {, over temp } \\ R_{L} \leq 10 \mathrm{k} \Omega, \mathrm{~V}+=5 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \\ \hline \end{gathered}$ | 20 | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \\ \hline \end{gathered}$ | 20 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{v} \end{aligned}$ |
| Icc | Supply current | $R_{L}=\infty, V_{C C}=30 V$, over temp. $R_{L}=\infty$, on all op amps, over temp. |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{\mathrm{O}} \text { swing); } \\ \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \\ \mathrm{~V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{\mathrm{O}} \text { swing), }, \\ \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \text {, over temp. } \\ \hline \end{gathered}$ | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Amplifier-to-amplifier coupling4 | $\begin{gathered} \mathrm{f}=1 \mathrm{kHz} \text { to } 20 \mathrm{kHz}, \\ \text { input referred } \end{gathered}$ |  | -120 |  |  | -120 |  | dB |
| PSRR |  | $\mathrm{RS} \leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | 65 | 100 |  | dB |
|  | Output current Source <br> Sink |  | $\begin{aligned} & 20 \\ & 10 \\ & 10 \\ & 5 \\ & 12 \\ & \hline \end{aligned}$ | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | $\begin{gathered} 20 \\ 10 \\ 10 \\ 5 \\ 12 \\ \hline \end{gathered}$ | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | mA <br> mA <br> mA <br> mA <br> $\mu \mathrm{A}$ |
| Isc | Short circuit current ${ }^{4}$ |  |  | 40 | 60 |  | 40 | 60 | mA |
|  | Differential input voltage ${ }^{6}$ |  |  |  | V+ |  |  | V+ | V |

## NOTES

1. $\mathrm{V}_{\mathrm{O}} \cong 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}}=0 \Omega$ with $\mathrm{V}+$ from 5 V to 30 V and over full input common mode range ( $\mathrm{OVdc}+$ to $\mathrm{V}+-1.5 \mathrm{~V}$ ).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5$, but either or both inputs can go to +32 V without damage.
4. Short circuits from the output to $\mathrm{V}+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $\mathrm{V}+$. At values of supply voltage in excess of +15 Vdc continous shortcircuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to +32 Vdc without damage.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM324/LM358 |  |  | SA534 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos <br> Vos | Offset voltage ${ }^{1}$ <br> Drift |  | $\begin{gathered} \mathrm{Rs} \leq 10 \mathrm{k} \Omega \\ \mathrm{Rs}_{\mathrm{s}} \leq 10 \mathrm{k} \Omega \text {, over temp. } \\ \mathrm{Rs}_{\mathrm{S}}=0 \Omega \text {, over temp. } \end{gathered}$ |  | $\begin{gathered} \pm 2 \\ 7 \end{gathered}$ | $\begin{aligned} & \pm 7 \\ & \pm 9 \end{aligned}$ |  | $\begin{gathered} \pm 2 \\ 7 \\ \hline \end{gathered}$ | $\begin{aligned} & \pm 7 \\ & \pm 9 \end{aligned}$ | $\left\|\begin{array}{c} \mathrm{mV} \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{array}\right\|$ |
| IBIAS | Input current2 | $\begin{gathered} \operatorname{liN}(+)-\operatorname{liN}(-) \\ \operatorname{liN}(+)-\operatorname{liN}(-), \text { over temp. } \end{gathered}$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 250 \\ & 500 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 250 \\ & 500 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Ios <br> los | Offset current <br> Drift | $\begin{array}{r} \operatorname{liN}(+)-\operatorname{liN}(-) \\ \operatorname{liN}(+)-\operatorname{liN}(-) ; \text { over temp. } \\ \text { over temp. } \end{array}$ |  | $\begin{aligned} & \pm 5 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} \pm 50 \\ \pm 150 \end{gathered}$ |  | $\begin{aligned} & \pm 5 \\ & 10 \end{aligned}$ | $\begin{gathered} \pm 50 \\ \pm 150 \end{gathered}$ | $\begin{array}{\|c\|} \hline \mathrm{nA} \\ \mathrm{nA} \\ \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ \hline \end{array}$ |
| VCM <br> CMRR | Common mode voltage range ${ }^{3}$ <br> Common mode rejection ratio | $\begin{gathered} \mathrm{V}+=30 \mathrm{~V} \\ \mathrm{~V}+=30 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{gathered} \hline 0 \\ 0 \\ 65 \\ \hline \end{gathered}$ | 70 | $\begin{gathered} V+-1.5 \\ V+-2 \end{gathered}$ | $\begin{gathered} 0 \\ 0 \\ 65 \\ \hline \end{gathered}$ | 70 | $\begin{gathered} V+-1.5 \\ V+-2 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~dB} \end{gathered}$ |
| VOUT <br> VOH <br> VOL | Output voltage swing | $\begin{gathered} \hline R_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}+=+30 \mathrm{~V}, \text { over temp. } \\ R_{\mathrm{L}} \leq 10 \mathrm{k} \Omega \text {, over temp } \\ \mathrm{R}_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \mathrm{~V}+=5 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \\ \hline \end{gathered}$ | 20 | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \\ \hline \end{gathered}$ | 20 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| Icc | Supply current | $R_{L}=\infty, V_{C C}=30 \mathrm{~V}$, over temp. <br> $R_{L}=\infty$, on all op amps, over temp. | $\cdot$ | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{\mathrm{O}} \text { swing), } \\ \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \\ \mathrm{~V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{O} \text { swing), } \\ R_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 |  | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 |  | $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ |
|  | Amplifier-to-amplifier coupling ${ }^{4}$ | $\begin{gathered} f=1 \mathrm{kHz} \text { to } 20 \mathrm{kHz}, \\ \text { input referred } \end{gathered}$ |  | -120 |  |  | -120 |  | dB |
| PSRR |  | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | 65 | 100 |  | dB |
|  | Output current Source <br> Sink |  | 20 <br> 10 <br> 10 <br> 5 <br> 12 | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | 20 <br> 10 <br> 10 <br> 5 <br> 12 | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| Isc | Short circuit current ${ }^{4}$ |  |  | 40 | 60 |  | 40 | 60 | mA |
|  | Differential input voltage 6 |  |  |  | V+ |  |  | V+ | V |

## NOTES

1. $\mathrm{V}_{\mathrm{O}} \cong 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}}=0 \Omega$ with $\mathrm{V}+$ from 5 V to 30 V and over full input common mode range ( $\mathrm{OVdc}+$ to $\mathrm{V}+-1.5 \mathrm{~V}$ )
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5$, but either or both inputs can go to +32 V without damage.
4. Short circuits from the output to $\mathrm{V}+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $\mathrm{V}+$. At values of supply voltage in excess of +15 Vdc continous shortcircuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to +32 Vdc without damage.

DC ELECTRICAL CHARACTERISTICS $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM158A |  |  | LM258A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos <br> Vos | Offset voltage ${ }^{1}$ <br> Drift |  | $R_{S} \leq 10 k \Omega$ <br> $R_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$, over temp. <br> $R_{S}=0 \Omega$, over temp. |  | $7$ | $\begin{gathered} 2 \\ 4 \\ 15 \end{gathered}$ |  | 7 | $\begin{gathered} 3 \\ 4 \\ 15 \end{gathered}$ | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| IBIAS | Input current2 | $\begin{gathered} \operatorname{liN}(+)-\operatorname{IIN}(-) \\ \operatorname{IIN}(+)-\operatorname{IiN}(-), \text { over temp. } \end{gathered}$ |  | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ | $\begin{gathered} 50 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 40 \\ & 40 \end{aligned}$ | $\begin{gathered} 80 \\ 100 \end{gathered}$ | $\begin{aligned} & \hline \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| los <br> los | Offset current <br> Drift | $\operatorname{lin}(+)-\operatorname{lin}(-)$ <br> $\operatorname{liN}(+)-\operatorname{liN}(-)$, over temp. over temp. |  | $\begin{gathered} 2 \\ 10 \end{gathered}$ | $\begin{gathered} 10 \\ 30 \\ 200 \end{gathered}$ |  | 2 10 | $\begin{aligned} & 15 \\ & 30 \\ & 200 \end{aligned}$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{nA} \\ \mathrm{pA} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| $V_{C M}$ <br> CMRR | Common mode voltage range ${ }^{3}$ <br> Common mode rejection ratio | $\begin{gathered} \mathrm{V}+=30 \mathrm{~V} \\ \mathrm{~V}+=30 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{gathered} \hline 0 \\ 0 \\ 70 \end{gathered}$ | 85 | $\begin{gathered} \mathrm{V}+-1.5 \\ \mathrm{~V}+-2 \end{gathered}$ | $\begin{gathered} \hline 0 \\ 0 \\ 70 \end{gathered}$ | 85 | $\begin{gathered} v+-1.5 \\ v+-2 \end{gathered}$ | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~dB} \end{gathered}$ |
| Vout <br> V OH <br> Vol | Output voltage swing | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}+=+30 \mathrm{~V}, \text { over temp. } \\ R_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \text { over temp } \\ R_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \mathrm{~V}+=5 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Icc | Supply current | $R_{L}=\infty, V_{C C}=30 V$, over temp. $R_{L}=\infty$, on all op amps, over temp. |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \hline V+=+15 \mathrm{~V} \text { (for large } V_{0} \text { swing), } \\ R_{L} \geq 2 k \Omega \\ V+=+15 \mathrm{~V} \text { (for large } V_{O} \text { swing), } \\ R_{L} \geq 2 k \Omega \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & \hline \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Amplifier-to-amplifier coupling 4 | $f=1 \mathrm{kHz} \text { to } 20 \mathrm{kHz},$ input referred |  | -120 |  | $\cdots$ | -120 |  | dB |
| PSRR |  | $\mathrm{RS} \leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | 65 | 100 |  | dB |
|  | Output current Source <br> Sink |  | $\begin{aligned} & 20 \\ & 10 \\ & 10 \\ & 5 \\ & 12 \\ & \hline \end{aligned}$ | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | $\begin{aligned} & 20 \\ & 10 \\ & 10 \\ & 5 \\ & 12 \\ & \hline \end{aligned}$ | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | mA <br> mA <br> mA <br> mA <br> $\mu \mathrm{A}$ |
| Isc | Short circuit current ${ }^{4}$ |  |  | 40 | 60 |  | 40 | 60 | mA |
|  | Differential input voltage ${ }^{6}$ |  |  |  | V+ |  |  | V+ | V |

NOTES

1. $V_{O} \cong 1.4 \mathrm{Vdc}, R \mathrm{~S}=0 \Omega$ with $\mathrm{V}+$ from 5 V to 30 V and over full input common mode range ( $\mathrm{OVdc}+$ to $\mathrm{V}+-1.5 \mathrm{~V}$ ).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5$, but either or both inputs can go to +32 V without damage.
4. Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $\mathrm{V}+$. At values of supply voltage in excess of +15 Vdc continous shortcircuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to +32 Vdc without damage.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LM358A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vos <br> Vos | Offset voltage 1 <br> Drift |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \text {, over temp. } \\ \mathrm{R}_{\mathrm{S}}=0 \Omega \text {, over temp. } \end{gathered}$ |  | $\begin{aligned} & 2 \\ & 7 \end{aligned}$ | $\begin{gathered} 3 \\ 5 \\ 20 \end{gathered}$ | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| IBIAS | Input current2 | $\begin{gathered} \operatorname{liN}(+)-\operatorname{liN}(-) \\ \operatorname{liN}(+)-\operatorname{liN}(-), \text { over temp. } \end{gathered}$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 100 \\ & 200 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| los <br> los | Offset current Drift | $\begin{array}{r} \operatorname{liN}(+)-\operatorname{liN}(-) \\ \operatorname{liN}(+)-\operatorname{liN}(-), \text { over temp. } \\ \text { over temp. } \\ \hline \end{array}$ |  | 5 <br> 10 | $\begin{array}{r} 30 \\ 75 \\ 300 \\ \hline \end{array}$ | nA nA $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| VCM <br> CMRR | Common mode voltage range ${ }^{3}$ <br> Common mode rejection ratio | $\begin{gathered} \mathrm{V}+=30 \mathrm{~V} \\ \mathrm{~V}+=30 \mathrm{~V}, \text { over temp. } \end{gathered}$ | $\begin{gathered} 0 \\ 0 \\ 65 \\ \hline \end{gathered}$ | 85 | $\begin{gathered} \mathrm{V}+-1.5 \\ \mathrm{~V}+-2 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~dB} \end{gathered}$ |
| Vout <br> VOH <br> VOL | Output voltage swing | $\begin{gathered} \hline R_{L}=2 k \Omega, \mathrm{~V}+=+30 \mathrm{~V}, \text { over temp. } \\ R_{\mathrm{L}} \leq 10 \mathrm{k} \Omega \text {, over temp } \\ \mathrm{R}_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \mathrm{~V}+=5 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & \hline 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| Icc | Supply current | $R_{L}=\infty, V_{C C}=30 \mathrm{~V} \text {, over temp. }$ <br> $\mathrm{R}_{\mathrm{L}}=\infty$, on all op amps, over temp. |  | $\begin{aligned} & 1.5 \\ & 0.7 \end{aligned}$ | $\begin{gathered} 3 \\ 1.2 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{\mathrm{O}} \text { swing) } \\ \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \\ \mathrm{~V}+=+15 \mathrm{~V} \text { (for large } \mathrm{V}_{\mathrm{O}} \text { swing) }, \\ \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ | $25$ <br> 15 | 100 |  | $\mathrm{V} / \mathrm{mV}$ <br> $\mathrm{V} / \mathrm{mV}$ |
|  | Amplifier-to-amplifier coupling4 | $\begin{gathered} \mathrm{f}=1 \mathrm{kHz} \text { to } 20 \mathrm{kHz}, \\ \text { input referred } \end{gathered}$ |  | -120 |  | dB |
| PSRR |  | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | dB |
|  | Output current Source <br> Sink |  | $\begin{aligned} & 20 \\ & 10 \\ & 10 \\ & 5 \\ & 12 \end{aligned}$ | 40 <br> 20 <br> 20 <br> 8 <br> 50 |  | mA <br> mA <br> mA <br> mA <br> $\mu \mathrm{A}$ |
| ISC | Short circuit current ${ }^{4}$ |  |  | 40 | 60 | mA |
|  | Differential input voltage ${ }^{6}$ |  |  |  | V+ | V |

NOTES

1. $\mathrm{V}_{\mathrm{O}} \cong 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}}=0 \Omega$ with $\mathrm{V}+$ from 5 V to 30 V and over full input common mode range (OVdc+ to $\mathrm{V}+-1.5 \mathrm{~V}$ ).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5$, but either or both inputs can go to +32 V without damage.
4. Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $\mathrm{V}+$. At values of supply voltage in excess of +15 Vdc continous shortcircuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to +32 Vdc without damage.

## TYPICAL PERFORMANCE CHARACTERISTICS



LARGE SIGNAL
FREQUENCY RESPONSE


VOLTAGE FOLLOWER PULSE RESPONSE


## DESCRIPTION

The MC1456/1556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The MC1456/1556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

OFFSET ADJUST CIRCUIT


PIN CONFIGURATIONS


## FEATURES

- Low input bias current-15nA maximum
- Low input offset current-2.0nA maximum
- Low input offset voltage-4.0mV maximum
- High slew rate-2.5V/ $\mu$ s typical
- Large power bandwidth- 40 kHz typical
- Low power consumption-45mW maximum
- Offset voltage null capability
- Output short circuit protection
- Input over-voltage protection
- Mil std 883A,B,C, available



## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Power supply voltage MC1556 | MC1456 | $\pm 22$ |
| V |  |  |
| Differential input voltage | $\pm 18$ | V |
| Common mode input voltage | $\pm \mathrm{VCC}$ | V |
| Load current | 20 | V |
| Output short circuit duration | Continuous | mA |
| Power dissipation | 680 | mW |
| Derate above $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 4.6 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| MC1556 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| MC1456 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified

| PARAMETER |  | TEST CONDITIONS | MC1556 |  |  | MC1456 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | Over temperature |  | 2.0 | $\begin{aligned} & 4.0 \\ & 6.0 \end{aligned}$ |  | 5.0 | $\begin{aligned} & 10.0 \\ & 14.0 \end{aligned}$ | $m V d c$ <br> mVdc |
| Ios | Offset current | $\begin{gathered} 0^{\circ} \mathrm{C} \leq T_{A} \leq 70^{\circ} \mathrm{C} \\ 25^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq 125^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq 25^{\circ} \mathrm{C} \\ \hline \end{gathered}$ |  | 1.0 | $\begin{aligned} & 2.0 \\ & 3.0 \\ & 5.0 \\ & \hline \end{aligned}$ |  | 5.0 | $\begin{gathered} 10.0 \\ 14 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IBIAS | Input current | Over temperature |  | 8.0 | $\begin{aligned} & 15 \\ & 30 \end{aligned}$ |  | 15.0 | $\begin{gathered} 30.0 \\ 40 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| VCM CMRR $Z_{I N}$ | Common mode voltage range Common mode rejection ratio Common mode input impedance | $\begin{gathered} R_{S} \leq 10 \mathrm{k} \Omega, T_{A}=25^{\circ} \mathrm{C}, f=100 \mathrm{~Hz} \\ f=20 \mathrm{~Hz} \end{gathered}$ | $\begin{gathered} \pm 12 \\ 80 \end{gathered}$ | $\begin{gathered} \pm 13 \\ 110 \\ \\ 250 \end{gathered}$ |  | $\begin{gathered} \pm 11 \\ 70 \end{gathered}$ | $\begin{array}{r}  \pm 12 \\ 110 \\ \\ 250 \end{array}$ |  | V <br> dB <br> $M \Omega$ |
| Vout | Output voltage swing | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ | $\pm 12$ | $\pm 13$ |  | $\pm 11$ | $\pm 12$ |  | V |
| IcC | Supply current |  |  | 1.0 | 1.5 |  | 1.3 | 3.0 | mA |
| PD | DC quiescent power dissipation $\left(\mathrm{V}_{\mathrm{O}}=0\right)$ |  |  | 30 | 45 |  | 40 | 90 | mW |
| PSRR | Supply voltage rejection ratio | R S $\leq 10 \mathrm{k} \Omega$ |  | 50 | 100 |  | 75 | 200 | $\mu \mathrm{V} / \mathrm{V}$ |
|  | Large signal voltage gain | $R_{L} \leq 2 \mathrm{k} \Omega, \text { V OUT }= \pm 10 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Over temperature | $\begin{gathered} 100 \\ 40 \end{gathered}$ | 200 |  | $\begin{aligned} & 70 \\ & 40 \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{S}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | MC1556 |  |  | MC1456 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \mathrm{c}_{\mathrm{p}} \\ & \mathrm{r}_{\mathrm{p}} \\ & \mathrm{e}_{\mathrm{n}} \end{aligned}$ | Differential input impedance Parallel input capacitance Parallel input resistance Equivalent input noise voltage |  | Open loop $\mathrm{f}=20 \mathrm{~Hz}$ $\begin{gathered} A_{V}=100, R_{s}=10 \mathrm{k} \Omega, f=1.0 \mathrm{kHz} \\ B W=1.0 \mathrm{~Hz} \end{gathered}$ |  | $\begin{gathered} 6.0 \\ 5 \\ 45 \end{gathered}$ |  |  | $\begin{gathered} 6.0 \\ 3 \\ 45 \end{gathered}$ |  | pF <br> $\mathrm{M} \Omega$ $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| $\mathrm{BW}_{\mathrm{p}}$ <br> $S_{R}$ | Power bandwidth <br> Phase margin (open loop, unity gain) <br> Gain margin <br> Slew rate (unity gain) | $\begin{gathered} A_{V}=1, R_{L}=2 k \Omega, T H D \leq 5 \% \\ V_{\text {OUT }}= \pm 10 V \end{gathered}$ |  | $\begin{aligned} & 40 \\ & 70 \\ & \\ & 18 \\ & 2.5 \end{aligned}$ |  |  | $\begin{aligned} & 40 \\ & 70 \\ & \\ & 18 \\ & 2.5 \end{aligned}$ |  | $\begin{gathered} \mathrm{kHz} \\ \text { degrees } \\ \mathrm{dB} \\ \mathrm{~V} / \mu \mathrm{sec} \\ \hline \end{gathered}$ |
| $\begin{aligned} & \text { ZOUT } \\ & \text { BW } \end{aligned}$ | Output impedance Unity gain crossover frequency (open loop) | $\mathrm{f}=20 \mathrm{~Hz}$ |  | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | 2.0 |  | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | 2.5 | $\begin{gathered} \mathrm{k} \Omega \\ \mathrm{MHz} \end{gathered}$ |

TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The $\mu A 741$ is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The $\mu \mathrm{A} 741$ is short-circuit protected and allows for nulling of offset voltage.
The MC1558/MC1458/SA. 1458 consist of a pair of 741 operational amplifiers on a single chip.

## FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range
- No latch-up
- 1558/1458 are 2 "op amps" in space of one 741 package
- MC1558 Mil std 883A,B,C available
- $\mu A 741$ Mil std 883A,B,C available

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Supply voltage |  |  |
| SA741C, $\mu A 741 \mathrm{C}$, | $\pm 18$ | V |
| MC1458, SA1458 | $\pm 22$ | V |
| $\mu A 741$, MC1558 | 600 | mW |
| Internal power dissipation, $\mathrm{N}-14$ | 500 | mW |
| N package | 800 | mW |
| T package 1 | 1000 | V |
| F package | $\pm 30$ | V |
| Differential input voltage | $\pm 15$ |  |
| Input voltage2 | Continuous | ${ }^{\circ} \mathrm{C}$ |
| Output short-circuit duration | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mu A 741 C$, MC1458 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SA741C, SA1458 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mu A 741$, MC1558 | 300 |  |
| Storage temperature range |  |  |
| Lead temperature (soldering 60sec) |  |  |

NOTES

1. Ratings based on thermal resistances, junction to ambient, of $208^{\circ} \mathrm{C} / \mathrm{W}, 240^{\circ} \mathrm{C} / \mathrm{W}$ $150^{\circ} \mathrm{C} / \mathrm{W}, 110^{\circ} \mathrm{C} / \mathrm{W}$ for $\mathrm{N}-14, \mathrm{~N}, \mathrm{~T}$ and F packages respectively, and a maximum junction temperature of $150^{\circ} \mathrm{C}$.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voitage.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | $\mu$ A741 |  |  | $\mu$ A741C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}}=10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}}=10 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ |  | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ |  | 2.0 | $\begin{aligned} & 6.0 \\ & 7.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| los | Offset current | Over temp. $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 20 \\ & 7.0 \\ & 20 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \\ & 500 \end{aligned}$ |  | 20 | $\begin{aligned} & 200 \\ & 300 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IBIAS | Input bias current | Over temp. $\begin{gathered} \mathrm{T}_{A}=+125^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{gathered} 80 \\ 30 \\ 300 \end{gathered}$ | $\begin{gathered} 500 \\ 500 \\ 1500 \end{gathered}$ |  | 80 | $\begin{aligned} & 500 \\ & 800 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Vout | Output voltage swing | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} R_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | $\begin{aligned} & 20 \\ & 15 \end{aligned}$ | 200 |  | $\begin{aligned} & \hline \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Offset voltage adjustment range |  |  | $\pm 30$ |  |  | $\pm 30$ |  | mV |
| PSRR | Supply voltage rejection ratio | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ |  | 10 | 150 |  | 10 | 150 | $\begin{aligned} & \mu \mathrm{V} / \mathrm{V} \\ & \mu \mathrm{~V} / \mathrm{V} \end{aligned}$ |
| CMRR | Common mode rejection ratio | Over temp. | 70 | 90 |  |  |  |  | $\mathrm{dB}$ |
| Icc | Supply current | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 1.4 \\ & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.8 \\ & 2.5 \\ & 3.3 \end{aligned}$ |  | 1.4 | 2.8 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & V_{I N} \\ & R_{I N} \end{aligned}$ | Input voltage range Input resistance | ( $\mu$ A741, over temp.) | $\begin{gathered} \pm 12 \\ 0.3 \end{gathered}$ | $\begin{gathered} \pm 13 \\ 2.0 \end{gathered}$ |  | $\begin{gathered} \pm 12 \\ 0.3 \end{gathered}$ | $\begin{gathered} \pm 13 \\ 2.0 \end{gathered}$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{M} \Omega \end{gathered}$ |
| $\mathrm{Pd}_{\text {d }}$ | Power consumption | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 50 \\ & 45 \\ & 45 \end{aligned}$ | $\begin{gathered} 85 \\ 75 \\ 100 \end{gathered}$ |  | 50 | 85 | $\begin{aligned} & \mathrm{mW} \\ & \mathrm{~mW} \\ & \mathrm{~mW} \end{aligned}$ |
| Rout Isc | Output resistance <br> Output short-circuit current |  |  | $\begin{aligned} & 75 \\ & 25 \end{aligned}$ |  |  | $\begin{aligned} & 75 \\ & 25 \end{aligned}$ |  | $\begin{gathered} \Omega \\ \mathrm{mA} \end{gathered}$ |

## 

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA741C |  |  | MC1558 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}}=10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}}=10 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ |  | 2.0 | $\begin{aligned} & 6.0 \\ & 7.5 \end{aligned}$ |  | 1.0 | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| los | Offset current | Over temp. |  | 20 | $\begin{aligned} & 200 \\ & 500 \\ & \hline \end{aligned}$ |  | 20 | $\begin{aligned} & 200 \\ & 500 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IBIAS | Input bias current | Over temp. |  | 80 | $\begin{gathered} 500 \\ 1500 \\ \hline \end{gathered}$ |  | 80 | $\begin{gathered} 500 \\ 1500 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Vout | Output voltage swing | $\begin{gathered} R_{L}=10 \mathrm{k} \Omega \\ R_{L}=2 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 20 \\ & 15 \end{aligned}$ | 200 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Offset voltage adjustment range |  |  | $\pm 30$ |  |  | $\pm 30$ |  | mV |
| PSRR | Supply voltage rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ |  | 10 | 150 |  | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| CMRR | Common mode rejection ratio |  |  |  |  |  | 70 | 90 | dB |
| ICC | Supply current |  |  | 1.4 | 2.8 |  | 2.3 | 5.6 | mA |
| $\begin{aligned} & \mathrm{V}_{\mathrm{IN}} \\ & \mathrm{R}_{\mathrm{IN}} \end{aligned}$ | Input voltage range Input resistance | ( $\mu$ A741, over temp.) | $\begin{gathered} \pm 12 \\ 0.3 \end{gathered}$ | $\begin{gathered} \pm 13 \\ 2.0 \end{gathered}$ |  | $\pm 12$ | $\pm 13$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{M} \Omega \end{gathered}$ |
| $\mathrm{P}_{\mathrm{d}}$ | Power consumption |  |  | 50 | 85 |  | 70 | 150 | mW |
| Rout Isc | Channel separation <br> Output resistance <br> Output short-circuit current |  |  | $\begin{aligned} & 75 \\ & 25 \end{aligned}$ |  |  | $\begin{aligned} & 120 \\ & 25 \end{aligned}$ |  | $\begin{gathered} \mathrm{dB} \\ \Omega \\ \mathrm{~mA} \end{gathered}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | MC1458 |  |  | SA1458 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}}=10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}}=10 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ |  | 2.0 | $\begin{aligned} & 6.0 \\ & 7.5 \\ & \hline \end{aligned}$ |  | 2.0 | $\begin{aligned} & 6.0 \\ & 7.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| los | Offset current | Over temp. |  | 20 | $\begin{aligned} & 200 \\ & 300 \\ & \hline \end{aligned}$ |  | 20 | $\begin{aligned} & 200 \\ & 500 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IBIAS | Input bias current | Over temp. |  | 80 | $\begin{aligned} & 500 \\ & 800 \\ & \hline \end{aligned}$ |  | 80 | $\begin{gathered} 500 \\ 1500 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Vout | Output voltage swing | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | V |
| Avol | Large signal voltage gain | $\begin{gathered} R_{L}=2 k \Omega, V_{O}= \pm 10 \mathrm{~V} \\ R_{L}=2 k \Omega, V_{O}= \pm 10 \mathrm{~V} \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 200 |  | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 200 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Offset voltage adjustment range |  |  | $\pm 30$ |  |  | $\pm 30$ |  | mV |
| PSRR | Supply voltage rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ |  | 30 | 170 |  | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| CMRR | Common mode rejection ratio |  |  | 70 | 90 |  | 70 | 90 | dB |
| Icc | Supply current |  |  | 2.3 | 5.0 |  | 2.3 | 5.6 | mA |
| Vin <br> RIN | Input voltage range Input resistance | ( $\mu \mathrm{A} 741$, over temp.) | $\pm 12$ | $\pm 13$ |  | $\pm 12$ | $\pm 13$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{M} \Omega \end{gathered}$ |
| $\mathrm{Pd}_{\mathrm{d}}$ | Power consumption |  |  | 70 | 170 |  | 70 | 170 | mW |
| Isc | Channel separation Output short-circuit current |  |  | $\begin{gathered} 120 \\ 25 \end{gathered}$ |  |  | $\begin{gathered} 120 \\ 25 \end{gathered}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~mA} \end{aligned}$ |

MC1458/1558/SA1458-F,N,T
AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{S}= \pm 15 \mathrm{~V}$, unless otherwise specified.

| PARAMETER | TEST CONDITIONS | $\mu A 741, \mu A 741$ C, SA741C |  |  | MC1558, MC1458, SA1458 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Parallel input resistance Parallel input capacitance | Open loop, $f=20 \mathrm{~Hz}$ Open loop, $f=20 \mathrm{~Hz}$ |  | 1.4 |  | 0.3 |  |  | $\mathrm{M} \Omega$ pF |
| Common mode input impedance | $\mathrm{f}=20 \mathrm{~Hz}$ |  |  |  |  | 200 |  | $\mathrm{M} \Omega$ |
| Equivalent input noise voltage | $\begin{aligned} A_{V}=100, R_{S} & =10 \mathrm{k} \Omega, B_{W}=1.0 \mathrm{kHz} \\ f & =1.0 \mathrm{kHz} \end{aligned}$ |  |  |  |  | 45 |  | $n \mathrm{~V} \sqrt{\mathrm{~Hz}}$ |
| Power bandwidth | $\begin{gathered} A_{V}=1, R_{L}=2.0 \mathrm{k} \Omega, T H D \leq 5 \% \\ V_{\text {OUT }}=20 \mathrm{Vp}-\mathrm{p} \end{gathered}$ |  |  |  |  | 14 |  | kHz |
| Phase margin Gain margin |  |  |  |  |  | 65 11 |  | degrees dB |
| Unity gain crossover frequency | Open loop |  | 1.0 |  |  | 1.0 |  | MHz |
| Transient response unity gain Rise time | $V_{I N}=20 \mathrm{mV}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}} \leq 100 \mathrm{pf}$ |  | 0.3 |  |  | 0.3 | * | $\mu \mathrm{S}$ |
| Overshoot |  |  | 5.0 |  |  | 5.0 |  | \% |
| Slew rate | $\mathrm{C} \leq 100 \mathrm{pf}, \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k}, \mathrm{V}_{\mathrm{IN}}= \pm 10 \mathrm{~V}$ |  | 0.5 |  |  | 0.8 |  | $\mathrm{V} / \mu \mathrm{s}$ |

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

## INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF
AMBIENT TEMPERATURE


BROADBAND NOISE FOR VARIOUS BANDWIDTHS


POWER CONSUMPTION
AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY


POWER BANDWIDTH (Large Signal Swing vs Frequency)


## DESCRIPTION

The 515 is a general purpose high-gain amplifier with differential input and output. It is fabricated within a monolithic silicon substrate by planar and epitaxial techniques. A pair of compensation points is provided to allow frequency compensation for stable closed loop operation.
This device is not internally referenced to ground and with proper input bias may be operated from a single power supply.

## FEATURES

- Differential voltage gain (open loop) $=$ 4,500
- Input offset voltage $=0.5 \mathrm{mV}$
- Input offset voltage stability $=5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- Input common mode range $=1.5 \mathrm{~V},-1.0 \mathrm{~V}$
- Common mode rejection ratio $=100 \mathrm{~dB}$
- Bandwidth (open loop) $=1.0 \mathrm{MHz}$
- Mil std 883A,B,C available


## EQUIVALENT SCHEMATIC



NOTE
All resistors values are typical and in ohms. Component values are typical.

PIN CONFIGURATION


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Voltage |  |  |
| Applied (V+ to V -) | 12 | V |
| Differential input $\left(\mathrm{V}_{5}\right.$ to $\left.\mathrm{V}_{7}\right)$ | $\pm 5.0$ | V |
| Current | $\pm 2.0$ | mA |
| Input ( $\left.I_{5}, I_{7}\right)$ | $\pm 30$ | mA |
| Output ( $\left.\mathrm{I}_{2}, \mathrm{I}_{10}\right)$ | ${ }^{\circ} \mathrm{C}$ |  |
| Temperature range | 0 to +75 |  |
| Operating | -65 to +150 |  |
| Storage | 150 |  |
| Junction |  |  |

Maximum ratings are limiting values above which serviceability may be impaired.
Pin numbers refer to K package.

DC ELECTRICAL CHARACTERISTICS
$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{7}=0 \mathrm{~V}, \mathrm{~V}_{1}=3.0 \mathrm{~V}$ unless otherwise specified. $1,2,3,4,5,6,7,8,9,10,11$

| PARAMETER | TEST CONDITIONS | SE515 ( $\left.\mathbf{V}_{6}=+4 \mathrm{~V}\right)$ |  |  | SE515 ( $\mathbf{V}_{6}=+6 \mathrm{~V}$ ) |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Open loop voltage gain2 | $\mathrm{T}_{\mathrm{A}}=$ high temp. |  | $\begin{array}{r} 2500 \\ 1800 \\ \hline \end{array}$ |  | 3500 | $\begin{aligned} & 4500 \\ & 3000 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} / \mathrm{V} \\ & \mathrm{~V} / \mathrm{V} \end{aligned}$ |
| Input offset voltage ${ }^{1}$ | $\begin{aligned} T_{A} & =\text { low temp. } \\ T_{A} & =\text { high temp. } . \end{aligned}$ |  | $\begin{aligned} & .5 \\ & .5 \\ & .5 \end{aligned}$ |  | - | $\begin{aligned} & 0.5 \\ & 0.5 \\ & 0.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 3.0 \\ & 2.0 \\ & 3.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Input bias current 1 | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=\text { low temp. } \\ @+25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 18 \\ & 12 \end{aligned}$ |  |  | $\begin{aligned} & 25 \\ & 16 \end{aligned}$ | $\begin{aligned} & 40 \\ & 24 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Differential input resistance ${ }^{10}$ | $\mathrm{T}_{\mathrm{A}}=$ low temp. |  | $\begin{aligned} & 2 \\ & 4 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 3.2 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{k} \Omega \\ & \mathrm{k} \Omega \\ & \hline \end{aligned}$ |
| Input common mode range |  |  | $\pm 1.0$ |  |  | +1.5 -1.0 |  | V |
| Balanced output. DC level | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=\text { low temp. } \\ @+25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=\text { high temp. } \end{gathered}$ |  | $\begin{gathered} \hline-0.1 \\ +0.3 \\ +.6 \\ \hline \end{gathered}$ |  |  | $\begin{aligned} & +1.2 \\ & +1.6 \\ & +1.9 \end{aligned}$ | 1.8 | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Output voltage swing ${ }^{3}$ | Over temp. |  | 4.7 |  | 5.7 | 6.3 |  | V |
| High output level | $\begin{gathered} V_{5}=10 \mathrm{mV}, T_{A}=\text { low temp. } \\ V_{5}=10 \mathrm{mV} \\ V_{5}=10 \mathrm{mV}, T_{A}=\text { high temp. } \end{gathered}$ |  | $\begin{aligned} & +2.3 \\ & +2.6 \\ & +3.0 \end{aligned}$ |  | $\begin{aligned} & +4.0 \\ & +4.3 \\ & +4.7 \end{aligned}$ | $\begin{aligned} & \hline+4.3 \\ & +4.6 \\ & +5.0 \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Low output level | $\begin{gathered} V_{5}=10 \mathrm{mV}, T_{A}=\text { low temp. } \\ V_{5}=10 \mathrm{mV} \\ V_{5}=10 \mathrm{mV}, T_{A}=\text { high temp. } \end{gathered}$ |  | $\begin{aligned} & -2.4 \\ & -2.1 \\ & -1.7 \end{aligned}$ |  | $\begin{aligned} & \hline-1.7 \\ & -1.4 \\ & -1.0 \end{aligned}$ | $\begin{aligned} & \hline-2.0 \\ & -1.7 \\ & -1.3 \end{aligned}$ |  | $\begin{aligned} & \hline \text { V } \\ & \text { v } \\ & \text { v } \end{aligned}$ |
| Output resistance ${ }^{1}$ |  |  | 100 |  |  | 100 |  | $\Omega$ |
| Common mode rejection ratio |  |  | 100 |  |  | 100 |  | dB |
| Power supply current ${ }^{1}$ | $\begin{aligned} & T_{A}=\text { low temp } . \\ & T_{A}=\text { high temp } . \end{aligned}$ |  | 3.5 |  |  | 5.5 | $\begin{aligned} & 7.0 \\ & 7.0 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{7}=0 \mathrm{~V}, \mathrm{~V}_{1}=3.0 \mathrm{~V}$ unless otherwise specified. $1,2,3,4,5,6,7,8,9,10,11$

| PARAMETER | TEST CONDITIONS | NE515 ( $\left.\mathbf{V}_{6}=+4 \mathrm{~V}\right)$ |  |  | NE515 ( $\left.\mathrm{V}_{6}=+6 \mathrm{~V}\right)$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Open loop voltage gain² | $\mathrm{T}_{\mathrm{A}}=$ high temp . |  | $\begin{aligned} & \hline 1800 \\ & 1350 \end{aligned}$ |  | 2500 | $\begin{aligned} & 3200 \\ & 2200 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} / \mathrm{V} \\ & \mathrm{~V} / \mathrm{V} \end{aligned}$ |
| Input offset voltage ${ }^{1}$ | $\begin{aligned} \mathrm{T}_{\mathrm{A}} & =\text { low temp } . \\ \mathrm{T}_{\mathrm{A}} & =\text { high temp. } . \end{aligned}$ |  | $\begin{aligned} & \hline 0.5 \\ & 0.5 \\ & 0.5 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & \hline 0.5 \\ & 0.5 \\ & 0.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.0 \\ & 3.0 \\ & 4.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Input bias current ${ }^{\text {1 }}$ | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=\text { low temp. } \\ @+25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 18 \\ & 15 \end{aligned}$ |  |  | $\begin{aligned} & 25 \\ & 20 \end{aligned}$ | $\begin{aligned} & 40 \\ & 31 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Differential input resistance ${ }^{10}$ | $\mathrm{T}_{\mathrm{A}}=$ low temp. |  | $\begin{aligned} & \hline 3.2 \\ & 3.5 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.4 \\ & 1.7 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.3 \\ & 2.6 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \\ & \hline \end{aligned}$ |
| Input common mode range |  |  | $\pm 1.0$ |  |  | +1.5 -1.0 |  | V |
| Balanced output DC level | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=\text { low temp. } \\ \text { @ }+25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=\text { high temp. } . \\ \hline \end{gathered}$ |  | $\begin{array}{r} -0.1 \\ +0.3 \\ +0.6 \\ \hline \end{array}$ |  |  | $\begin{array}{r} +1.2 \\ +1.6 \\ +1.9 \\ \hline \end{array}$ | +1.8 | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Output voltage swing ${ }^{3}$ | Over temp. |  | 4.5 |  | 5.3 | 6.1 |  | V |
| High output level | $\begin{gathered} \mathrm{V}_{5}=10 \mathrm{mV}, \mathrm{~T}_{\mathrm{A}}=\text { low temp. } \\ \mathrm{V}_{5}=10 \mathrm{mV} \\ \mathrm{~V}_{5}=10 \mathrm{mV}, \mathrm{~T}_{\mathrm{A}}=\text { high temp. } \end{gathered}$ |  | $\begin{aligned} & +2.3 \\ & +2.5 \\ & +2.8 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & +3.9 \\ & +4.1 \\ & +4.3 \\ & \hline \end{aligned}$ | $\begin{array}{r} +4.3 \\ +4.5 \\ +4.8 \\ \hline \end{array}$ |  | $\begin{aligned} & \hline v \\ & v \\ & v \end{aligned}$ |
| Low output level | $\begin{gathered} \mathrm{V}_{5}=10 \mathrm{mV}, \mathrm{~T}_{\mathrm{A}}=\text { low temp. } \\ \mathrm{V}_{5}=10 \mathrm{mV} \\ \mathrm{~V}_{5}=10 \mathrm{mV}, T_{A}=\text { high temp. } \end{gathered}$ |  | $\begin{aligned} & -2.2 \\ & -2.0 \\ & -1.7 \end{aligned}$ |  | $\begin{aligned} & \hline-1.4 \\ & -1.2 \\ & -1.0 \end{aligned}$ | $\begin{aligned} & \hline-1.8 \\ & -1.6 \\ & -1.3 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Output resistance ${ }^{1}$ |  |  | 100 |  |  | 100 |  | $\Omega$ |
| Common mode rejection ratio |  |  | 100 |  |  | 100 |  | dB |
| Power supply current ${ }^{1}$ | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=\text { low temp } . \\ & \mathrm{T}_{\mathrm{A}}=\text { high temp. } . \end{aligned}$ |  | 3.5 |  |  | 5.5 | $\begin{aligned} & 7.0 \\ & 7.0 \\ & 7.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{7}=0 \mathrm{~V}, \mathrm{~V}_{1}=3.0 \mathrm{~V}$ unless otherwise specified. $1,2,3,4,5,6,7,8,9,10,11$

| PARAMETER | TEST CONDITIONS | SE515 $\left(\mathbf{V}_{\mathbf{6}}=+\mathbf{4 V}\right)$ |  |  | SE515 $\left(\mathbf{V}_{\mathbf{6}}=+\mathbf{6 V}\right)$ |  | UNIT |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min |  | Max |
|  |  |  |  |  |  |  |  |
| Open loop voltage gain | $\mathrm{f}=800 \mathrm{kHz}$ |  | 2000 |  | 2500 | 3500 |  | $\mu \mathrm{~V} / \mathrm{V}$ |

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{7}=0 \mathrm{~V}, \mathrm{~V}_{1}=3.0 \mathrm{~V}$ unless otherwise
specified. 1,2,3,4,5,6,7,8,9,10,11

| PARAMETER | TEST CONDITIONS | NE515 ( $\left.\mathbf{V}_{6}=+4 \mathrm{~V}\right)$ |  |  | NE515 ( $\left.\mathrm{V}_{6}=+6 \mathrm{~V}\right)$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Open loop voltage gain | $\mathrm{f}=800 \mathrm{kHz}$ |  | 1500 |  | 1700 | 2500 |  | $\mu \mathrm{V} / \mathrm{V}$ |

NOTES

1. Adjust $\mathrm{V}_{5}$ to obtain $\mathrm{V}_{2}=\mathrm{V}_{10}$.
2. Output voltage swing $=1.3 \mathrm{~V}$ peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers for K Package.
5. All measurements are referenced to power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins 5 and 7 .

## Acceptance Test Sub-Group references apply to minimum and maximum limits only

8. The SE515k has Pins 1,3 and 9 connected to the case.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test SubGroup. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.
11. Operating temperature range:

SE515 $-55^{\circ} \mathrm{C}$ TA $125^{\circ} \mathrm{C}$
NE515 $0^{\circ} \mathrm{C}$ TA $75^{\circ} \mathrm{C}$

## DESCRIPTION

The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

## FEATURES

- $35 \mathrm{~V} / \mu \mathrm{sec}$ slew rate at unity gain
- Pin for pin replacement for $\mu \mathrm{A} 709, \mu \mathrm{~A} 748$ or LM101
- Compensated with a single capacitor
- Same low drift offset null circuitry as $\mu$ A741
- Small signal bandwidth $\mathbf{1 M H z}$
- Large signal bandwidth 500 KHz
- True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.

PIN CONFIGURATIONS


## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | $\pm 22$ | V |
| Internal power dissipation1 | 300 | mW |
| Differential input voltage <br> Common mode input voltage2 <br> Voltage between offset null <br> and V- | $\pm 15$ | V |
| Operating temperature range <br> NE531 <br> SE531 <br> Storage temperature range <br> Lead temperature <br> (soldering, 60 sec) <br> Output short circuit duration 3 | $\pm 0.5$ | V |

NOTES

1. Rating applies for case temperature to $125^{\circ} \mathrm{C}$, derate linearly at $6.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for ambient temperatures above $+75^{\circ} \mathrm{C}$.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to $+125^{\circ} \mathrm{C}$ case temperature or to $+75^{\circ} \mathrm{C}$ ambient temperature.

DC ELECTRICAL CHARACTERISTICS
$V_{S}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE531 |  |  | NE531 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{aligned} & \mathrm{R}_{S} \leq 10 \mathrm{k} \Omega, \mathrm{~T}_{A}=25^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \text { over temp } \end{aligned}$ |  | 2.0 | $\begin{aligned} & 5.0 \\ & 6.0 \\ & \hline \end{aligned}$ |  | 2.0 | $\begin{aligned} & 6.0 \\ & 7.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Ios | Offset current | $\begin{aligned} T_{A} & =25^{\circ} \mathrm{C} \\ T_{A} & =H I G H \\ T_{A} & =L O W \end{aligned}$ |  | 30 | $\begin{aligned} & 200 \\ & 200 \\ & 500 \end{aligned}$ |  | 50 | $\begin{aligned} & 200 \\ & 200 \\ & 300 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IBIAS | Input current | $\begin{aligned} & T_{A}=25^{\circ} \mathrm{C} \\ & T_{A}=H I G H \\ & T_{A}=L O W \end{aligned}$ |  | 300 | $\begin{gathered} 500 \\ 500 \\ 1500 \end{gathered}$ |  | 400 | $\begin{aligned} & 1500 \\ & 1500 \\ & 2000 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| VCM CMRR | Common mode voltage range Common mode rejection ratio | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \text { Over temp } \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \end{gathered}$ | $\begin{array}{r}  \pm 10 \\ 70 \end{array}$ | 90 |  | $\begin{gathered} \pm 10 \\ 70 \end{gathered}$ | 100 |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~dB} \\ \mathrm{~dB} \end{gathered}$ |
| RIN | Input resistance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 20 |  |  | 20 |  | $\mathrm{M} \Omega$ |
| Vout | Output voltage swing | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega$, over temp | $\pm 10$ | $\pm 13$ |  | $\pm 10$ | $\pm 13$ |  | V |
| Icc $P_{D}$ | Supply current <br> Power consumption | $\begin{gathered} \mathrm{T}_{A}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{MAX}} \\ \mathrm{~T}_{A}=25^{\circ} \mathrm{C} \\ \hline \end{gathered}$ |  |  | $\begin{aligned} & \hline 7.0 \\ & 5.5 \\ & 210 \\ & \hline \end{aligned}$ |  |  | $\begin{gathered} 10 \\ 10 \\ 300 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mW} \end{aligned}$ |
| PSRR | Power supply rejection ratio | $\begin{aligned} & R_{S} \leq 10 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \text { over temp} \end{aligned}$ |  | 10 | 150 |  | 10 | 150 | $\begin{aligned} & \mu \mathrm{V} / \mathrm{V} \\ & \mu \mathrm{~V} / \mathrm{V} \end{aligned}$ |
| Rout | Output resistance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 75 |  |  | 75 |  | $\Omega$ |
| Avol | Large signal voltage gain | $\begin{aligned} & \mathrm{T}_{A}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {OUT }}= \pm 10 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{OUT}}= \pm 10 \mathrm{~V}, \text { over temp. } \end{aligned}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & 20 \\ & 15 \end{aligned}$ | 60 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |

NOTE

1. Temperature range:

SE531-55 ${ }^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$
NE531 $0^{\circ} \mathrm{C} \leq T_{A} \leq 70^{\circ} \mathrm{C}$

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE531 |  |  | SE531 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Full power bandwidth |  |  | 500 |  |  | 500 |  | kHz |
| Settling time (1\%) (.01\%) | $A v=+1, \mathrm{~V}_{\text {IN }}= \pm 10 \mathrm{~V}$ |  | $\begin{aligned} & 1.5 \\ & 2.5 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 1.5 \\ & 2.5 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mu \mathrm{S} \\ & \mu \mathrm{~s} \\ & \hline \end{aligned}$ |
| Large signal overshoot Small signal overshoot | $\begin{gathered} A v=+1, V_{I N}= \pm 10 V \\ A v=+1, V_{I N}=400 \mathrm{mV} \end{gathered}$ |  | $\begin{aligned} & 2 \\ & 5 \end{aligned}$ |  |  | $\begin{aligned} & 2 \\ & 5 \end{aligned}$ |  | $\begin{aligned} & \% \\ & \% \end{aligned}$ |
| Small signal risetime | $A v=+1, V_{\text {IN }}=400 \mathrm{mV}$ |  | 300 |  |  | 300 |  | ns |
| Slew rate | $\begin{gathered} A V=100 \\ A V=10 \\ A v=1 \text { (noninverting) } \\ A v=1 \text { (inverting) } \end{gathered}$ |  | $\begin{aligned} & 35 \\ & 35 \\ & 30 \\ & 35 \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 25 \end{aligned}$ | 35 35 30 35 |  | $\mathrm{V} / \mu \mathrm{s}$ <br> $\mathrm{V} / \mu \mathrm{s}$ <br> $\mathrm{V} / \mu \mathrm{S}$ <br> $\mathrm{V} / \mu \mathrm{S}$ |

NOTE

1. All AC testing is performed in the transient response test circuit.

## TEST LOAD CIRCUITS

OFFSET NULL CIRCUIT

TRANSIENT RESPONSE CIRCUIT


TYPICAL PERFORMANCE CHARACTERISTICS $\quad\left(\mathrm{V}_{S}= \pm 15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise specified.)


TYPICAL PERFORMANCE CHARACTERISTICS

CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE


SUPPLY VOLTAGE - $\pm \mathrm{V}$

OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## TYPICAL APPLICATIONS



## TYPICAL APPLICATIONS

POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*

## RESPONSE OF 3-POLE ACTIVE BUTTERWORTH <br> MAXIMALLY FLAT FILTER


*Reference-EDN Dec. 15, 1970 Simplify 3-Pole Active Filter Design A. Paul Brokow

PRECISION RECTIFIERS
(a) HALF WAVE

(b) FULL WAVE



## DESCRIPTION

The 532 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

## FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain-(100dB)
- Wide bandwidth (unity gain)-1MHz (temperature compensated)
- Wide power supply range single supply-( 3 Vdc to 30 Vdc ) or dual supplies-( $\pm 1.5 \mathrm{Vdc}$ to $\pm 15 \mathrm{Vdc})$
- Very low supply current drain $(400 \mu \mathrm{~A})$ essentially independent of supply voltage ( $1 \mathrm{~mW} / \mathrm{op}$ amp at +5 Vdc )
- Low input biasing current-(45nA dc temperature compensated)
- Low input offset voltage-(2mVdc) and offset current-(5nA dc)
- Differential input voltage range equal to the power supply voltage
- Large output voltage-(OVdc to V+一$1.5 V d c$ swing)
- SE532 Mil std 883A,B,C available


## UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

## PIN CONFIGURATIONS



EQUIVALENT CIRCUIT


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage, V+ | 32 or $\pm 16$ | Vdc |
| Differential input voltage | 32 | Vdc |
| Input voltage | -0.3 to +32 | Vdc |
| Power dissipation | 680 | mW |
| T package | 625 | mW |
| N package | Continuous |  |
| Output short-circuit to GND | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| V+ < 15 Vdc and TA $=25^{\circ} \mathrm{C}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| NE532 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| SA532 | 300 | ${ }^{\circ} \mathrm{C}$ |
| SE532 |  |  |
| Storage temperature range |  |  |
| Lead temperature |  |  |
| (soldering, 10sec) |  |  |

## DUAL OPERATIONHL AMPIIIER SIUGE OR DUAL POUER SUPPIV OPERATION

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=+5 \mathrm{~V}$ unless otherwise specified (see Notes on following page).

| PARAMETER | TEST CONDITIONS | SE532 |  |  | NE532 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos Offset voltage ${ }^{1}$ | $\begin{gathered} R_{S} \leq 10 k \\ R_{S} \leq 10 k \Omega, \text { over temp. } \end{gathered}$ |  | $\pm 2$ | $\begin{aligned} & \pm 5 \\ & \pm 7 \end{aligned}$ |  | $\pm 2$ | $\begin{gathered} \pm 6 \\ \pm 7.5 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos Drift | $\mathrm{R}_{\mathrm{S}}=0 \Omega$, over temp. |  | 7 |  |  | 7 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Ios Offset current <br> los Offset current <br> los Drift | $\operatorname{liN}^{N}(+)$ or $l_{\mathbb{N}}(-)$ Over temp. Over temp. |  | $\begin{aligned} & \pm 3 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} \pm 30 \\ \pm 100 \end{gathered}$ |  | $\begin{aligned} & +5 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} \pm 50 \\ \pm 150 \end{gathered}$ |  |
| IBIAS Input current² | $\operatorname{liN}_{1}(+)$ or $\operatorname{liN}^{(-)}$ Over temp., $\operatorname{liN}^{(+)}$or $\operatorname{IIN}^{(-)}$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 150 \\ & 300 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 250 \\ & 500 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CM}}$ Common mode voltage range ${ }^{3}$ <br> CMRRCommon mode rejection ratio | $\begin{gathered} \mathrm{V}+=30 \mathrm{~V} \\ \text { Over temp., } \mathrm{V}+=30 \mathrm{~V} \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \hline \end{gathered}$ | $0$ $70$ | 85 | $\begin{array}{\|l} \mathrm{V}+-1.5 \\ \mathrm{~V}+-2.0 \end{array}$ | $0$ $65$ | 70 | $\begin{array}{\|c} \mathrm{V}+-1.5 \\ \mathrm{~V}+-2.0 \end{array}$ | $\begin{gathered} V \\ V \\ d B \end{gathered}$ |
| VOUT Output voltage swing ( $\mathrm{V}_{\mathrm{OH}}$ ) <br> Vout Output voltage swing ( $\mathrm{V}_{\mathrm{OL}}$ ) | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}+=30 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} \geq 10 \mathrm{k} \Omega, \mathrm{~V}+=30 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 | $\begin{gathered} V \\ V \\ \mathrm{mV} \end{gathered}$ |
| Icc Supply current | $R_{L}=\infty$ on all amplifiers, over temp |  | 0.5 | 1.2 |  | 0.5 | 1.2 | mA |
| Avol Large signal voltage Gain | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {OUT }} \pm 10 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ Over temp. | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| PSRR Supply voltage rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | 65 | 100 |  | dB |
| Amplifier-to-amplifier coupling 4 | $\mathrm{f}=1 \mathrm{kHz}$ to 20kHz (input referred) |  | -120 |  |  | -120 |  | dB |
| Output current source Output current sink $\operatorname{Isc}^{5}$ | $\begin{array}{\|l\|} \hline \mathrm{V}_{\mathrm{N}^{+}}=1 \mathrm{Vdc}, \mathrm{~V}_{I N^{-}}=0 \mathrm{Vdc}, \mathrm{~V}+=15 \mathrm{Vdc} \\ \mathrm{~V}_{\mathrm{I}}-=1 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{Vdc}, \mathrm{~V}+=15 \mathrm{Vdc} \\ \mathrm{~V}_{\mathrm{N}^{-}}=1 \mathrm{Vdc}, \mathrm{~V}_{I N}=0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{OUT}}=200 \mathrm{mVdc} \end{array}$ | $\begin{aligned} & 20 \\ & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \\ & 50 \\ & 40 \\ & \hline \end{aligned}$ | 60 | $\begin{aligned} & 20 \\ & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \\ & 50 \\ & 40 \\ & \hline \end{aligned}$ | 60 | $\begin{aligned} & \hline \mathrm{mA} \\ & \mathrm{~mA} \\ & \mu \mathrm{~A} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}+=+5 \mathrm{~V}$ unless otherwise specified (see Notes on following page).

| PARAMETER | TEST CONDITIONS | SA532 |  |  | SE532A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos Offset voltage ${ }^{1}$ | $\begin{gathered} R_{S} \leq 10 k \\ R_{S} \leq 10 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ |  | $\pm 2$ | $\begin{gathered} \pm 6 \\ \pm 7.5 \end{gathered}$ |  | 1 | $\begin{aligned} & 2 \\ & 4 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos Drift | Rs $=0 \Omega$, over temp. |  | 7 |  |  | 7 | 15 | $\mu \mathrm{V}^{\circ} \mathrm{C}$ |
| los Offset current <br> los Offset current <br> los Drift | $\operatorname{lin}^{(+)}$or $\operatorname{lin}^{(-)}$ Over temp. Over temp. |  | $\begin{aligned} & \pm 5 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} \pm 50 \\ \pm 150 \end{gathered}$ |  | $\begin{gathered} 2 \\ 10 \\ \hline \end{gathered}$ | $\begin{array}{r} 10 \\ 30 \\ 200 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline \mathrm{nA} \\ \mathrm{nA} \\ \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ \hline \end{array}$ |
| IBIAS Input current ${ }^{2}$ | $\operatorname{liN}^{(+)} \operatorname{or} \operatorname{liN}(-)$ Over temp., $\operatorname{liN}(+)$ or $\operatorname{liN}^{(-)}$ |  | $\begin{aligned} & 45 \\ & 40 \end{aligned}$ | $\begin{aligned} & 250 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ | $\begin{gathered} 50 \\ 100 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| VCM Common mode voltage range ${ }^{3}$ <br> CMRR Common mode rejection ratio | $V+=30 \mathrm{~V}$ <br> Over temp., $\mathrm{V}+=30 \mathrm{~V}$ $\mathrm{R}_{\mathrm{s}} \leq 10 \mathrm{k} \Omega$ | 0 $65$ | 70 | $\begin{aligned} & \mathrm{V}+-1.5 \\ & \mathrm{~V}+-2.0 \end{aligned}$ | $\begin{gathered} 0 \\ 0 \\ 70 \\ \hline \end{gathered}$ | 85 | $\begin{array}{\|l\|} \hline \mathrm{V}+-1.5 \\ \mathrm{~V}+-1.5 \end{array}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~dB} \end{gathered}$ |
| Vout Output voltage swing ( VOH ) <br> Vout Output voltage swing ( $\mathrm{V}_{\mathrm{OL}}$ ) | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}+=30 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} \geq 10 \mathrm{k} \Omega, \mathrm{~V}+=30 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} \leq 10 \mathrm{k} \Omega, \text { over temp. } \end{gathered}$ | $\begin{aligned} & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 28 \\ 5 \end{gathered}$ | 20 |  |  |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{mV} \end{gathered}$ |
| ICC Supply current | $R_{L}=\infty$ on all amplifiers, over temp. |  | 0.5 | 1.2 |  | 0.5 | 1.2 | mA |
| Avol Large signal voltage Gain | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {out }} \pm 10 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ \text { Over temp. } \end{gathered}$ | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 |  | $\begin{aligned} & 50 \\ & 25 \\ & \hline \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| PSRR Supply voltage rejection ratio | $\mathrm{RS} \leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | 65 | 100 |  | dB |
| Amplifier-to-amplifier coupling ${ }^{4}$ | $\mathrm{f}=1 \mathrm{kHz}$ to 20 kHz (input referred) |  | -120 |  |  | -120 |  | dB |
| Output current source Output current sink $\mathrm{ISC}^{5}$ | $\begin{array}{\|l\|} \hline \mathrm{V}_{\mathrm{N}^{+}}=1 \mathrm{Vdc}, \mathrm{~V}_{1 N^{-}}=0 \mathrm{Vdc}, \mathrm{~V}+=15 \mathrm{Vdc} \\ \mathrm{~V}_{\mathrm{N}^{-}}=1 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{Vdc}, \mathrm{~V}+=15 \mathrm{Vdc} \\ \mathrm{~V}_{\mathrm{N}^{-}}=1 \mathrm{Vdc}, \mathrm{~V}_{\mathbb{N}}=0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{OUT}}=200 \mathrm{mVdc} \end{array}$ | $\begin{aligned} & 20 \\ & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \\ & 50 \\ & 40 \end{aligned}$ | 60 | $\begin{aligned} & 20 \\ & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \\ & 50 \\ & 40 \end{aligned}$ | 60 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mu \mathrm{~A} \\ & \mathrm{~mA} \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=+5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE532A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vos Offset voltage ${ }^{1}$ | $\begin{gathered} \mathrm{R}_{\mathrm{s}} \leq 10 \mathrm{k} \\ \mathrm{Rs} \leq 10 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ |  | 2 | $\begin{aligned} & 3 \\ & 5 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos Drift | Rs $=0 \Omega$, over temp. |  | 7 | 20 | $\mu \mathrm{V}^{\circ} \mathrm{C}$ |
| Ios Offset current <br> los Offset current <br> los Drift | $\operatorname{lin}(+)$ or $\operatorname{lin}(-)$ Over temp. Over temp. |  | 5 10 | $\begin{gathered} 30 \\ 75 \\ 300 \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{nA} \\ \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ \hline \end{gathered}$ |
| IBIAS Input current2 | $\operatorname{lin}(+) \operatorname{or} \operatorname{lin}(-)$ Over temp., $\operatorname{lin}(+)$ or $\operatorname{lin}(-)$ |  | $\begin{aligned} & 45 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & 100 \\ & 200 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CM}}$ Common mode voltage range ${ }^{3}$ <br> CMRR Common mode rejection ratio | $\mathrm{V}+=30 \mathrm{~V}$ Over temp., $\mathrm{V}+=30 \mathrm{~V}$ RS $\leq 10 \mathrm{k} \Omega$ | $\begin{gathered} \hline 0 \\ 0 \\ 65 \\ \hline \end{gathered}$ | 85 | $\begin{aligned} & \mathrm{V}+-1.5 \\ & \mathrm{~V}+-1.5 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~dB} \end{gathered}$ |
| Vout Output voltage swing (VOH) <br> Vout Output voltage swing (VOL) | $\begin{gathered} R_{L} \geq 2 \mathrm{k} \Omega, \mathrm{~V}+=30 \mathrm{~V} \\ R_{L} \geq 10 \mathrm{k} \Omega, \mathrm{~V}+=30 \mathrm{~V} \\ R_{L} \leq 10 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ |  |  |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{mV} \end{gathered}$ |
| Icc Supply current | $\mathrm{R}_{\mathrm{L}}=\infty$ on all amplifiers, over temp. |  | 0.5 | 1.2 | mA |
| Avol Large signal voltage Gain | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {Out }} \pm 10 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ \text { Over temp. } \end{gathered}$ | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| PSRR Supply voltage rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ | 65 | 100 |  | dB |
| Amplifier-to-amplifier coupling ${ }^{4}$ | $\mathrm{f}=1 \mathrm{kHz}$ to 20 kHz (input referred) |  | -120 |  | dB |
|  Output current source <br> Output current sink <br> $\mathrm{ISC}^{5}$  | $\begin{aligned} & V_{I N^{+}}=1 \mathrm{Vdc}, V_{I N^{-}}=0 \mathrm{Vdc}, \mathrm{~V}+=15 \mathrm{Vdc} \\ & \mathrm{~V}_{1 N^{-}}=1 \mathrm{Vdc}, \mathrm{~V}_{1 N}=0 \mathrm{Vdc}, \mathrm{~V}+=15 \mathrm{Vdc} \\ & \mathrm{~V}_{1 N^{-}}=1 \mathrm{Vdc}, \mathrm{~V}_{1}=0 \mathrm{Vdc}, \mathrm{Vout}_{0}=200 \mathrm{mVdc} \end{aligned}$ | $\begin{aligned} & 20 \\ & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \\ & 50 \\ & 40 \\ & \hline \end{aligned}$ | 60 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mu \mathrm{~A} \\ & \mathrm{~mA} \end{aligned}$ |

NOTES

1. $V_{O} \cong 1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=0 \Omega$ with $\mathrm{V}+$ from 5 V to 30 V ; and over the full input common-mode range ( 9 V to $\mathrm{V}+-1.5 \mathrm{~V}$ ).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially contant, independent of the state of the output so no loading change exists on the input lines
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range

[^0]4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.
5. Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $\mathrm{V}+$. At values of supply voltage in excess of +15 Vdc , continuous shortcircuits can exceed the power dissipation ratings and cause eventual destruction.

DUAL OPERATIONAL AMPIIIIER SINGIE OR DUAL POWER SUPPIY OPERATION

TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The 535 and 5535 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. The 535 is a single device while the 5535 is a dual configuration. Internally compensated for unity gain, the SE535 and SE5535 feature a guaranteed unity gain slew rate of $10 \mathrm{~V} / \mu \mathrm{s}$ with 2 mV maximum offset voltage. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 741,747 and 1558 .

## FEATURES

- $15 \mathrm{~V} / \mu$ s unity gain slew rate
- Internal frequency compensation
- Low input offset voltage- $2 m \mathrm{~V}$ max
- Low input bias current 60nA max
- Short circuit protected
- Offset null capability
- Large common mode and differential voltage ranges

|  | 535 | 5535 |
| :--- | :---: | :---: |
| - Pin out | 741 | 747,1558 |
| - Configuration | Single | Dual |

- Configuration

Single Dual

PIN CONFIGURATIONS


EQUIVALENT SCHEMATIC (One Amplifier)


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SE535/ <br> SE5535 | NE535/ <br> NE5535 | UNIT |
| :--- | :---: | :---: | :---: |
| Supply voltage | $\pm 22$ | $\pm 18$ | V |
| Internal power dissipation 1 | 500 | 500 | mW |
| N Package | 800 | 800 | mW |
| K/T Package | 1000 | 1000 | mW |
| F Package | $\pm 30$ | $\pm 30$ | V |
| Differential input voltage | $\pm 15$ | $\pm 15$ | ${ }^{\circ} \mathrm{C}$ |
| Input voltage2 | -55 to +125 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -65 to +150 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | 300 |  |
| Lead temperature (solder, 60sec) | Indefinite | Indefinite |  |
| Output short circuit 3 |  |  |  |

## NOTES

1. Rating applies for thermal resistances junction to ambient of $240^{\circ} \mathrm{C} / \mathrm{W}$ and $150^{\circ} \mathrm{C} / \mathrm{W}$ for N and $\mathrm{K}, \mathrm{T}$ packages, respectively. Maximum chip temperature is $150^{\circ} \mathrm{C}$.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to $125^{\circ} \mathrm{C}$ case temperature or $75^{\circ} \mathrm{C}$ ambient temperature

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.*

| PARAMETER |  | TEST CONDITIONS | SE535/SE5535 |  |  | NE535/NE5535 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ \mathrm{RS} \leq 10 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ |  | 0.7 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ |  | 2.0 | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| $\Delta \mathrm{V}_{\text {os }}$ | Input offset voltage drift | Rs $=0 \Omega$, over temp. |  | 3.0 | 15 |  | 6.0 |  | $\mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| los | Input offset current | Over temp. |  | 5 | $\begin{aligned} & 10 \\ & 20 \\ & \hline \end{aligned}$ |  | 15 | $\begin{aligned} & 40 \\ & 80 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{nA} \\ \mu \vee \mathrm{nA} \end{gathered}$ |
| IB | Input current | Over temp. |  | 45 | $\begin{gathered} 60 \\ 100 \end{gathered}$ |  | 65 | $\begin{aligned} & 150 \\ & 200 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Vcm CMRR | Common mode voltage range Common mode rejection ratio | Rs $\leq 10 \mathrm{k} \Omega$, over temp. | $\begin{array}{\|c\|} \hline \pm 12 \\ 70 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline \pm 13 \\ 90 \\ \hline \end{array}$ |  | $\begin{array}{\|c\|} \hline \pm 12 \\ 70 \end{array}$ | $\begin{array}{\|c\|} \hline \pm 13 \\ 90 \end{array}$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~dB} \end{gathered}$ |
| PSRR | Power supply rejection | RS $\leq 10 \mathrm{k} \Omega$, over temp. |  | 30 | 150 |  | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| RIN | Input resistance |  | 3 | 10 |  | 1 | 6 |  | $\mathrm{M} \Omega$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {OUT }}= \pm 10 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \text { V OUT }= \pm 10 \mathrm{~V} \text {, over temp. } \\ \hline \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 500 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 500 |  | $\mathrm{V} / \mathrm{mV}$ $\mathrm{V} / \mathrm{mV}$ |
| Vout | Output voltage | $R_{L} \geq 2 k \Omega$, over temp. $R_{L} \geq 10 \mathrm{k} \Omega$, over temp. | $\begin{array}{\|r\|} \hline \pm 10 \\ \pm 12 \\ \hline \end{array}$ | $\begin{aligned} & \pm 13 \\ & \pm 14 \end{aligned}$ |  | $\begin{array}{\|l\|} \hline \pm 10 \\ \pm 12 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline \pm 13 \\ \pm 14 \end{array}$ |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \\ & \hline \end{aligned}$ |
| Icc | Supply current | Per amplifier Per amplifier, over temp. |  | $\begin{gathered} 1.8 \\ 2 \\ \hline \end{gathered}$ | $\begin{aligned} & 2.8 \\ & 3.3 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 1.8 \\ 2 \\ \hline \end{gathered}$ | 2.8 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| PD | Power dissipation | Per amplifier Per amplifier, over temp. |  | $\begin{aligned} & \hline 54 \\ & 60 \end{aligned}$ | $\begin{aligned} & 84 \\ & 99 \end{aligned}$ |  | $\begin{aligned} & \hline 54 \\ & 60 \end{aligned}$ | 84 | $\begin{aligned} & \mathrm{mW} \\ & \mathrm{~mW} \end{aligned}$ |
| Isc | Output short circuit current |  |  | 25 |  |  | 25 |  | mA |
| Rout | Output resistance |  |  | 100 |  |  | 100 |  | $\Omega$ |

*NOTE
Temperature range
SE types $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$
$N E$ types $0^{\circ} \mathrm{C} \leq T_{A} \leq 70^{\circ} \mathrm{C}$

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE535/SE5535 |  |  | NE535/NE5535 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Gain/bandwidth product |  |  | 1 |  |  | 1 |  | MHz |
| Transient response Small signal rise time Small signal overshoot Settling time Slew rate | To 0.1\% <br> $T_{A}=25 C, R_{L} \geq 10 k \Omega$, unity gain, non-inverting | 10 | $\begin{gathered} 0.25 \\ 6 \\ 3 \\ 15 \end{gathered}$ |  | 10 | $\begin{gathered} 0.25 \\ 6 \\ 3 \\ 15 \end{gathered}$ |  | $\begin{gathered} \mu \mathrm{S} \\ \% \\ \mu \mathrm{~S} \\ \mathrm{~V} / \mu \mathrm{S} \end{gathered}$ |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


## VOLTAGE WAVEFORMS



TEST CIRCUITS
SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE

note
Pins not shown are not connected.
All resistors values are typical and in ohms.


## DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing an FET input stage for extremely high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

## FEATURES

- 5pA input bias current
- Input and output protection
- Offset null capability
- Internally compensated
- $6 \mathbf{V} / \mu \mathrm{sec}$ slew rate
- Standard pinout
- 1MHz unity gain bandwidth


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | $\pm 22$ | V |
| Differential input voltage range | $\pm 30$ | V |
| Common mode input voltage range | $\pm \mathrm{V}_{\mathrm{s}}$ | mW |
| Power dissipation1 | 500 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -55 to +85 |  |
| SU536T | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE536T | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 |  |
| Lead temperature (solder, 60sec) | ${ }^{\circ} \mathrm{C}$ |  |
| Output short circuit duration2 |  |  |

## PIN CONFIGURATION



NOTES

1. Rating applies for case temperature to $+25^{\circ} \mathrm{C}$; derate linearly at $6.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for ambient temperatures above $75^{\circ} \mathrm{C}$.
2. Short circuit may be to ground or either supply. Rating applies to $+125^{\circ} \mathrm{C}$ case temperature or $+75^{\circ} \mathrm{C}$ ambient temperature.

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{S}= \pm 15 \mathrm{~V}$ unless otherwise specified. 1

| PARAMETER |  | TEST CONDITIONS | NE536 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vos <br> Vos | Offset voltage <br> Drift |  | $\begin{gathered} \text { Rs } \leq 10 \mathrm{k} \Omega \\ \text { Over temp., Rs } \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}}=0 \Omega \text {, over temp. } \end{gathered}$ |  | 30 30 30 | 90 | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| los | Offset current |  |  | 5 |  | pA |
| IBIAS | Input current ${ }^{2}$ |  |  | 30 | 100 | pA |
| VCM CMRR | Common mode voltage range Common mode rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{IN}}= \pm 10 \mathrm{~V}$ | $\begin{gathered} \pm 10 \\ 64 \end{gathered}$ | $\begin{gathered} \pm 11 \\ 80 \end{gathered}$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~dB} \end{gathered}$ |
| RIN | Input resistance |  |  | $10^{14}$ |  | $\Omega$ |
| Vout | Output voltage swing | $R_{L} \geq 2 k \Omega$, over temp. $R_{L} 10 \mathrm{k} \Omega$, over temp. | $\begin{aligned} & \pm 10 \\ & \pm 12 \\ & \hline \end{aligned}$ | $\begin{array}{r}  \pm 11 \\ \pm 13 \\ \hline \end{array}$ |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| ICC | Supply current | $\mathrm{V}_{\text {OUT }}=\mathrm{OV}$ |  | 6.0 | 8.0 | mA |
| PSRR | Supply voltage rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \pm 6 \leq \mathrm{V}_{\mathrm{S}} \pm 15$ |  | 100 | 300 | $\mu \mathrm{V} / \mathrm{V}$ |
| Avol | Large signal voltage gain | $\begin{gathered} V_{O}= \pm 10 \mathrm{~V}, R_{\mathrm{L}} 2 k \Omega \\ V_{O}= \pm 10 \mathrm{~V}, R_{L} \geq 2 k \Omega \text {, over temp. } \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ |  |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| Ps | Power supply range |  | $\pm 6$ | $\pm 18$ |  | V |

## NOTES

1. Operating temperature range: NE536 is $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.
2. Input current typically doubles every $10^{\circ} \mathrm{C}$.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \pm 6 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 20 \mathrm{~V}$ unless otherwise specified. ${ }^{2}$

| PARAMETER | TEST CONDITIONS | SU536 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vos Offset voltage | $\begin{gathered} \mathrm{Rs} \leq 10 \mathrm{k} \Omega \\ \mathrm{Rs} \leq 10 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ |  | $\begin{aligned} & 7.5 \\ & 7.5 \end{aligned}$ | $\begin{aligned} & 20 \\ & 30 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos Drift | RS $\leq 10 \mathrm{k} \Omega$ |  | 20 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| los Offset current |  |  | 5 |  | PA |
| IBIAS Input current1 | Over temp. |  | $\begin{gathered} \hline 5 \\ 250 \end{gathered}$ | $\begin{gathered} \hline 30 \\ 3000 \end{gathered}$ | $\begin{aligned} & \mathrm{pA} \\ & \mathrm{pA} \end{aligned}$ |
| $V_{C M}$ Common mode voltage range CMRR Common mode rejection ratio | $\begin{gathered} V_{S}= \pm 15 \mathrm{~V} \\ R_{S} \leq 10 \mathrm{k} \Omega, V_{\text {IN }}= \pm 10 \mathrm{~V} \end{gathered}$ | $\begin{gathered} \pm 10 \\ 70 \end{gathered}$ | $\begin{gathered} \pm 11 \\ 80 \end{gathered}$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~dB} \end{gathered}$ |
| RIN Input resistance |  |  | $10^{14}$ |  | $\Omega$ |
| VOUT Output voltage swing | $R_{L} \geq 2 k \Omega, V_{S}= \pm 15 \mathrm{~V}$, over temp. $R_{L} \geq 10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, over temp. | $\begin{aligned} & \pm 10 \\ & \pm 12 \\ & \hline \end{aligned}$ | $\begin{aligned} & \pm 12 \\ & \pm 13 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \\ & \hline \end{aligned}$ |
| Icc Supply current | $\mathrm{V}_{\text {Out }}=\mathrm{OV}, \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}$ |  | 4.5 | 5.5 | mA |
| PSRR Supply voltage rejection ratio | $\mathrm{Rs} \leq 10 \mathrm{k} \Omega$ |  | 50 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| Avol Large signal voltage gain | Over temp., $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega$ | 50 |  |  | $\mathrm{V} / \mathrm{mV}$ |
| Ps Power supply range |  | $\pm 6$ |  | $\pm 20$ | V |

NOTES

1. Input current typically doubles every $10^{\circ} \mathrm{C}$.
. Operating temperature range for SU 336 is $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. 1,2

| PARAMETER | TEST CONDITIONS | NE536 |  |  | SU536 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Differential capacitance |  |  | 6 |  |  | 6 |  | pF |
| Input noise voltage | $0.1 \mathrm{~Hz}-100 \mathrm{kHz}$ |  | 20 |  |  | 20 |  | $\mu \mathrm{Vrms}$ |
| Output impedance |  |  | 100 |  |  | 100 |  |  |
| Unity gain frequency Full power bandwidth | $\begin{aligned} & V_{S}= \pm 15 \mathrm{~V} \\ & V_{S}= \pm 15 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 1 \\ 100 \end{gathered}$ |  |  | $\begin{gathered} 1 \\ 100 \end{gathered}$ |  | $\begin{aligned} & \mathrm{MHz} \\ & \mathrm{KHz} \end{aligned}$ |
| Slew rate, inverter Slew rate, follower | $\begin{aligned} & V_{S}= \pm 15 \mathrm{~V}, A=-1 \mathrm{~V} \\ & V_{S}= \pm 15 \mathrm{~V}, A=+1 \mathrm{~V} \end{aligned}$ |  | 6 |  |  | 6 |  | $\begin{aligned} & \mathrm{V} / \mu \mathrm{S} \\ & \mathrm{~V} / \mu \mathrm{S} \end{aligned}$ |

## NOTES

1. Temperature range for $S U 536$ is $-55 \leq T_{A} \leq 85^{\circ} \mathrm{C}$ Temperature range for NE536 is $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$
2. $\mathrm{SU} 536- \pm 6 \mathrm{~V} \leq \mathrm{T}_{\mathrm{A}} \pm 20 \mathrm{~V}$

NE536 - $\pm 15 \mathrm{~V}$

CIRCUIT SCHEMATIC


TYPICAL PERFORMANCE CHARACTERISTICS


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY


INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


VOLTAGE FOLLOWER TRANSIENT RESPONSE


INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE


NE/SU536-T

TYPICAL PERFORMANCE
CHARACERISTICS (Cont'd)
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


TEST CIRCUITS


OFFSET NULL CIRCUIT


## DESCRIPTION

The 538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/SE5538 offer guaranteed minimum slew rates of $40 \mathrm{~V} / \mu \mathrm{s}$ or larger. Featuring 2 mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual version. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

## FEATURES

- 2 mV max input offset voltage
- 60nA max input offset current
- Short circuit protected
- Offset null capability
- Large common mode and differential voltage ranges
- $60 \mathrm{~V} / \mu \mathrm{s}$ slew rate (gain of $+5,-4 \mathrm{~min}$ )
- 6 MHz gain bandwidth product (gain +5, -4 minimum)
- Internal frequency compensation (gain of +5, -4 minimum)
- Pin out: 538 same as 741 (single) 5538 same as 747, 1458 (dual)

PIN CONFIGURATIONS


## ABSOLUTE MAXIMUM RATINGS1,2,3

| PARAMETER |  | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| V CC | Supply voltage |  |  |
|  | SE military grade | $\pm 22$ | V |
|  | NE commercial grade | $\pm 18$ | V |
| PD | Internal power dissipation | 1000 | mW |
|  | F package |  |  |
| PD | Internal power dissipation1 | 500 | mW |
|  | N package |  |  |
| PD | Internal power dissipation1 K, T package | 800 | mW |
|  | Differential input voltage | $\pm 30$ | V |
|  | Input voltage2 | $\pm 15$ | V |
|  | Operating temperature range |  |  |
|  | SE military grade | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
|  | NE commercial grade | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
|  | Output short circuit3 | indefinite |  |
|  | Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
|  | Lead temperature (solder, 60sec.) | 300 | ${ }^{\circ} \mathrm{C}$ |

## NOTES

1. Rating applies for thermal resistances of $240^{\circ} \mathrm{C} / \mathrm{W}$ and $150^{\circ} \mathrm{C} / \mathrm{W}$ junction to ambient for N and K, T packages, respectively. Maximum chip temperature is $150^{\circ} \mathrm{C}$.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to $125^{\circ} \mathrm{C}$ case temperature or $75^{\circ} \mathrm{C}$ ambient temperature.

## EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE538/SE5538 |  |  | NE538/NE5538 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $V_{\text {os }}$ $\mathrm{V}_{\mathrm{os}}$ | Input offset voltage Input offset voltage |  | $\begin{gathered} \mathrm{Rs} \leq 10 \mathrm{k} \Omega \\ \mathrm{Rs} \leq 10 \mathrm{k} \Omega \text {, over temp. } \\ \hline \end{gathered}$ |  | 0.7 | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ |  | 2.0 | $\begin{aligned} & 5.0 \\ & 6.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| $\Delta V_{\text {os }}$ | Input offset voltage drift | $\mathrm{R}_{\mathrm{S}}=0 \Omega$, over temp. |  | 3.0 | 15 |  | 6.0 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { los } \\ & \text { los } \end{aligned}$ | Input offset current Input offset current | Over temp. |  | 5 | $\begin{aligned} & 10 \\ & 20 \end{aligned}$ |  | 15 | $\begin{aligned} & 40 \\ & 80 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{IB} \\ & \mathrm{I}_{\mathrm{B}} \end{aligned}$ | Input current Input current | Over temp. |  | 45 | $\begin{gathered} 60 \\ 100 \\ \hline \end{gathered}$ |  | 65 | $\begin{aligned} & 150 \\ & 200 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $V_{\text {CM }}$ | Input common mode voltage range |  | $\pm 12$ | $\pm 13$ |  | $\pm 12$ | $\pm 13$ |  | V |
| $\mathrm{C}_{\text {MRR }}$ | Common mode rejection ratio | $\mathrm{Rs} \leq 10 \mathrm{k} \Omega$, over temp. | 70 | 90 |  | 70 | 90 |  | dB |
| PSRR | Power supply rejection | Rs $\leq 10 \mathrm{k} \Omega$, over temp. |  | 30 | 150 |  | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| RIN | Input resistance |  | 3 | 10 |  | 1 | 6 |  | $\mathrm{M} \Omega$ |
| Avol Avol | Large signal voltage gain Large signal voltage gain | $\begin{aligned} & \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \text { Vout }= \pm 10 \mathrm{~V} \\ & \text { Over temp., } \\ & \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {OuT }}= \pm 10 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| Vout Vout | Output voltage Output voltage | Over temp., $R_{L} \geq 2 k \Omega$ Over temp., $R_{L} \geq 10 \mathrm{k} \Omega$ | $\begin{aligned} & \pm 10 \\ & \pm 12 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 14 \end{aligned}$ |  | $\begin{aligned} & \pm 10 \\ & \pm 12 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 14 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{Icc} \\ & \mathrm{Icc} \\ & \hline \end{aligned}$ | Supply current Supply current | Per amplifier Over temp., per amplifier |  | $\begin{gathered} 2 \\ 2.2 \end{gathered}$ | $\begin{gathered} \hline 3 \\ 3.6 \\ \hline \end{gathered}$ |  | $\begin{gathered} 2 \\ 2.2 \end{gathered}$ | 3 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{PD} \\ & \mathrm{PD} \end{aligned}$ | Power dissipation Power dissipation | Per amplifier Over temp., per amplifier |  | $\begin{aligned} & \hline 60 \\ & 66 \end{aligned}$ | $\begin{gathered} 90 \\ 108 \end{gathered}$ |  | $\begin{aligned} & 60 \\ & 66 \end{aligned}$ | 90 | $\begin{aligned} & \mathrm{mW} \\ & \mathrm{~mW} \end{aligned}$ |
| Isc | Output short circuit current |  |  | 25 |  |  | 25 |  | mA |
| Rout | Output resistance |  |  | 100 |  |  | 100 |  | $\Omega$ |

NOTE
Temperature Range
SE Types $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$
NE Types $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE538/SE5538 |  |  | NE538/NE5538 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Gain bandwidth product (Gain +5, -4 minimum) |  |  | 6 |  |  | 6 |  | MHz |
| Transient response Small signal rise time Small signal overshoot |  |  | $\begin{gathered} 0.25 \\ 6 \end{gathered}$ |  |  | $\begin{gathered} 0.25 \\ 6 \end{gathered}$ |  | $\begin{gathered} \mu \mathrm{S} \\ \% \end{gathered}$ |
| Settling time | To 0.1\% |  | 1.2 |  |  | 1.2 |  | $\mu \mathrm{S}$ |
| Slew rate | Minimum gain $=5$ <br> Noninverting $R_{L} \geq 2 \mathrm{k} \Omega$ | 40 | 60 |  |  | 60 |  | $\mathrm{V} / \mu \mathrm{S}$ |

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TEST LOAD CIRCUITS

## SLEW RATE AND SMALL SIGNAL

 TRANSIENT RESPONSE TEST CIRCUIT

NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

TEST LOAD CIRCUITS (Cont'd)


## DESCRIPTION

The SE/NE5534 is a high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as 741 and 301A, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amp is internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the SE/NE5534A version be used which has guaranteed noise specifications.

PIN CONFIGURATIONS


## FEATURES

- Small-signal bandwidth: 10 MHz
- Output drive capability: $600 \Omega, 10 \mathrm{~V}$ (rms)
 at $V_{s}= \pm 18 \mathrm{~V}$
- Input noise voltage: $\mathbf{4 n V} / \sqrt{\mathbf{H z}}$
- DC voltage gain: 100000
- AC voltage gain: $\mathbf{6 0 0 0}$ at $\mathbf{1 0 k H z}$
- Power bandwidth: 200kHz
- Slew-rate: 13V/ $\mu \mathbf{s}$
- Large supply voltage range: $\pm 3$ to $\pm 20 \mathrm{~V}$


## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| $V_{S}$ <br> VIN <br> VDifF <br> $\mathrm{T}_{\mathrm{A}}$ | Supply voltage | $\pm 22$ | V |
|  | Input voltage | $\pm \mathrm{V}$ supply | V |
|  | Differential input voltage | $\pm .5$ | V |
|  | Operating temperature range ${ }^{1}$ |  |  |
|  | SE | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
|  | NE | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| Tstg <br> TJ <br> PD | Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
|  | Junction temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
|  | Power dissipation |  |  |
|  | 5534 T | 680 | mW |
|  | 5534 N | 500 | mW |
|  | Output short circuit duration ${ }^{2}$ | indefinite |  |
|  | Lead temperature (soldering 10 sec$)^{3}$ | 300 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6 V Maximum current should be limited to $\pm 10 \mathrm{~mA}$.
2. For operation at elevated temperature $T$ package must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$ junction to ambient, $45^{\circ} \mathrm{C} / \mathrm{W}$ junction to case. Thermal resistance of the N package is $240^{\circ} \mathrm{C} / \mathrm{W}$.
3. Output may be shorted to ground at $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified. 1,2

| PARAMETER |  | TEST CONDITIONS | SE5534/5534A |  |  | NE5534/5534A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | Over temperature |  | . 5 | $\begin{aligned} & 2 \\ & 3 \end{aligned}$ |  | . 5 | $\begin{aligned} & 4 \\ & 5 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| los | Offset current | Over temperature |  | 10 | $\begin{aligned} & 200 \\ & 500 \\ & \hline \end{aligned}$ |  | 20 | $\begin{aligned} & 300 \\ & 400 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| IB | Input current | Over temperature |  | 400 | $\begin{gathered} \hline 800 \\ 1500 \end{gathered}$ |  | 500 | $\begin{aligned} & 1500 \\ & 2000 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| Icc | Supply current | Over temperature |  | 4 | $\begin{gathered} 6.5 \\ 9 \end{gathered}$ |  | 4 | 8 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $V_{C M}$ CMRR PSRR | Common mode input range Common mode rejection ratio Power supply rejection ratio |  | $\begin{gathered} \pm 12 \\ 80 \end{gathered}$ | $\begin{gathered} \pm 13 \\ 100 \\ 10 \end{gathered}$ | 50 | $\begin{gathered} \pm 12 \\ 70 \end{gathered}$ | $\begin{gathered} \pm 13 \\ 100 \\ 10 \end{gathered}$ | 100 | $\begin{gathered} V \\ d B \\ \mu V / V \end{gathered}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 600 \Omega, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \\ \text { Over temperature } \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 |  | $\begin{aligned} & 25 \\ & 15 \\ & \hline \end{aligned}$ | 100 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| Vout | Output swing | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 600 \Omega \\ \mathrm{R}_{\mathrm{L}} \geq 600 \Omega \mathrm{~V}_{\mathrm{S}}= \pm 18 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & \pm 12 \\ & \pm 15 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 16 \end{aligned}$ |  | $\begin{aligned} & \pm 12 \\ & \pm 15 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 16 \end{aligned}$ |  | V |
| $\begin{aligned} & \text { RIN } \\ & \text { Isc } \end{aligned}$ | Input resistance Output short circuit current |  | 50 | $\begin{gathered} 100 \\ 38 \end{gathered}$ |  | 30 | $\begin{aligned} & 100 \\ & 38 \end{aligned}$ |  | $\begin{aligned} & \mathrm{K} \Omega \\ & \mathrm{~mA} \end{aligned}$ |

NOTES

1. For NE5534, NE5534A, $\mathrm{T}_{\text {MIN }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {MAX }}=70^{\circ} \mathrm{C}$
2. For SE5534, SE5534A, $T_{M I N}=-55^{\circ} \mathrm{C}, \operatorname{TMAX}=+125^{\circ} \mathrm{C}$

AC ELECTRICAL CHARACTERISTICS
$T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE5534/5534A |  |  | NE5534/5534A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Rout | Output resistance |  | $\begin{gathered} A v=30 \mathrm{~dB} \text { closed loop } \\ f=10 \mathrm{kHz}, R_{L}=600 \Omega, C_{C}=22 \mathrm{pF} \end{gathered}$ |  | 0.3 |  |  | 0.3 |  | $\Omega$ |
|  | Transient response | Voltage follower, $\mathrm{V}_{\mathrm{IN}}=50 \mathrm{mV}$ $R_{L}=600 \Omega, C_{C}=22 p F, C_{L}=100 \mathrm{pF}$ |  | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ |  |  | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & \text { ns } \\ & \% \end{aligned}$ |
| Transient response | response <br> Rise time Overshoot | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=50 \mathrm{mv}, \mathrm{R}_{\mathrm{L}}=600 \Omega \\ & \mathrm{C}_{\mathrm{C}}=47 \mathrm{pF}, \mathrm{C}_{\mathrm{L}}=500 \mathrm{pF} \end{aligned}$ |  | $\begin{aligned} & 50 \\ & 35 \end{aligned}$ |  |  | $\begin{aligned} & 50 \\ & 35 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { ns } \\ & \% \end{aligned}$ |
| AC | Gain | $\begin{gathered} f=10 \mathrm{kHz}, \mathrm{C}_{\mathrm{C}}=0 \\ \mathrm{f}=10 \mathrm{kHz}, C_{C}=22 \mathrm{pF} \\ \hline \end{gathered}$ |  | $\begin{gathered} 6 \\ 2.2 \end{gathered}$ |  |  | $\begin{gathered} 6 \\ 2.2 \end{gathered}$ |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | Gain bandwidth product | $\mathrm{C}_{\mathrm{C}}=22 \mathrm{pF}, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$ |  | 10 |  |  | 10 |  | mHz |
|  | Slew rate | $\begin{gathered} C_{C}=0 \\ C_{C}=22 p F \end{gathered}$ |  | $\begin{gathered} 13 \\ 6 \end{gathered}$ |  |  | $\begin{gathered} 13 \\ 6 \end{gathered}$ |  | $\begin{aligned} & \hline \mathrm{V} / \mu \mathrm{S} \\ & \mathrm{~V} / \mu \mathrm{S} \end{aligned}$ |
|  | Power bandwidth | $\begin{gathered} \text { VOUT }= \pm 10 \mathrm{~V}, \mathrm{C}_{\mathrm{C}}=0 \\ \text { VOUT }= \pm 10 \mathrm{~V}, \mathrm{C}_{\mathrm{C}}=22 \mathrm{pF} \\ \text { VOUT }= \pm 14 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=600 \Omega \\ \mathrm{C}_{\mathrm{C}}=22 \mathrm{pF}, \mathrm{~V}_{\mathrm{CC}}= \pm 18 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} \hline 200 \\ 95 \\ 70 \end{gathered}$ |  |  | $\begin{gathered} \hline 200 \\ 95 \\ 70 \end{gathered}$ |  | $\begin{aligned} & \mathrm{kHz} \\ & \mathrm{kHz} \\ & \mathrm{kHz} \end{aligned}$ |

ELECTRICAL CHARACTERISTICS $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE5534/NE5534 |  |  | SE5534A/NE5534A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input noise voltage | $\begin{aligned} & \mathrm{f}_{0}=30 \mathrm{~Hz} \\ & \mathrm{f}_{\mathrm{O}}=1 \mathrm{kHz} \end{aligned}$ |  | $\begin{aligned} & 7 \\ & 4 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 5.5 \\ & 3.5 \end{aligned}$ | $\begin{gathered} 7 \\ 4.5 \end{gathered}$ | $\begin{aligned} & n \mathrm{nV} / \sqrt{\mathrm{Hz}} \\ & \mathrm{nV} / \sqrt{\mathrm{Hz}} \\ & \hline \end{aligned}$ |
| Input noise current | $\begin{aligned} & \mathrm{f}_{\mathrm{o}}=30 \mathrm{~Hz} \\ & \mathrm{f}_{\mathrm{o}}=1 \mathrm{kHz} \end{aligned}$ |  | $\begin{aligned} & 2.5 \\ & 0.6 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 1.5 \\ & 0.4 \end{aligned}$ |  | $\begin{aligned} & \mathrm{pA} / \sqrt{\mathrm{Hz}} \\ & \mathrm{pA} / \sqrt{\mathrm{Hz}} \end{aligned}$ |
| Broadband noise figure | $\mathrm{f}=10 \mathrm{~Hz}-20 \mathrm{kHz}, \mathrm{RS}_{\mathrm{S}}=5 \mathrm{k} \Omega$ |  | - |  |  | 0.9 |  | dB |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS
(INPUT NOISE CURRENT DENSITY

TEST LOAD CIRCUITS


CLOSED LOOP FREQUENCY RESPONSE


## DESCRIPTION

The 709 is a high performance monolithic operational amplifier with differential inputs. High open loop gain, high input impedance, wide input common mode and output voltage ranges plus low temperature drift enable it to be used in many applications formerly satisfied only by discrete amplifiers.

## FEATURES

- Open loop voltage gain $=\mathbf{4 5 , 0 0 0}$
- Output voltage swing $= \pm 14 \mathrm{~V}$
- Input common mode range $= \pm 10 \mathrm{~V}$
- Differential input resistance $=$

SA709C 250K
$\mu A 709 \mathrm{C}$ 250K
$\mu$ A709 400K
$\mu A 709 A$ 700K

- $\mu A 709,709 A$ Mil Std 883 A,B,C available


## PIN CONFIGURATIONS



ORDER PART NO.
$\mu$ A709AF, $\mu$ A709AN-14, $\mu$ A709F, $\mu \mathrm{A} 709 \mathrm{~N}-14$, SA $709 \mathrm{CF}, \mathrm{SA} 709 \mathrm{CN}-14$, $\mu$ A709CN-14

TPACKAGE


ORDER PART NO.
ORDER PART NO.
$\mu \mathrm{A} 709 \mathrm{AT}, \mu \mathrm{A} 709 \mathrm{~T}, \mu \mathrm{~A} 709 \mathrm{CT}$


## EQUIVALENT SCHEMATIC

*NOTE
Rating applied for case temperatures to $+125^{\circ} \mathrm{C}$. Derate linearly at $5.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for ambient temperatures above $+95^{\circ} \mathrm{C}$.


DC ELECTRICAL CHARACTERISTICS $\pm 9 \mathrm{~V} \leq \mathrm{V}_{\mathrm{S}} \leq \pm 15 \mathrm{~V}(\mu \mathrm{~A} 709, \mu \mathrm{~A} 709 \mathrm{~A}) \mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V}(\mu \mathrm{~A} 709 \mathrm{C}, \mathrm{SA} 709 \mathrm{C})$ $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.*

| PARAMETER |  | TEST CONDITIONS | $\mu$ A709 |  |  | $\mu$ A709C |  |  | $\mu$ A709A |  |  | SA709C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & V_{\text {os }} \\ & V_{\text {os }} \end{aligned}$ | Offset voltage Offset voltage |  | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ <br> Over temp |  | 1.0 | $\begin{array}{\|l\|} \hline 5.0 \\ 6.0 \\ \hline \end{array}$ |  | 2.0 | $\begin{aligned} & 7.5 \\ & 10 \end{aligned}$ |  | 0.6 | $\begin{array}{\|l\|} \hline 2.0 \\ 3.0 \\ \hline \end{array}$ |  | 2.0 | $\begin{aligned} & 7.5 \\ & 10 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vos | Drift | $\begin{gathered} \mathrm{R}_{\mathrm{s}}=50 \text { over temp } \\ \mathrm{R}_{\mathrm{s}} \leq 10 \mathrm{k}+25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {max }} \\ \mathrm{R}_{\mathrm{s}} \leq 10 \mathrm{k} \mathrm{~T}_{\text {min }} \leq \mathrm{T}_{\mathrm{A}}<+25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{array}{\|l\|} \hline 3.0 \\ 6.0 \\ 6.0 \\ \hline \end{array}$ |  |  |  |  |  | 1.8 <br> 2.0 <br> 4.8 | $\begin{aligned} & 10 \\ & 15 \\ & 25 \\ & \hline \end{aligned}$ |  |  |  | $\begin{array}{l\|} \hline \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{array}$ |
| los | Offset current | $\begin{aligned} & T_{\text {max }} \\ & T_{\text {min }} \end{aligned}$ |  | $\begin{array}{\|c\|} \hline 50 \\ 20 \\ 100 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline 200 \\ 200 \\ 500 \\ \hline \end{array}$ |  | 100 | $\begin{aligned} & 500 \\ & 750 \\ & 750 \end{aligned}$ |  | 10 <br> 3.5 <br> 40 | $\begin{array}{\|l\|} \hline 50 \\ 50 \\ 250 \\ \hline \end{array}$ |  | 100 | $\begin{array}{\|l\|} \hline 500 \\ 750 \\ 750 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| IBIAS | Input current | $\begin{aligned} & T_{\text {min }} \\ & T_{\text {max }} \\ & \hline \end{aligned}$ |  | $\begin{array}{\|l\|} \hline 200 \\ 500 \end{array}$ | $\begin{array}{\|c\|} \hline 500 \\ 1500 \\ \hline \end{array}$ |  | 300 | $\begin{array}{\|l\|} \hline 1500 \\ 2000 \\ 2000 \\ \hline \end{array}$ |  | $\begin{array}{\|l\|} \hline 100 \\ 300 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline 200 \\ 600 \\ \hline \end{array}$ |  | 300 | $\begin{aligned} & 1100 \\ & 2000 \\ & 2000 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Common mode voltage range | $\begin{gathered} \mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{s}}= \pm 15 \mathrm{~V} \text { over temp } \end{gathered}$ | $\pm 8.0$ | $\pm 10$ |  | $\pm 8.0$ | $\pm 10$ |  | $\pm 8.0$ | $\pm 10$ |  | $\pm 8.0$ | $\pm 10$ |  | $\bar{v}$ v |
| CMRR | Common mode rejection ratio | $\begin{gathered} R_{s} \leq 10 \mathrm{k} \Omega \\ R_{\mathrm{x}} \leq 10 \mathrm{k} \Omega \text { over temp } \end{gathered}$ |  | 70 | 90 | 65 | 90 |  | 80 | 110 |  | 65 | 90 |  | $\overline{d B}$ $d B$ |
| RIN | Input resistance | Over temp | $\begin{array}{\|c\|} \hline 150 \\ 40 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline 400 \\ 100 \\ \hline \end{array}$ |  | $\begin{aligned} & 50 \\ & 35 \end{aligned}$ | 250 |  | $\begin{array}{\|c\|} \hline 350 \\ 85 \\ \hline \end{array}$ | $\begin{aligned} & 700 \\ & 170 \end{aligned}$ |  | $\begin{aligned} & 50 \\ & 35 \end{aligned}$ | 250 |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| Avol | Large signal voltage gain | $\begin{gathered} \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {out }}= \pm 10 \mathrm{~V} \\ R_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {out }}= \pm 10 \mathrm{~V} \text {, over temp } \end{gathered}$ | 25 | 45 | 70 | $\begin{aligned} & 15 \\ & 12 \end{aligned}$ | 45 |  | 25 |  | 70 | $\begin{aligned} & 15 \\ & 12 \end{aligned}$ | 45 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
| V OUT | Output voltage swing | $\begin{gathered} R_{L}=2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{s}}= \pm 15 \mathrm{~V} \\ R_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}= \pm 15 \mathrm{~V} \text { over temp } \\ \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}= \pm 15 \mathrm{~V} \text { over temp } \end{gathered}$ | $\pm 10$ <br> $\pm 12$ <br> $\pm 10$ <br> $\pm 12$ | $\pm 13$ <br> $\pm 14$ <br> $\pm 13$ <br> $\pm 14$ |  | $\begin{array}{\|l\|} \hline \pm 10 \\ \pm 12 \end{array}$ | $\begin{array}{\|l\|} \hline \pm 13 \\ \pm 14 \end{array}$ |  | $\begin{array}{\|l\|} \hline \pm 10 \\ \pm 12 \\ \pm 10 \\ \pm 12 \\ \hline \end{array}$ | $\begin{array}{\|}  \pm 13 \\ \pm 14 \\ \pm 13 \\ \pm 14 \end{array}$ |  | $\begin{array}{\|l\|} \hline \pm 10 \\ \pm 12 \\ \hline \end{array}$ | $\left.\begin{array}{\|l\|} \hline \pm 13 \\ \pm 14 \end{array} \right\rvert\,$ |  | V V V |
| $\mathrm{P}_{\mathrm{D}}$ | Power consumption | $\begin{aligned} & \mathrm{V}_{S}= \pm 15 \mathrm{~V} \\ & T_{A}=h i g h \\ & T_{A}=\text { low } \end{aligned}$ |  | 80 | 165 |  | 80 | 200 |  | 75 <br> 63 <br> 81 | 108 <br> 90 <br> 135 |  | 80 | 200 | $\begin{aligned} & \mathrm{mW} \\ & \mathrm{~mW} \\ & \mathrm{~mW} \\ & \hline \end{aligned}$ |
| PSRR | Supply voltage rejection ratio | $\begin{gathered} \mathrm{R}_{\mathrm{s}} \leq 10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \text { over temp } \end{gathered}$ | 25 | 150 |  |  | 25 | 200 |  | 40 | 100 |  | 25 | 200 | $\mu \mathrm{V} / \mathrm{V}$ |
| Rout | Output resistance |  |  | 150 |  |  | 150 |  |  | 150 |  |  | 150 |  | $\Omega$ |

*NOTE
Operating temperature range
$\mu \mathrm{A} 709, \mu \mathrm{~A} 709 \mathrm{~A} \quad-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$
$S A 709 \mathrm{C} \quad-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$
$\mu \mathrm{A} 709 \mathrm{C} \quad 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$

## AC ELECTRICAL CHARACTERISTICS

$\pm 9 \mathrm{~V} \leq \mathrm{V}_{\mathrm{s}} \leq \pm 15 \mathrm{~V}(\mu \mathrm{~A} 709, \mu \mathrm{~A} 709 \mathrm{~A}) \mathrm{V}_{\mathrm{s}}= \pm 15 \mathrm{~V}(\mu \mathrm{~A} 709 \mathrm{C}, \mathrm{SA} 709 \mathrm{C})$
$T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.


## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


## DESCRIPTION

The $\mu \mathrm{A} 740 \mathrm{C}$ is a special purpose high performance operational amplifier utilizing a FET input stage for high input impedance and low input current.
The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

## FEATURES

- 0.1nA input bias current
- Input and output protection
- Offset null capability
- Internally compensated
- $6 \mathrm{~V} / \mu \mathrm{s}$ slew rate
- Standard pinout
- No latch-up

PIN CONFIGURATION
T PACKAGE


| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | $\pm 22$ | V |
| Differential input voltage range | $\pm 30$ | V |
| Common mode input voltage range | $\pm \mathrm{VS}_{\mathrm{s}}$ |  |
| Power dissipation1 | 500 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | 300 |
| Lead temperature (solder, 60sec) | ${ }^{\circ} \mathrm{C}$ |  |
| Output short circuit duration2 | indefinite |  |

NOTES

1. Rating applies to case temperature to $+25^{\circ} \mathrm{C}$. Derate linearly at $6.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for ambient temperatures above $75^{\circ} \mathrm{C}$.
2. Short circuit may be to ground or either supply. Rating applies to $+125^{\circ} \mathrm{C}$ case temperature or $+75^{\circ} \mathrm{C}$ ambient temperature.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{S}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | $\mu \mathrm{A} 740 \mathrm{C}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 100 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{S}} \leq 100 \mathrm{k} \Omega \text {, over temp. } \end{gathered}$ |  | $\begin{aligned} & 30 \\ & 30 \\ & \hline \end{aligned}$ | 110 | $\begin{aligned} & m V \\ & m V \end{aligned}$ |
| los | Offset current | Over temp. |  | $\begin{aligned} & \hline 60 \\ & 60 \\ & \hline \end{aligned}$ | 300 | $\begin{aligned} & \mathrm{pA} \\ & \mathrm{pA} \end{aligned}$ |
| IBIAS | Input current ${ }^{1}$ | Over temp. |  | $\begin{aligned} & 0.1 \\ & 1.1 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| VCM CMRR | Common mode voltage range ${ }^{2}$ Common mode rejection ratio | Over temp. Over temp. | $\begin{gathered} \pm 10 \\ 55 \end{gathered}$ | $\begin{gathered} \pm 12 \\ 80 \end{gathered}$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~dB} \end{gathered}$ |
| RIN | Input resistance |  |  | 1,000,000 |  | $\mathrm{M} \Omega$ |
| Vout | Output voltage swing | Over temp., $R_{L} \geq 2 k \Omega$ Over temp., $R_{L} \geq 10 \mathrm{k} \Omega$ | $\begin{aligned} & \pm 10 \\ & \pm 12 \\ & \hline \end{aligned}$ | $\begin{array}{r}  \pm 13 \\ \pm 14 \\ \hline \end{array}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| $\begin{aligned} & \text { ICC } \\ & \mathrm{Pd} \end{aligned}$ | Supply current Power consumption |  |  | $\begin{aligned} & 4.2 \\ & 126 \\ & \hline \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 240 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mW} \end{aligned}$ |
| PSRR | Supply voltage rejection ratio | $\mathrm{RS} \leq 10 \mathrm{k} \Omega$, over temp. |  | 70 | 500 | $\mu \mathrm{V} / \mathrm{V}$ |
|  | Output resistance |  |  | 75 |  | $\Omega$ |
| Avol | Large signal voltage gain | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \mathrm{~V}_{\text {OUT }}= \pm 10 \mathrm{~V},$ <br> $R_{L} \geq 2 k \Omega$, over temp. | 20 | $\begin{gathered} 1000 \\ 500 \end{gathered}$ |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |

NOTES

1. Typically doubles for every $10^{\circ} \mathrm{C}$ increase in temperature.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, absolute maximum input voltage is equal to the supply voltage.

## EQUIVALENT SCHEMATIC



## AC ELECTRICAL CHARACTERISTICS

$T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$
unless otherwise specified.

| PARAMETER | TEST CONDITIONS | $\mu \mathrm{A} 40 \mathrm{C}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Slew rate Unity gain bandwidth |  |  | $\begin{aligned} & 6.0 \\ & 1.0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} / \mu \mathrm{S} \\ & \mathrm{MHz} \end{aligned}$ |
| Transient response (voltage follower circuit) <br> Rise time Overshoot | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{~V}_{1 \mathrm{~N}}=100 \mathrm{mV} \\ \mathrm{C}_{\mathrm{L}} \leq 100 \mathrm{pf}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \end{gathered}$ |  | $\begin{array}{\|c\|} \hline 300 \\ 10 \end{array}$ |  | ns |

TYPICAL PERFORMANCE CHARACTERISTICS


## TEST CIRCUITS

## OFFSET NULL CIRCUIT




## DESCRIPTION

The 747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. High common mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal $6 \mathrm{~dB} /$ octave roll-off insures stability in closed loop applications. For single amplifier performance, see $\mu \mathrm{A} 741$ data sheet.

## FEATURES

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up
- $\mu$ A747, SA747C Mil std 883A,B,C available


## PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC
EQUIVALENT CIRCUIT (EACH SIDE)


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage |  |  |
| $\mu A 747$ | $\pm 22$ | V |
| $\mu \mathrm{~A} 747 \mathrm{C}$ | $\pm 18$ | V |
| SA747C | V |  |
| Internal power dissipation | 500 | mW |
| Metal can | 670 | mW |
| DIP | $\pm 30$ | V |
| Differential input voltage | $\pm 15$ | V |
| Input voltage | $\pm 0.5$ | V |
| Voltage between offset null | -65 to +155 | ${ }^{\circ} \mathrm{C}$ |
| and V- | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -40 to +85 |  |
| $\mu A 747$ |  |  |
| $\mu A 747 \mathrm{C}$ |  | ${ }^{\circ} \mathrm{C}$ |
| SA747C | 300 |  |
| Lead temperature | indefinite |  |
| (soldering, 60 sec) |  |  |
| Output short-circuit duration |  |  |

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | $\mu$ A747 |  |  | $\mu$ A747C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos Vos | Offset voltage Offset voltage | $\begin{gathered} \mathrm{Rs} \leq 10 \mathrm{k} \Omega \\ \text { Rs } \leq 10 \mathrm{k} \Omega, \text { over temp } \end{gathered}$ |  | $\begin{aligned} & 2.0 \\ & 3.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 7.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| $\begin{aligned} & \text { los } \\ & \text { los } \\ & \text { los } \\ & \text { los } \end{aligned}$ | Offset current Offset current Offset current Offset current | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \\ \text { Over temp } \end{gathered}$ |  | $\begin{aligned} & 20 \\ & 7.0 \\ & 85 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & 200 \\ & 300 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IBIAS <br> IBIAS <br> IBIAS <br> IBIAS | Input current Input current Input current Input current | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \\ & \text { Over temp } \end{aligned}$ |  | $\begin{gathered} \hline 80 \\ 30 \\ 300 \end{gathered}$ | $\begin{aligned} & \hline 500 \\ & 500 \\ & 1500 \end{aligned}$ |  | 80 <br> 30 | $\begin{aligned} & 500 \\ & 800 \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Vout | Output voltage swing | $R_{L} \geq 2 k \Omega$, over temp $R_{L} \geq 10 \mathrm{k} \Omega$, over temp | $\begin{aligned} & \pm 10 \\ & \pm 12 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 14 \end{aligned}$ |  | $\begin{aligned} & \pm 10 \\ & \pm 12 \end{aligned}$ | $\begin{aligned} & \pm 13 \\ & \pm 14 \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| Icc | Supply current | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \\ & \text { Over temp } \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.7 \\ & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \hline 2.8 \\ & 2.5 \\ & 3.3 \end{aligned}$ |  | $\begin{aligned} & \hline 1.7 \\ & 2.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 2.8 \\ & 3.3 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
|  | Power consumption | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \end{aligned}$ Over temp |  | $\begin{aligned} & 50 \\ & 45 \\ & 60 \end{aligned}$ | $\begin{gathered} 85 \\ 75 \\ 100 \end{gathered}$ |  | 50 <br> 60 | $\begin{gathered} 85 \\ 100 \end{gathered}$ | $\begin{aligned} & \mathrm{mW} \\ & \mathrm{~mW} \\ & \mathrm{~mW} \\ & \mathrm{~mW} \end{aligned}$ |
|  | Input capacitance |  |  | 1.4 |  |  | 1.4 |  | pF |
|  | Offset voltage adjustment range |  |  | $\pm 15$ |  |  | $\pm 15$ |  | V |
|  | Output resistance |  |  | 75 |  |  | 75 |  | $\Omega$ |
|  | Channel separation |  |  | 120 |  |  | 120 |  | dB |
| PSRR | Supply voltage rejection ratio | RS $\leq 10 \mathrm{k} \Omega$, over temp |  | 30. | 150 |  | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| Avol | Large signal voltàge gain (DC) | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \mathrm{V}_{\text {OUT }}= \pm 10 \mathrm{~V}$ | 50,000 |  |  | 25,000 |  |  | V/V |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA747C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ |  | 2.0 | 6.0 | mV |
| Vos | Offset voltage | $\mathrm{Rs} \leq 10 \mathrm{k} \Omega$, over temp |  | 3.0 | 7.5 | mV |
| los | Offset current |  |  | 20 | 200 | nA |
| los | Offset current | Over temp |  |  | 500 | nA |
| IBIAS | Input current |  |  |  | 1500 | nA |
| IBIAS | Input current | Over temp |  |  | 500 | nA |
| Vout | Output voltage swing | $R_{L} \geq 2 k \Omega$, over temp | $\pm 10$ | $\pm 13$ |  | V |
|  |  | $R_{L} \geq 10 \mathrm{k} \Omega$, over temp | $\pm 12$ | $\pm 14$ |  | V |
| ICC | Supply current |  |  | 1.7 | 2.8 | mA |
|  |  | Over temp |  | 2.0 | 3.3 | mA |
|  | Power consumption |  |  | 50 | 85 | mW |
|  |  | Over temp |  | 60 | 100 | mW |
|  | Input capacitance |  |  | 1.4 |  | pF |
|  | Offset voltage adjustment range |  |  | $\pm 15$ |  | V |
|  | Output resistance |  |  | 75 |  | $\Omega$ |
|  | Channel separation |  |  | 120 |  | dB |
| PSRR | Supply voltage rejection ratio | $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$, over temp |  | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
|  | Large signal voltage gain (DC) | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega$ V $\mathrm{OUT}= \pm 10 \mathrm{~V}$ | 25,000 |  |  | V/V |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{S}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | $\mu$ A747/ $\mu$ A747C/SA747C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Transient response Risetime Overshoot | $\mathrm{V}_{\mathrm{IN}}=20 \mathrm{mV}, \mathrm{R}_{1}=2 \mathrm{k} \Omega, \mathrm{C}_{1}<100 \mathrm{pf}$ <br> Unity gain $C L \leq 100 \mathrm{pf}$ <br> Unity gain $\mathrm{CL} \leq 100 \mathrm{pf}$ |  | $\begin{aligned} & 0.3 \\ & 5.0 \\ & \hline \end{aligned}$ |  | $\mu \mathrm{S}$ $\%$ |
| Slew rate | $\mathrm{RL}>2 \mathrm{k} \Omega$ |  | 0.5 |  | $\mathrm{V} / \mu \mathrm{s}$ |

TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE


TRANSIENT RESPONSE

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE


OUTPUT VOLTAGE SWING AS A FUNCTION OF frequency


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)
 AS A FUNCTION OF AMBIENT TEMPERATURE


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE


INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


## DESCRIPTION

The 748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

## FEATURES

- Short circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up
- Mil std 883A,B,C available


## EQUIVALENT CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

$\left.\begin{array}{|c|c|c|}\hline \text { PARAMETER } & \text { RATING } & \text { UNIT } \\ \hline \text { Supply voltage } & & \\ \mu A 748 & \pm 22 & \mathrm{~V} \\ \mu \mathrm{~A} 748 \mathrm{C} \\ \text { SA748C }\end{array}\right\}$

NOTES

1. Rating applies for case temperatures to $+70^{\circ} \mathrm{C}$.
2. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to $+70^{\circ} \mathrm{C}$ ambient temperature.

## PIN CONFIGURATIONS



## GENERIL PIRPOSE OPERATIONAL AMPLIFIER

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | $\mu \mathrm{A} 448$ |  |  | $\mu \mathrm{A} 48 \mathrm{C}$ |  |  | SA748C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Offset voltage |  | $\begin{gathered} \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \text { Over temperature } \end{gathered}$ |  | 1.0 | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ |  | 2.0 | $\begin{aligned} & 6.0 \\ & 7.5 \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 7.5 \end{aligned}$ | 6.0 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| $\begin{aligned} & \text { los } \\ & \text { los } \\ & \text { los } \end{aligned}$ | Offset current Offset current Offset current | $\begin{aligned} & 25^{\circ} \leq T_{A} \leq T_{\max } \\ & T_{\text {min }} \leq T_{A} \leq 25^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 7.0 \\ & 85 \end{aligned}$ | $\begin{array}{\|l\|} \hline 200 \\ 200 \\ 500 \\ \hline \end{array}$ |  | $\begin{aligned} & 20 \\ & 9.0 \\ & 35 \end{aligned}$ | $\begin{aligned} & 200 \\ & 300 \\ & 300 \end{aligned}$ |  | 20 7.0 85 | $\begin{array}{\|l\|} \hline 200 \\ 200 \\ 500 \\ \hline \end{array}$ | nA |
| IBIAS <br> IBIAS <br> IBIAS | Input current Input current Input current | $\begin{aligned} & 25^{\circ} \leq T_{A} \leq T_{\max } \\ & T_{\min } \leq T_{A} \leq 25^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & \hline 80 \\ & 30 \\ & 300 \\ & \hline \end{aligned}$ | $\begin{array}{\|l\|} \hline 500 \\ 500 \\ 1500 \end{array}$ |  | $\begin{array}{c\|} \hline 80 \\ 40 \\ 130 \end{array}$ | $\begin{aligned} & \hline 500 \\ & 800 \\ & 800 \end{aligned}$ |  | $\begin{aligned} & \hline 80 \\ & 30 \\ & 300 \end{aligned}$ | $\begin{array}{\|c\|} \hline 500 \\ 500 \\ 1500 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| $V_{\text {CM }}$ | Common mode voltage range | Over temperature | $\pm 12$ | $\pm 13$ |  | $\pm 12$ | $\pm 13$ |  |  | $\pm 12$ | $\pm 13$ | V |

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | $\mu$ A748 |  |  | $\mu$ A748C/SA748C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| CmRR | Common mode rejection ratio |  | RS $\leq \pm 10 k \Omega$, over temperature | 70 | 90 |  | 70 | 90 |  | dB |
| RIN | Input resistance |  | 0.3 | 2.0 |  | . 30 | 2.0 |  | $\mathrm{M} \Omega$ |
| Vout | Output voltage swing | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega$, over temperature | $\pm 10$ | $\pm 13$ |  | $\pm 10$ | $\pm 13$ |  | V |
| Vout | Output voltage swing | $R_{L} \geq 10 \mathrm{k} \Omega$, over temperature | $\pm 12$ | $\pm 14$ |  | $\pm 12$ | $\pm 14$ |  | V |
| ICc | Supply current |  |  | 1.7 | 2.8 |  | 1.7 | 2.8 | mA |
| Icc | Supply current | $25^{\circ} \leq T_{A} \leq T_{\text {max }}$ |  | 1.5 | 2.5 |  | 1.6 | 3.3 | mA |
| ICC | Supply current | $\mathrm{T}_{\text {min }} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C}$ |  | 2.0 | 3.3 |  | 1.8 | 3.3 | mA |
| $\mathrm{P}_{\mathrm{d}}$ | Power consumption | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 50 | 85 |  | 50 | 85 | mW |
| $\mathrm{Pd}_{\mathrm{d}}$ | Power consumption | $25^{\circ} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {max }}$ |  | 45 | 75 |  | 48 | 100 | mW |
| $\mathrm{Pd}_{\mathrm{d}}$ | Power consumption | $T_{\text {min }} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C}$ |  | 60 | 100 |  | 54 | 100 | mW |
| PSRR | Supply voltage rejection ratio | RS $\leq 10 \mathrm{k} \Omega$, over temperature |  | 30 | 150 |  | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
|  | Output resistance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 75 |  |  | 75 |  | $\Omega$ |
| Avol | Large signal voltage gain | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega$ V ${ }_{\text {OUT }} \pm 10 \mathrm{~V} \pm 15 \mathrm{~V}$ | 50 | 200 |  | 50 | 200 |  | $\mathrm{V} / \mathrm{mV}$ |
| Avol | Large signal voltage gain | Over temperature | 25 |  |  | 25 |  |  | $\mathrm{V} / \mathrm{mV}$ |
|  | Input capacitance |  |  | 1.4 |  |  | 1.4 |  | pF |
|  | Offset voltage adjustment range |  |  | $\pm 15$ |  |  | $\pm 15$ |  | mV |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | $\mu$ A748 |  |  | $\mu$ A748C/SA748C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Transient response (unity gain) <br> Rise time Overshoot | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=20 \mathrm{mV}, R_{\mathrm{L}}=2 \mathrm{k} \Omega \\ \mathrm{C}_{\mathrm{L}} \leq 100 \mathrm{pF} \\ \mathrm{C}_{1}=30 \mathrm{pF} \end{gathered}$ |  | $\begin{aligned} & 0.3 \\ & 5.0 \end{aligned}$ |  |  | $\begin{aligned} & 0.3 \\ & 5.0 \end{aligned}$ |  | ${ }_{\text {M }} \mathrm{S}$ |
| Slew rate | $\mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \mathrm{C}_{1}=30 \mathrm{pF}$ |  | 0.5 |  |  | 0.5 |  | $\mathrm{V} / \mu \mathrm{S}$ |

## TYPICAL CHARACTERISTIC CURVES

## POWER CONSUMPTION

 AS A FUNCTION OF SUPPLY VOLTAGE

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY


INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE


ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE


BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE


TYPICAL CHARACTERISTIC CURVES
(Cont'd)

OPEN LOOP VOLTAGE GAIN
AS A FUNCTION OF FREQUENCY


INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY


TRANSIENT RESPONSE


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY


OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY


COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


## VIDEO AMPIIFIERS

## DESCRIPTION

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the $\mu \mathrm{A} 733$.

## EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | $\pm 8$ | V |
| Differential input voltage | $\pm 5$ | V |
| Common mode | $\pm 6$ | V |
| Input voltage | 10 | mA |
| Output current |  | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE592K | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE592K | -65 to +150 | mW |
| Storage temperature range | 500 |  |
| Power dissipation |  |  |

## FEATURES

- 120 MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required

PIN CONFIGURATION


NOTE
Pin 5 connected to case.

DC ELECTRICAL CHARACTERISTICS
$T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 6 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0$ unless otherwise specified
Recommend operating supply voltages $\mathrm{V}_{\mathrm{S}}= \pm 6.0 \mathrm{~V}$

| PARAMETER | TEST CONDITIONS | NE592 |  |  | SE592 |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Differential voltage gain Gain 11 Gain 22 | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$, V VOUT $=3 \mathrm{~V}$ p-p | $\begin{gathered} 250 \\ 80 \\ \hline \end{gathered}$ | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 120 \end{aligned}$ | $\begin{gathered} 300 \\ 90 \end{gathered}$ | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 500 \\ & 110 \end{aligned}$ | $\begin{aligned} & V / V \\ & V / V \end{aligned}$ |
| $\begin{array}{r} \hline \text { Bandwidth } \\ \text { Gain } 11 \\ \text { Gain } 22 \\ \text { Rise time } \\ \text { Gain } 11 \\ \text { Gain } 22 \\ \hline \end{array}$ | Vout $=1 \mathrm{Vp}$ pp |  | $\begin{gathered} 40 \\ 90 \\ \\ 10.5 \\ 4.5 \end{gathered}$ | 12 |  | $\begin{gathered} 40 \\ 90 \\ \\ 10.5 \\ 4.5 \\ \hline \end{gathered}$ | 10 | MHz <br> MHz <br> ns ns |
| Propagation delay Gain 11 Gain 22 | $\mathrm{V}_{\text {OUT }}=1 \mathrm{Vp}-\mathrm{p}$ |  | $\begin{aligned} & 7.5 \\ & 6.0 \end{aligned}$ | 10 |  | $\begin{aligned} & 7.5 \\ & 6.0 \end{aligned}$ | 10 | $\begin{aligned} & \mathrm{ns} \\ & \text { ns } \\ & \hline \end{aligned}$ |
| Input resistance <br> Gain 11 <br> Gain 22 <br> Input capacitance2 Input offset current Input bias current Input noise voltage Input voltage range | Gain 2 <br> BW 1 kHz to 10 kHz | 10 | $\begin{aligned} & 4.0 \\ & 30 \\ & 2.0 \\ & 0.4 \\ & 9.0 \\ & 12 \end{aligned}$ | $\begin{array}{r} 5.0 \\ 30 \\ \\ \pm 1.0 \\ \hline \end{array}$ | 20 | $\begin{aligned} & 4.0 \\ & 30 \\ & 2.0 \\ & 0.4 \\ & 9.0 \\ & 12 \end{aligned}$ | $\begin{array}{r} 3.0 \\ 20 \\ \\ \pm 1.0 \\ \hline \end{array}$ | $\begin{gathered} \mathrm{k} \Omega \\ \mathrm{k} \Omega \\ \mathrm{pF} \\ \mu \mathrm{~A} \\ \mu \mathrm{~A} \\ \mu \mathrm{Vms} \\ \mathrm{~V} \end{gathered}$ |
| Common mode rejection ratio <br> Gain 2 <br> Gain 2 <br> Supply voltage rejection ratio Gain 2 | $\begin{gathered} \mathrm{VCM} \pm 1 \mathrm{~V}, \mathrm{~F}<100 \mathrm{kHz} \\ \mathrm{VCM} \pm 1 \mathrm{~V}, \mathrm{~F}=5 \mathrm{MHz} \\ \Delta \mathrm{VS}= \pm 0.5 \mathrm{~V} \end{gathered}$ | 60 <br> 50 | 86 <br> 60 <br> 70 |  | 60 <br> 50 | $\begin{aligned} & 86 \\ & 60 \\ & 70 \\ & \hline \end{aligned}$ |  | dB <br> dB <br> dB |
| Output offset voltage <br> Gain 33 <br> Output common mode voltage <br> Ouptut voltage swing <br> Ouput resistance <br> Power supply current | $\begin{aligned} R_{L} & =\infty \\ R_{L} & =\infty \\ R_{L} & =2 K \\ & \\ R_{L} & =\infty \end{aligned}$ | $\begin{aligned} & 2.4 \\ & 3.0 \end{aligned}$ | $\begin{gathered} 0.35 \\ 2.9 \\ 4.0 \\ 20 \\ 18 \end{gathered}$ | $\begin{gathered} 0.75 \\ 3.4 \end{gathered}$ <br> 24 | $\begin{aligned} & 2.4 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 0.35 \\ & 2.9 \\ & 4.0 \\ & 20 \\ & 18 \end{aligned}$ | $\begin{gathered} 0.75 \\ 3.4 \\ \\ 24 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \\ \Omega \\ \mathrm{~mA} \end{gathered}$ |

NOTES

1. Gain select pins $G_{1 A}$ and $G_{1 B}$ connected together.
2. Gain select pins $G_{2 A}$ and $G_{2 B}$ connected together.
3. All gain select pins open.

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


VOLTAGE GAIN AS A FUNCTION OF FREQUENCY


PHASE SHIFT AS A FUNCTION OF FREQUENCY


VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)


TEST CIRCUITS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified



## DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

## FEATURES

- 120 MHz bandwidth
- 250k $\Omega$ input resistance
- Selectable gains of 10,100 and 400
- No frequency compensation required
- Mil std 883A,B,C available

PIN CONFIGURATION


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Differential input Voltage | $\pm 5$ | V |
| Common mode input Voltage | $\pm 6$ | V |
| Vcc | $\pm 8$ | V |
| Ouput current | 10 | mA |
| Junction temperature | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operation temperature range |  |  |
| $\mu$ A733C | 0 to +75 | ${ }^{\circ} \mathrm{C}$ |
| $\mu$ A733 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| PD Power dissipation |  |  |
| K package | 500 | mW |
| N, F package | 670 | mW |

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm \mathrm{V}, \mathrm{VCM}=0$ unless otherwise specified.
Recommended operating supply voltages $V_{S}= \pm 6.0 \mathrm{~V}$.

| PARAMETER | TEST CONDITIONS | ${ }_{\mu \text { A733C }}$ |  |  | $\mu$ A733 |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| ```Differential voltage gain Gain \(1^{1}\) Gain \(2^{2}\) Gain \(3^{3}\)``` | $\mathrm{R}_{\mathrm{I}}=2 \mathrm{k} \Omega$, $\mathrm{V}_{\text {OUT }}=3 \mathrm{Vp}-\mathrm{p}$ | $\begin{gathered} 250 \\ 80 \\ 8.0 \end{gathered}$ | $\begin{gathered} 400 \\ 100 \\ 10 \end{gathered}$ | $\begin{gathered} 600 \\ 120 \\ 12 \end{gathered}$ | $\begin{gathered} 300 \\ 90 \\ 9.0 \end{gathered}$ | $\begin{gathered} 400 \\ 100 \\ 10 \end{gathered}$ | $\begin{gathered} 500 \\ 110 \\ 11 \end{gathered}$ | $\begin{aligned} & V / V \\ & V / V \\ & V / V \end{aligned}$ |
| Bandwidth Gain $1^{1}$ Gain $2^{2}$ Gain $3^{3}$ Rise time Gain $1^{1}$ Gain $2^{2}$ Gain $3^{3}$ | $V_{\text {OUT }}=1 \mathrm{Vp}-\mathrm{p}$ |  | $\begin{gathered} 40 \\ 90 \\ 120 \\ \\ 10.5 \\ 4.5 \\ 2.5 \end{gathered}$ | 12 |  | $\begin{gathered} 40 \\ 90 \\ 120 \\ \\ 10.5 \\ 4.5 \\ 2.5 \\ \hline \end{gathered}$ | 10 | MHz <br> MHz <br> MHz <br> ns <br> ns <br> ns |
| ```Propagation delay Gain \(1^{1}\) Gain \(2^{2}\) Gain \(3^{3}\)``` | $\mathrm{V}_{\text {OUT }}=1 \mathrm{Vp}-\mathrm{p}$ |  | 7.5 6.0 3.6 | 10 |  | $\begin{aligned} & 7.5 \\ & 6.0 \\ & 3.6 \end{aligned}$ | 10 | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| Input resistance <br> Gain $1^{1}$ <br> Gain $2^{2}$ <br> Gain $3^{3}$ <br> Input capacitance2 Input offset current Input bias current Input noise voltage Input voltage range | Gain 2 $\mathrm{BW}=1 \mathrm{kHz} \text { to } 10 \mathrm{MHz}$ | 10 $\pm 1.0$ | $\begin{gathered} 4.0 \\ 30 \\ 250 \\ 2.0 \\ 0.4 \\ 9.0 \\ 12 \end{gathered}$ | 5.0 30 | 20 $\pm 1.0$ | $\begin{aligned} & 4.0 \\ & 30 \\ & 250 \\ & 2.0 \\ & 0.4 \\ & 9.0 \\ & 12 \end{aligned}$ | 3.0 20 | $\begin{gathered} \mathrm{k} \Omega \\ \mathrm{k} \Omega \\ \mathrm{k} \Omega \\ \mathrm{pF} \\ \mu \mathrm{~A} \\ \mu \mathrm{~A} \\ \mu \mathrm{Vms} \\ \mathrm{~V} \end{gathered}$ |
| Common mode <br> Rejection ratio Gain 2 <br> Gain 2 <br> Supply voltage Rejection ratio Gain 2 | $\begin{aligned} & \mathrm{VCM}= \pm \mathrm{V}, \mathrm{f} \leq 100 \mathrm{kHz} \\ & \mathrm{VCM}= \pm 1 \mathrm{~V}, \mathrm{~F}=5 \mathrm{MHz} \end{aligned}$ $\Delta V_{S}= \pm 0.5 \mathrm{~V}$ | 60 <br> 50 | 86 60 <br> 70 |  | 60 <br> 50 | 86 60 <br> 70 |  | dB <br> dB <br> dB |
| Output offset voltage Gain $1^{1}$ Gain 2 and $3^{2,3}$ <br> Output common mode voltage <br> Output voltage swing <br> Output sink current <br> Output resistance <br> Power supply current | $\begin{aligned} R_{L} & =\infty \\ R_{L} & =\infty \\ R_{L} & =2 k \end{aligned}$ <br> $R \mathrm{~L} \pm \infty$ | $\begin{aligned} & 2.4 \\ & 3.0 \\ & 2.5 \end{aligned}$ | $\begin{gathered} 0.6 \\ 0.35 \\ 2.9 \\ 4.0 \\ 3.6 \\ 20 \\ 18 \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 1.5 \\ & 3.4 \end{aligned}$ <br> 24 | 2.4 3.0 2.5 | 0.6 0.35 2.9 4.0 3.6 20 18 | $\begin{aligned} & 1.5 \\ & 1.0 \\ & 3.4 \end{aligned}$ <br> 24 | V V <br> v <br> mA <br> $\Omega$ <br> mA |

NOTES

1. Gain select pins $G_{1 A}$ and $G_{1 B}$ connected together.
2. Gain select pins $G_{2 A}$ and $G_{2 B}$ connected together.
3. All gain select pins open.

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TEST CIRCUITS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.


## section 3 VOITAGE REGULATORS

## DESCRIPTION

The LM109/209/309 are complete 5 volt regulators fabricated on a single silicon chip. These regulators are designed for local "on card" regulation to eliminate many of the noise and ground loop problems associated with single-point regulation. They employ internal current limiting, thermal shutdown, and safe-area compensation which makes the circuitry essentially blowout proof. If adequate heat sinking is provided, the devices can deliver output currents in excess of 200 mA from the TO-5 package, and 1A from the TO-3 package. In addition to their use as fixed 5 volt regulators, these devices may be used with external components to obtain adjustable output levels. They may also be used as the power pass element in precision regulators.

FEATURES

- Output currents in excess of 1 mA
- Internal thermal overload protection
- Internal current limiting
- No external components required
- LM109 military qualifications pending

PIN CONFIGURATION
DB PACKAGE (TO-5).


ORDER PART NOS. LM109DB/LM209DB/LM309DB
DA PACKAGE (TO-3)


CASE IS CONNECTED TO GROUND.
ORDER PART NO. LM109DA/LM209DA/LM309DA

## EQUIVALENT CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Input voltage | 35 | V |
| Power dissipation | Internally limited |  |
| Operating junction temperature range | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| LM109 | -25 to 150 | ${ }^{\circ} \mathrm{C}$ |
| LM209 | 0 to 125 | ${ }^{\circ} \mathrm{C}$ |
| LM309 | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{J}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}$ unless otherwise specified 1,2

| PARAMETER | TEST CONDITIONS | LM109/LM209 |  |  | LM309 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output voltage |  | 4.7 | 5.05 | 5.3 | 4.8 | 5.05 | 5.2 | V |
| Line regulation | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  | 4 | 50 |  | 4 | 50 | mV |
| $\begin{aligned} & \text { Load regulation } \\ & \text { TO-5 } \\ & \text { TO-3 } \end{aligned}$ | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 0.5 \mathrm{~A} \\ & 5 \mathrm{~mA} \leq \text { Iout } \leq 1.5 \mathrm{~A} \\ & \hline \end{aligned}$ |  | $\begin{array}{r} 20 \\ 50 \\ \hline \end{array}$ | $\begin{gathered} 50 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{array}{r} 20 \\ 50 \\ \hline \end{array}$ | $\begin{gathered} 50 \\ 100 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Output voltage | $\begin{gathered} 5 \mathrm{~mA} \leq I_{\text {OUT }} \leq I_{\text {max }} P<P_{\text {max }} \text { over temp. } \\ 8 V \leq V_{\text {IN }} \leq 20 V \\ 7 \mathrm{~V} \leq V_{\text {IN }} \leq 25 \mathrm{~V} \\ \hline \end{gathered}$ | 4.6 |  | 5.4 | 4.75 |  | 5.25 | V |
| Quiescent current Quiescent current change | $\begin{gathered} \hline 7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V} \text {, over temp. } \\ 5 \mathrm{~mA} \leq \text { IouT } \leq I_{\text {max }} \\ 8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V} \\ 7 \mathrm{~V} \leq \mathrm{VIN}_{\text {IN }} \leq 25 \mathrm{~V} \\ \hline \end{gathered}$ |  | 5.2 | $\begin{aligned} & 10 \\ & 0.5 \\ & 0.8 \end{aligned}$ |  | 5.2 | $\begin{aligned} & \hline 10 \\ & 0.5 \\ & \\ & 0.8 \\ & \hline \end{aligned}$ | $\begin{array}{\|l\|} \hline \mathrm{mA} \\ \mathrm{~mA} \\ \mathrm{~mA} \\ \mathrm{~mA} \\ \hline \end{array}$ |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 40 |  |  | 40 |  | $\mu \mathrm{V}$ |
| Long term stability |  |  |  | 10 |  |  | 20 | mV |
| $\begin{aligned} & \text { Thermal resistance junction to case }{ }^{2} \\ & \text { TO-5 } \\ & \text { TO-3 } \end{aligned}$ |  |  | 15 3 |  |  | 15 3 |  | $0^{\circ} \mathrm{C} / \mathrm{W}$ |

## NOTES

1. Unless otherwise specified, IOUT $=0.1 \mathrm{~A}$ for the TO-5 package or IOUT $=0.5 \mathrm{~A}$ for the TO-3 package. For the TO-5 package, $\mathrm{I} \max =0.2 \mathrm{~A}$ and $\mathrm{Pmax}=2.0 \mathrm{~W}$. For the $\mathrm{TO}-3$ package, $\operatorname{Imax}=1.0 \mathrm{~A}$ and $\mathrm{Pmax}=20 \mathrm{~W}$.
2. Without a heat sink, the thermal resistance of the TO-5 package is about $150^{\circ} \mathrm{C} / \mathrm{W}$, while that of the TO-3 package is approximately $35^{\circ} \mathrm{C} / \mathrm{W}$. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The LM340 series of 3-terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi , and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages.

FEATURES

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-220 and metal TO-3 packages


## EQUIVALENT SCHEMATIC



## PIN CONFIGURATION



DA PACKAGE (TO-3) (Top View)


ORDER INFORMATION

| ORDER INFORMATION |  |
| :---: | :---: |
| OUTPUT | ORDER |
| VOLTAGE | PART NO. |
| 5 V | LM340-5DA |
| 6 V | LM340-6DA |
| 8 V | LM340-8DA |
| 12 V | LM340-12DA |
| 15 V | LM340-15DA |
| 18 V | LM340-18DA |
| 24 V | LM340-24DA |

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Input voltage |  |  |
| $\mathrm{V}_{0}=5 \mathrm{~V}$ through 18 V | 35 | V |
| $\mathrm{~V}_{0}=24 \mathrm{~V}$ | 40 | V |
| Internal power dissipation1 | Internally limited | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | 0 to 70 |  |
| Maximum junction temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| TO-3 package | 150 | ${ }^{\circ} \mathrm{C}$ |
| TO-220 package | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range |  | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  | ${ }^{\circ} \mathrm{C}$ |
| TO-3 package (soldering 10sec) | 200 |  |
| TO-220 package (soldering, 10 sec ) | 230 |  |

NOTE

1. Thermal resistance without a heat sink for junction to case temperature is $4^{\circ} \mathrm{C} / \mathrm{W}$ for the TO-3 package and $6^{\circ} \mathrm{C} / \mathrm{W}$ for the TO-220 package. Thermal resistance for case to ambient temperature is $35^{\circ} \mathrm{C} / \mathrm{W}$ for the TO-3 package and $50^{\circ} \mathrm{C} / \mathrm{W}$ for the TO-220 package.

DC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | LM340-5 |  |  | LM340-6 |  |  | LM340-8 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Output voltage | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \mathrm{PD}_{\mathrm{D}}=\leq 15 \mathrm{~W} \\ 5 \mathrm{~mA} \leq \mathrm{IOUT} \leq 1.0 \mathrm{~A} \end{gathered}$ | $\begin{array}{r} 4.8 \\ 7 \mathrm{~V} \\ 4.75 \end{array}$ | $\begin{gathered} N=10 \\ 5 \\ V_{\text {IN }} \leq \end{gathered}$ | $\begin{gathered} 5.2 \\ 0 \mathrm{~V} \\ 5.25 \end{gathered}$ | $\begin{array}{r} 5.75 \\ 81 \\ 5.7 \end{array}$ | N $=1$ 6 VIN | $6.25$ $21 \mathrm{~V}$ $6.3$ | $\begin{gathered} 7.7 \\ 10 \\ 7.6 \end{gathered}$ | $\begin{aligned} & \mathbb{N}=1 \\ & 8 \\ & \leq V_{I N} \end{aligned}$ | $\begin{array}{r} 8.3 \\ =23 \mathrm{~V} \\ 8.4 \end{array}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Line regulation | $\begin{aligned} & \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & \mathrm{IOUT}=100 \mathrm{~mA} \\ & \text { IOUT }=500 \mathrm{~mA} \end{aligned}$ |  | $\mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} 5 \mathrm{~V} \\ 50 \\ 100 \\ \hline \end{gathered}$ |  | VIN | $\begin{gathered} \hline 25 \mathrm{~V} \\ 60 \\ 120 \\ \hline \end{gathered}$ |  | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{gathered} \hline 25 \mathrm{~V} \\ 80 \\ 160 \\ \hline \end{gathered}$ | mV |
| Load regulation | $\begin{gathered} \mathrm{TJ}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \mathrm{IOUT} \leq 1.5 \mathrm{~A} \end{gathered}$ |  |  | 100 |  |  | 120 |  |  | 160 | mV |
| Quiescent current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 4.2 | 10 |  | 4.2 | 10 |  | 4.2 | 10 | mA |
| Quiescent current change |  | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  | mA |
|  | $5 \mathrm{~mA} \leq$ IOUT $\leq 1.5 \mathrm{~A}$ |  |  | . 5 |  |  | . 5 |  |  | . 5 | mA |
| Output noise voltage | $\begin{gathered} T_{J}=25^{\circ} \mathrm{C} \\ 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{gathered}$ |  | 40 |  |  | 45 |  |  | 52 |  | $\mu \mathrm{A}$ |
| Voltage drift | $\mathrm{mV} / 1000 \mathrm{Hrs}$. |  |  | 20 |  |  | 24 |  |  | 32 | mV |
| Ripple rejection | $\begin{gathered} \text { IOUT }=20 \mathrm{~mA} \\ f=120 \mathrm{~Hz} \end{gathered}$ |  | 60 |  |  | 57 |  |  | 55 |  | dB |
| Dropout voltage | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | 2 |  |  | 2 |  |  | 2.5 |  |  | V |

DC ELECTRICAL CHARACTERISTICS (Cont'd) lout $=500 \mathrm{~mA},\left(0^{\circ} \mathrm{C} \leq T_{A} \leq 70^{\circ} \mathrm{C}\right)$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LM340-12 |  |  | LM340-15 |  |  | LM340-18 |  |  | LM340-24 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Output voltage | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \mathrm{PD}_{\mathrm{D}}=\leq 15 \mathrm{~W} \\ 5 \mathrm{~mA} \leq \mathrm{IOUT}^{\leq} \leq 1.0 \mathrm{~A} \end{gathered}$ | $\begin{gathered} V^{V} \\ 11.5 \\ 14.5 \mathrm{~V} \\ 11.4 \end{gathered}$ | $\mathrm{N}=1$ 12 $\leq \mathrm{V}$ IN | $\begin{gathered} 12.5 \\ \leq 27 \mathrm{~V} \\ 12.6 \end{gathered}$ | $\begin{array}{\|c\|} V \\ 14.4 \\ 17.5 V \\ 14.25 \end{array}$ | $\mathrm{N}=2$ 15 $\leq \mathrm{V}_{\text {IN }}$ | $\begin{aligned} & 3 \mathrm{~V} \\ & 15.6 \\ & \leq 30 \mathrm{~V} \\ & 15.75 \end{aligned}$ | $\begin{gathered} 17.3 \\ 21 \mathrm{~V} \\ 17.1 \end{gathered}$ | $\mathrm{N}=2$ 18 $\leq \mathrm{VIN}$ | $\begin{aligned} & 7 \mathrm{~V} \\ & 18.7 \\ & \leq 33 \mathrm{~V} \\ & 18.9 \end{aligned}$ | 23 27 V 22.8 | $=33$ 24 VIN | $\begin{aligned} & V \\ & 25 \\ & 38 \mathrm{~V} \\ & 25.2 \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| Line regulation | $\begin{aligned} \mathrm{T}_{J} & =25^{\circ} \mathrm{C} \\ \text { IOUT } & =100 \mathrm{~mA} \\ \text { IOUT } & =500 \mathrm{~mA} \end{aligned}$ | 14.5 V | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{gathered} \leq 30 \mathrm{~V} \\ 120 \\ 240 \\ \hline \end{gathered}$ | 17.5V | $\leq \mathrm{V}_{\mathrm{IN}}$ | $\begin{gathered} \leq 30 \mathrm{~V} \\ 150 \\ 300 \\ \hline \end{gathered}$ | 21 V | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{aligned} & \leq 33 \mathrm{~V} \\ & 180 \\ & 360 \\ & \hline \end{aligned}$ | 27 V | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{aligned} & \leq 38 \mathrm{~V} \\ & 240 \\ & 480 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load regulation | $\begin{gathered} \mathrm{TJ}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \mathrm{IOUT} \leq 1.5 \mathrm{~A} \end{gathered}$ |  |  | 240 |  |  | 300 |  |  | 360 |  |  | 480 | mV |
| Quiescent current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 4.2 | 10 |  | 4.2 | 10 |  | 4.2 | 10 |  | 4.2 | 10 | mA |
| Quiescent current change |  | $14.5 \mathrm{~V} \leq \mathrm{V}_{1 \mathrm{~N}} \leq 30 \mathrm{~V}$ |  | $\leq 30 \mathrm{~V}$ 1 | $17.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V}$ |  | $\leq 30 \mathrm{~V}$ 1 | 21V | $\leq \mathrm{V}_{\mathrm{IN}} \leq$ | $\begin{gathered} 33 \mathrm{~V} \\ 1 \end{gathered}$ | $27 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  | 10 <br> 38 V | mA |
|  | $5 \mathrm{~mA} \leq \mathrm{loUT} \leq 1.5 \mathrm{~A}$ |  |  | . 4 |  |  | . 5 |  |  | . 5 |  |  | . 5 | mA |
| Output noise voltage | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{gathered}$ |  | 75 |  |  | 90 |  |  | 110 |  |  | 170 |  | $\mu \mathrm{V}$ |
| voltage drift | $\mathrm{mV} / 1000 \mathrm{Hrs}$. |  |  | 48 |  |  | 60 |  |  | 72 |  |  | 96 | mV |
| Ripple rejection | $\begin{gathered} \text { Iout }=20 \mathrm{~mA} \\ f=120 \mathrm{~Hz} \end{gathered}$ |  | 52 |  |  | 50 |  |  | 48 |  |  | 44 |  | dB |
| Dropout voltage | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | 2.5 |  |  | 2.5 |  |  | 3 |  |  | 3 |  |  | V |

## dual polarity reculator

## DESCRIPTION

The NE/SE5551, 2, 3, 4, 5 are dual polarity tracking regulators designed to produce balanced or unbalanced output voltages from 5 to 20 volts with up to 300 mA output current. Similar in specifications to the 78 MXX and 79 MXX fixed regulators, the 5551 series can be continuously adjusted, balanced or unbalanced. Standard fixed voltages available are $\pm 5, \pm 6, \pm 12, \pm 15$, and $+5,-12$ volts. Employing current limiting and thermal shutdown protection, these dual polarity regulators are ideal for local on-card regulation.

FEATURES

- Output current to $\mathbf{3 0 0 m A}$
- Internally current limited
- Thermal overload protected
- Input voltage to $\pm \mathbf{3 2 V}$
- Output balance $1 \%$ typ.
- External balance control
- Continuously adjustable from 5 to 20 volts, balanced or unbalanced
- No external components required
- Short circuit current 400 mA
- Heat sink available for increased power dissipation


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| VIN input voltage | $\pm 32$ | V |
| TSG storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| TJ operating junction temperature | 0 to +125 | ${ }^{\circ} \mathrm{C}$ |
| NE5551,2,3,4,5 | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| SE5551,2,3,4,5 | 300 | ${ }^{\circ} \mathrm{C}$ |

BLOCK DIAGRAM


PIN CONFIGURATIONS


T PACKAGE


ORDER PART NUMBERS

| VOLTAGE | PART NO. |
| :--- | :--- |
| $\pm 5 \mathrm{~V}$ | SE/NE5551T |
| $\pm 6 \mathrm{~V}$ | SE/NE5552T |
| $\pm 12 \mathrm{~V}$ | SE/NE5553T |
| $\pm 15 \mathrm{~V}$ | SE/NE5554T |
| $+5,-12 \mathrm{~V}$ | SE/NE5555T |

Power dissipation (without heat sink)
T Package 2.0 W
N Package 2.0W
New power package pending for over 8W dissipation.

DC ELECTRICAL CHARACTERISTICS
$\mathrm{V}_{\mathrm{IN}}= \pm 20 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=100 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$,
$\mathrm{C}_{\mathrm{IN}}=\mathrm{C}_{\text {OUT }}=0.1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE5551 |  |  | NE5551 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\begin{array}{r} +4.8 \\ -5.2 \end{array}$ | $\begin{aligned} & +5 \\ & +5 \end{aligned}$ | $\begin{array}{r} +5.2 \\ -4.8 \end{array}$ | $\begin{array}{r} +4.8 \\ -5.2 \end{array}$ | $\begin{aligned} & +5 \\ & -5 \end{aligned}$ | $\begin{array}{r} +5.2 \\ -4.8 \\ \hline \end{array}$ | V |
|  | Line regulation Load regulation | $\begin{gathered} \pm 20 \leq \mathrm{VIN}_{\text {IN }} \leq \pm 30 \mathrm{~V} \\ 1 \mathrm{~mA} \leq \mathrm{I}_{\text {Load }} \leq 50 \mathrm{~mA} \\ 1 \mathrm{~mA} \leq \mathrm{I}_{\text {Load }} \leq 200 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} \hline 100 \\ 5 \\ 15 \\ \hline \end{gathered}$ | $\begin{aligned} & 150 \\ & 15 \\ & 50 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 100 \\ 5 \\ 15 \end{gathered}$ | $\begin{gathered} \hline 300 \\ 25 \\ 100 \\ \hline \end{gathered}$ | $\begin{aligned} & m V \\ & m V \\ & m V \end{aligned}$ |
| Vout | Output voltage | $\begin{gathered} 1 \mathrm{~mA} \leq \mathrm{IL} \leq 100 \mathrm{~mA} \\ \pm 20 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq \pm 30 \mathrm{~V} \text { over temp. } 1 \end{gathered}$ | $\begin{aligned} & +4.7 \\ & -5 . \end{aligned}$ | $\begin{aligned} & +5 \\ & -5 \end{aligned}$ | $\begin{aligned} & \hline+5.3 \\ & -4.7 \end{aligned}$ | $\begin{array}{r} \hline+4.7 \\ -5.3 \end{array}$ | $\begin{aligned} & \hline+5 \\ & -5 \end{aligned}$ | $\begin{aligned} & +5.3 \\ & -4.7 \end{aligned}$ | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| $\begin{aligned} & \mathrm{IQ}^{+} \\ & 1 \mathrm{Q}^{-} \end{aligned}$ | Positive quiescent current Negative quiescent current | $\begin{aligned} & I_{\text {Load }}=0 \\ & I_{\text {Load }}=0 \end{aligned}$ |  | $\begin{gathered} 1.70 \\ 5.6 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ |  | $\begin{gathered} 1.70 \\ 5.6 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $V_{\text {BAL }}$ | Input/output differential voltage Output voltage balance Output noise voltage | 100 Hz to 10 kHz |  | $\begin{gathered} 7 \\ .2 \\ 55 \\ \hline \end{gathered}$ |  |  | $\begin{array}{r} 7 \\ .2 \\ 55 \\ \hline \end{array}$ |  |  |
| IPeak | Peak output current <br> Temperature stability of output voltage |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  | $\begin{gathered} \mathrm{mA} \\ \mathrm{mV} /{ }^{\circ} \mathrm{C} \end{gathered}$ |

DC ELECTRICAL CHARACTERISTICS
(Cont'd)

| PARAMETER |  | TEST CONDITIONS | SE5552 |  |  | NE5552 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\begin{aligned} & +5.75 \\ & -6.25 \end{aligned}$ | $\begin{aligned} & \hline+6 \\ & -6 \end{aligned}$ | $\begin{aligned} & +6.25 \\ & -5.75 \end{aligned}$ | $\begin{aligned} & +5.75 \\ & -6.25 \end{aligned}$ | $\begin{aligned} & \hline+6 \\ & -6 \end{aligned}$ | $\begin{aligned} & +6.25 \\ & -5.75 \end{aligned}$ | V |
|  | Line regulation Load regulation | $\begin{gathered} \pm 20 \leq V_{I N} \leq+30 \mathrm{~V} \\ 1 \mathrm{~mA} \leq \mathrm{I}_{\text {Ioad }} \leq 50 \mathrm{~mA} \\ 1 \mathrm{~mA} \leq \mathrm{I}_{\text {Load }} \leq 200 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} \hline 100 \\ 5 \\ 15 \end{gathered}$ | $\begin{gathered} 150 \\ 15 \\ 50 \end{gathered}$ |  | $\begin{gathered} \hline 100 \\ 5 \\ 15 \end{gathered}$ | $\begin{gathered} \hline 300 \\ 25 \\ 100 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vout | Output voltage | $\begin{gathered} 1 \mathrm{~mA} \leq \mathrm{IL} \leq 100 \mathrm{~mA} \\ \pm 20 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq \pm 30 \mathrm{~V} \text { over temp. } 1 \\ \hline \end{gathered}$ | $\begin{aligned} & \hline+5.7 \\ & -6.3 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline+6 \\ & -6 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline+6.3 \\ & -5.7 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline+5.7 \\ & -6.3 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline+6 \\ & -6 \end{aligned}$ | $\begin{aligned} & \hline+6.3 \\ & -5.7 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| $\begin{aligned} & \mathrm{IQ}^{+} \\ & \mathrm{I}^{-} \\ & \hline \end{aligned}$ | Positive quiescent current Negative quiescent current | $\begin{aligned} & I_{\text {Load }}=0 \\ & I_{\text {Load }}=0 \end{aligned}$ |  | $\begin{gathered} \hline 1.70 \\ 5.6 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ |  | $\begin{aligned} & \hline 1.70 \\ & 5.60 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $V_{\text {bal }}$ | Input/output differential voltage <br> Output voltage balance <br> Output noise voltage | 100 Hz to 10 kHz |  | $\begin{gathered} 6 \\ .2 \\ 55 \\ \hline \end{gathered}$ |  |  | 6 <br> . <br> . <br> 55 |  | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~V} \\ \mu \mathrm{Vrms} \end{gathered}$ |
| IPeak | Peak output current Temperature stability of output voltage |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  | $\begin{gathered} \mathrm{mA} \\ \mathrm{mV} /{ }^{\circ} \mathrm{C} \end{gathered}$ |

## DC ELECTRICAL CHARACTERISTICS (Cont'd)

| PARAMETER |  | TEST CONDITIONS | SE5553 |  |  | NE5553 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\begin{aligned} & +11.5 \\ & -12.5 \end{aligned}$ | $\begin{aligned} & +12 \\ & -12 \end{aligned}$ | $\begin{array}{r} +12.5 \\ -11.5 \end{array}$ | $\begin{array}{r} +11.5 \\ -12.5 \end{array}$ | $\begin{aligned} & +12 \\ & -12 \end{aligned}$ | $\begin{array}{r} +12.5 \\ -11.5 \end{array}$ | V |
|  | Line regulation Load regulation | $\begin{aligned} \pm 20 & \leq \mathrm{V}_{\mathrm{IN}} \leq \pm 30 \mathrm{~V} \\ 1 \mathrm{~mA} & \leq I_{\text {Load }} \leq 50 \mathrm{~mA} \\ 1 \mathrm{~mA} & \leq I_{\text {Load }} \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{gathered} 100 \\ 10 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} 150 \\ 25 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{gathered} 100 \\ 10 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} 300 \\ 50 \\ 200 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vout | Output voltage | $\begin{gathered} 1 \mathrm{~mA} \leq I \mathrm{~L} \leq 100 \mathrm{~mA} \\ \pm 20 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq \pm 30 \mathrm{~V} \text { over temp. } 1 \\ \hline \end{gathered}$ | $\begin{array}{r} +11.4 \\ -12.6 \end{array}$ | $\begin{aligned} & +12 \\ & -12 \\ & \hline \end{aligned}$ | $\begin{aligned} & +12.6 \\ & -11.4 \end{aligned}$ | $\begin{array}{r} +11.4 \\ -12.6 \\ \hline \end{array}$ | $\begin{aligned} & +12 \\ & -12 \end{aligned}$ | $\begin{aligned} & +12.6 \\ & -11.4 \end{aligned}$ | $\bar{v}$ |
| $\begin{aligned} & \mathrm{IQ}+ \\ & \mathrm{IQ}- \end{aligned}$ | Positive quiescent current Negative quiescent current | $\begin{aligned} & I_{\text {Load }}=0 \\ & I_{\text {Load }}=0 \end{aligned}$ |  | $\begin{aligned} & \hline 1.70 \\ & 5.60 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ |  | $\begin{aligned} & \hline 1.70 \\ & 5.60 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| VBAL | Input/output differential voltage Output voltage balance Output noise voltage | 100 Hz to 10 kHz |  | $\begin{gathered} 2.5 \\ .2 \\ 55 \end{gathered}$ |  |  | $\begin{gathered} 2.5 \\ .2 \\ 55 \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~V} \\ \mu \mathrm{Vrms} \end{gathered}$ |
| IPeak | Peak output current Temperature stability of output voltage |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  | $\frac{\mathrm{mA}}{\mathrm{mV} /{ }^{\circ} \mathrm{C}}$ |

## DUAL POLARTY REGULATOR

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{V}_{\mathrm{IN}}= \pm 20 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=100 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$,
$\mathrm{C}_{\mathrm{IN}}=\mathrm{C}_{\text {OUT }}=0.1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE5554 |  |  | NE5554 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\begin{aligned} & +14.4 \\ & -15.6 \end{aligned}$ | $\begin{aligned} & +15 \\ & -15 \\ & \hline \end{aligned}$ | $\begin{aligned} & +15.6 \\ & -14.4 \\ & \hline \end{aligned}$ | $\begin{gathered} +14.4 \\ -15.6 \end{gathered}$ | $\begin{array}{r} +15 \\ -15 \end{array}$ | $\begin{aligned} & \hline+15.6 \\ & -14.4 \end{aligned}$ | V |
|  | Line regulation Load regulation | $\begin{gathered} \pm 20 \leq V_{I N} \leq \pm 30 \mathrm{~V} \\ 1 \mathrm{~mA} \leq I_{\text {Load }} \leq 50 \mathrm{~mA} \\ 1 \mathrm{~mA} \leq I_{\text {Load }} \leq 200 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 100 \\ 10 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 150 \\ 25 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline 100 \\ 10 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} 300 \\ 50 \\ 200 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Vout | Output voltage | $\begin{gathered} 1 \mathrm{~mA} \leq I_{\mathrm{L}} \leq 100 \mathrm{~mA} \\ \pm 20 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq \pm 30 \mathrm{~V} \text { over temp. } 1 \end{gathered}$ | $\begin{aligned} & +14.25 \\ & -15.75 \end{aligned}$ | $\begin{aligned} & +15 \\ & -15 \end{aligned}$ | $\left\|\begin{array}{l} +15.75 \\ -14.25 \end{array}\right\|$ | $\begin{array}{\|} +14.25 \\ -15.75 \end{array}$ | $\begin{aligned} & +15 \\ & -15 \end{aligned}$ | $\begin{aligned} & +15.75 \\ & -14.25 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \mathrm{I}^{+} \\ & \mathrm{I}^{-} \end{aligned}$ | Positive quiescent current Negative quiescent current | $\begin{aligned} & I_{\text {Load }}=0 \\ & I_{\text {Load }}=0 \end{aligned}$ |  | $\begin{aligned} & 1.70 \\ & 5.60 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ |  | $\begin{aligned} & 1.70 \\ & 5.60 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $V_{\text {baL }}$ | Input/output differential voltage Output voltage balance Output noise voltage | 100 Hz to 10 kHz |  | $\begin{gathered} 2.5 \\ .2 \\ 55 \end{gathered}$ |  |  | $\begin{gathered} 2.5 \\ .2 \\ 55 \end{gathered}$ |  | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~V} \\ \mu \mathrm{Vrms} \\ \hline \end{gathered}$ |
| IPeak | Peak output current Temperature stability of output voltage |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  | $\underset{\mathrm{mV} /{ }^{\circ} \mathrm{C}}{\mathrm{~mA}}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd)

| PARAMETER |  | TEST CONDITIONS | SE5555 |  |  | NE5555 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\begin{array}{r} +4.8 \\ -12.5 \\ \hline \end{array}$ | $\begin{gathered} +5 \\ -12 \\ \hline \end{gathered}$ | $\begin{array}{r} +5.2 \\ -11.5 \end{array}$ | $\begin{array}{r} +4.8 \\ -12.5 \\ \hline \end{array}$ | $\begin{array}{r} +5 \\ -12 \\ \hline \end{array}$ | $\begin{array}{r} +5.2 \\ -11.5 \\ \hline \end{array}$ | V |
|  | Line regulation Load regulation | $\begin{gathered} \pm 20 \leq V_{\mathrm{IN}} \leq \pm 30 \mathrm{~V} \\ 1 \mathrm{~mA} \leq I_{\text {Load }} \leq 50 \mathrm{~mA} \\ 1 \mathrm{~mA} \leq I_{\text {Load }} \leq 200 \mathrm{~mA} \\ \hline \end{gathered}$ |  | $\begin{gathered} 100 \\ 10 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} 150 \\ 25 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline 100 \\ 10 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} 300 \\ 50 \\ 200 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Vout | Output voltage | $\begin{gathered} 1 \mathrm{~mA} \leq \mathrm{I} \leq 100 \mathrm{~mA} \\ \pm 20 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq \pm 30 \mathrm{~V} \text { over temp. } 1 \end{gathered}$ | $\begin{array}{r} +4.7 \\ -12.6 \end{array}$ | $\begin{gathered} +5 \\ -12 \end{gathered}$ | $\begin{array}{r} +5.3 \\ -11.4 \end{array}$ | $\begin{gathered} +4.7 \\ -12.6 \end{gathered}$ | $\begin{gathered} +5 \\ -12 \end{gathered}$ | $\begin{gathered} +5.3 \\ -11.4 \end{gathered}$ | $\begin{aligned} & V \\ & V \end{aligned}$ |
| $\begin{aligned} & \mathrm{I}_{\mathrm{Q}^{+}} \\ & \mathrm{I}^{-} \end{aligned}$ | Positive quiescent current Negative quiescent current | $\begin{aligned} & I_{\text {Load }}=0 \\ & I_{\text {Load }}=0 \end{aligned}$ |  | $\begin{aligned} & 1.70 \\ & 5.60 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 8.5 \end{aligned}$ |  | $\begin{aligned} & 1.70 \\ & 5.60 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 8.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $V_{\text {BAL }}$ | Input/output differential voltage Output voltage balance Output noise voltage | 100 Hz to 10 kHz |  | $\begin{gathered} 2.5 \\ .2 \\ 55 \end{gathered}$ |  |  | $\begin{gathered} 2.5 \\ .2 \\ 55 \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~V} \\ \mu \mathrm{Vrms} \\ \hline \end{gathered}$ |
| IPeak | Peak output current <br> Temperature stability of output voltage |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  |  | $\begin{gathered} 400 \\ 1 \end{gathered}$ |  | $\underset{\mathrm{mV} /{ }^{\circ} \mathrm{C}}{\mathrm{~mA}}$ |

## NOTES

1. Junction temperature range

SE prefix $-55^{\circ} \mathrm{C}<\mathrm{T}_{J}<150^{\circ} \mathrm{C}$
NE prefix $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$
2. $\mathrm{C}_{\mathrm{IN}}$ needed only when isolated from filter capacitors

Cout needed only if dynamic regulation is to be improved
3. Thermal resistance, DIP
$\theta \mathrm{JA}=95^{\circ} \mathrm{C} / \mathrm{W} \theta_{\mathrm{Jc}}=35^{\circ} \mathrm{C} / \mathrm{W}$, TO-5
$\theta_{\mathrm{JA}}=150^{\circ} \mathrm{C} / \mathrm{W} \theta_{\mathrm{JC}}=25^{\circ} \mathrm{C} / \mathrm{W}$

TYPICAL PERFORMANCE CHARACTERISTICS


## BLOCK DIAGRAM



## TYPICAL APPLICATIONS

HIGH CURRENT TRACKING REGULATOR


$$
\mathrm{R} 1=\mathrm{R} 2=\frac{\mathrm{V}_{\mathrm{BE}}}{\mathrm{I}_{\mathrm{REG}}(\max )(\beta+1)-\mathrm{I}_{\text {out }}(\max )} \text { For }
$$

$\beta(Q) \geq 1$ out (max)
Ireg (max)

## DESCRIPTION

The 550 is a precision monolithic voltage regulator capable of positive or negative supply operation as series, shunt, switching or floating regulator. Guaranteed line regulation is provided for input voltages ranging from 8.5 volts to as high as 50 volts. The output voltage can be continuously adjusted from 2 volts to 40 volts. Foldback current limiting can be accomplished through the use of one external resistor. Internal circuitry permits on and off strobing with DTL and TTL logic inputs and latched shut-down with a pulsed input.

FEATURES

- Line regulation guaranteed over input voltage range of 8.5 volts to as high as 50 volts.
- Output voltage continuously adjustable from 2 volts to 40 volts
- .01\% line and load regulation
- Adjustable limiting of short circuit current
- Foldback current limiting with one external resistor
- Remote and latching shutdown
- Output current up to 150 mA without external power transistors

CIRCUIT SCHEMATIC


## PIN CONFIGURATIONS



## EQUIVALENT CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Voltage from V+ to V- |  |  |
| SE550 | 50 | V |
| NE550 | 40 | V |
| Input-output voltage differential | 45 | V |
| SE550 | 37 | mA |
| NE550 |  | mA |
| Maximum output current | 150 | mA |
| SE550 | 150 | mA |
| NE550 | 15 | mW |
| Current from VZ | 15 | mW |
| SE550 | 800 | ${ }^{\circ} \mathrm{C}$ |
| NE550 | 800 | ${ }^{\circ} \mathrm{C}$ |
| Internal power dissipation1 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE550 | to 70 | ${ }^{\circ} \mathrm{C}$ |
| NE550 |  | ${ }^{\circ}$ |
| Operating temperature range | ${ }^{\circ} \mathrm{C}$ |  |
| SE550 | ${ }^{\circ} \mathrm{C}$ |  |
| NE550 | -65 to +150 | to +150 |
| Storage temperature range | 300 | 300 |
| SE550 |  |  |
| NE550 |  |  |
| Lead temperature |  |  |
| SE550 |  |  |
| NE550 |  |  |

1. Rating applies for case temperatures to $125^{\circ} \mathrm{C}$; derate linearly at $6.5 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for ambient termperature above $+75^{\circ} \mathrm{C}$

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. 1,2

| PARAMETER | TEST CONDITIONS | NE550 |  |  | SE550 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Line regulation | $\begin{gathered} V_{I N}=8.5 \text { to } 40 \mathrm{~V} \\ 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{IN}}=12 \text { to } 40 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=12 \text { to } 40 \mathrm{~V} \\ \mathrm{VIN}^{2}=8.5 \text { to } 50 \mathrm{~V} \\ -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}, \mathrm{~V}_{I N}=12 \text { to } 40 \mathrm{~V} \end{gathered}$ |  | . 08 | $\begin{gathered} 0.3 \\ 0.35 \end{gathered}$ |  | $\begin{gathered} 0.05 \\ 0.2 \end{gathered}$ | $\begin{gathered} 0.1 \\ 0.6 \\ 0.25 \end{gathered}$ | \%VOUT \%VOUT \%VOUT \%VOUT \%VOUT |
| Load regulation | $\begin{gathered} \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA} \text { to } 50 \mathrm{~mA} \\ 0^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq 70^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq+125^{\circ} \mathrm{C} \end{gathered}$ |  | . 03 | $\begin{aligned} & 0.2 \\ & 0.4 \end{aligned}$ |  | 0.03 | $\begin{aligned} & .10 \\ & .6 \end{aligned}$ | \%VOUT \%Vout \%VOUT |
| Ripple rejection | $\begin{gathered} f=50 \mathrm{~Hz} \text { to } 10 \mathrm{kHz} \\ \text { CREF }=0 \\ \text { CREF }=5 \mu \mathrm{~F} \end{gathered}$ |  | $\begin{aligned} & 75 \\ & 90 \end{aligned}$ |  |  | $\begin{aligned} & 75 \\ & 90 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Average temperature coefficient of output voltage | $\begin{gathered} -55^{\circ} \leq T_{A} \leq+125^{\circ} \mathrm{C} \\ 0^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq 70^{\circ} \end{gathered}$ |  | . 002 | . 015 |  | . 002 | . 012 | $\begin{aligned} & \% /{ }^{\circ} \mathrm{C} \\ & \% /{ }^{\circ} \mathrm{C} \end{aligned}$ |
| Short circuit limit | RSC $=10 \Omega, \mathrm{~V}_{\text {OUT }}=0$ | 50 | 60 | 70 | 50 | 60 | 70 | mA |
| Reference voltage Output noise voltage | $B W=100 \mathrm{~Hz}$ to $10 \mathrm{kHz}, C_{\text {REF }}=0$ <br> $B W=100 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{C}_{\text {REF }}=5 \mu \mathrm{~F}$ | 1.58 | $\begin{gathered} \hline 1.63 \\ 20 \\ 2.5 \\ \hline \end{gathered}$ | 1.73 | 1.58 | $\begin{gathered} 1.63 \\ 20 \\ 2.5 \\ \hline \end{gathered}$ | 1.68 | V $\mu$ Vrms $\mu$ Vrms |
| Long term stability |  |  |  |  |  | 0.1 |  | \%/1000hrs. |
| Standby current drain | $\begin{aligned} & I_{L}=0, V_{I N}=50 \mathrm{~V} \\ & I_{L}=0, V_{I N}=40 \mathrm{~V} \end{aligned}$ |  | 1.6 | 3.0 |  | 1.3 | 2.0 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Input voltage range Output voltage range |  | $\begin{aligned} & 8.5 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 40 \\ & 40 \end{aligned}$ | $\begin{aligned} & 8.5 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 50 \\ & 37 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Input-output voltage differential |  | 3.0 |  | 38 | 3.0 |  | 45 | V |

1. $\mathrm{V}_{1} \mathrm{~N}=\mathrm{V}+=\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}, \mathrm{RSC}=0{ }_{1} \mathrm{Cl}=100 \mathrm{pF}$, and divider impedance as seen by error amplifier $\simeq 2 \mathrm{k} \Omega$.
2. The load and line regulation specifications are for constant temperature junction. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL APPLICATIONS


## TYPICAL APPLICATIONS (Cont'd)



TYPICAL APPLICATIONS (Cont'd)



$L_{1}$ is 50 turns of \#22 wire wound on Ferroxcube. 42/29-377
A400

## TYPICAL APPLICATIONS (Cont'd)

NEGATIVE FLOATING REGULATOR


## DESCRIPTION

The $\mu$ A723/SA723C is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The 723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

## FEATURES

- Positive or negative supply operation
- Series, shunt, switching or floating operation
- $.01 \%$ line and load regulation
- Output voltage adjustable from 2 to 37 volts
- Output current to 150 mA without external pass transistor
- $\mu$ A723 MIL STD 88 3A, B, C available


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Pulse voltage from V+ to V-(50 ms ) |  |  |
| $\mu \mathrm{A} 723$ | 50 | V |
| $\mu$ A723C |  |  |
| SA723C |  |  |
| Continous voltage from $\mathrm{V}+$ to V - |  |  |
| $\mu \mathrm{A} 723$ | 40 | V |
| $\mu$ A723C | 40 | V |
| SA723C | 40 | V |
| Input-output voltage differential | 40 | V |
| Maximum output current |  |  |
| $\mu \mathrm{A} 723$ | 150 | mA |
| $\mu$ A723C | 150 | mA |
| SA723C | 150 | mA |
| Current from Vref |  |  |
| $\mu A 723$ | 15 | mA |
| $\mu A 723 C$ |  |  |
| SA723C |  |  |
| Current from VZ A723 |  |  |
| $\mu$ A723C | 25 | mA |
| SA723C | 25 | mA |
| Internal power dissipation1 |  |  |
| $\mu$ A723 | 800 | mA |
| $\mu$ A723C | 800 | mA |
| SA723C | 800 | mA |
| Operating temperature range |  |  |
| $\mu$ A723 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mu$ A723C | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| SA723C | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range |  |  |
| $\mu \mathrm{A} 723$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mu$ A723C | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| SA723C | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  |  |
| $\mu \mathrm{A} 723$ | 300 | ${ }^{\circ} \mathrm{C}$ |
| $\mu A 723 C$ | 300 | ${ }^{\circ} \mathrm{C}$ |
| SA723C | 300 | ${ }^{\circ} \mathrm{C}$ |

PIN CONFIGURATION


ORDER PART NOS. $\mu \mathrm{A} 723 \mathrm{~N}, \mu \mathrm{~A} 723 \mathrm{~F}$, $\mu A 723 C N, \mu A 723 C F, S A 723 C F$, SA723CN
L PACKAGE

EQUIVALENT CIRCUIT


DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. 1

| PARAMETER | TEST CONDITIONS | $\mu$ A723C/SA723C |  |  | $\mu$ A723 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Line regulation ${ }^{2}$ | $\begin{aligned} & V_{\text {IN }}=12 \mathrm{~V} \text { to } \mathrm{VIN}=15 \mathrm{~V} \\ & V_{\text {IN }}=12 \mathrm{~V} \text { to } V_{\text {IN }}=40 \mathrm{~V} \end{aligned}$ |  | $\begin{gathered} 0.01 \\ 0.1 \end{gathered}$ | $\begin{aligned} & 0.1 \\ & 0.5 \end{aligned}$ |  | $\begin{aligned} & 0.01 \\ & 0.02 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.2 \end{aligned}$ | \%Vout \%Vout |
| Load regulation ${ }^{2}$ | $\begin{gathered} I_{L}=1 \mathrm{~mA} \text { to } I_{L}=50 \mathrm{~mA} \\ f=50 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}, C_{\text {REF }}=0 \\ f=50 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}, C_{\text {REF }}=5 \mu \mathrm{~F} \end{gathered}$ |  | $\begin{gathered} 0.03 \\ 74 \\ 86 \\ \hline \end{gathered}$ | 0.2 |  | $\begin{array}{c\|} \hline 0.03 \\ 74 \\ 86 \\ \hline \end{array}$ | 0.15 | $\begin{gathered} \hline \text { \%VOUT } \\ d B \\ d B \\ \hline \end{gathered}$ |
| Short circuit current limit | RSC $=10 \Omega$, V ${ }_{\text {OUT }}=0$ |  | 65 |  |  | 65 |  | mA |
| Reference voltage Output noise voltage | $\begin{aligned} & \mathrm{BW}=100 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}, \mathrm{C}_{\text {REF }}=0 \\ & \mathrm{BW}=100 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}, \mathrm{C}_{\text {REF }}=5 \mu \mathrm{~F} \end{aligned}$ | 6.80 | $\begin{gathered} \hline 7.15 \\ 20 \\ 2.5 \\ \hline \end{gathered}$ | 7.50 | 6.95 | $\begin{gathered} \hline 7.15 \\ 20 \\ 2.5 \\ \hline \end{gathered}$ | 7.35 |  |
| Long term stability Standby current drain | $\mathrm{I}_{L}=0, \mathrm{~V}_{1}=30 \mathrm{~V}$ |  | $\begin{array}{r} \hline 0.1 \\ 2.3 \\ \hline \end{array}$ | $\begin{aligned} & 0.1 \\ & 4.0 \\ & \hline \end{aligned}$ | 2.3 | $\begin{aligned} & 0.1 \\ & 3.5 \\ & \hline \end{aligned}$ |  | $\begin{array}{\|c\|} \hline \% / 1000 \mathrm{hrs} . \\ \mathrm{mA} \\ \hline \end{array}$ |
| Input voltage range Output voltage range |  | $\begin{aligned} & 9.5 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 40 \\ & 37 \\ & \hline \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 40 \\ & 37 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Input-output voltage differential |  | 3.0 |  | 38 | 3.0 |  | 38 | V |
| The following specifications apply over the operating temperature ranges <br> Line regulation |  |  |  | 0.3 |  |  | 0.3 | \%Vout |
| Load regulation |  |  |  | 0.6 |  |  | 0.6 | \%VOUT |
| Average temperature coefficient of output voltage | $\begin{aligned} & V_{I N}=12 \mathrm{~V} \text { to } V_{I N}=15 \mathrm{~V} \\ & I_{L}=1 \mathrm{~mA} \text { to } I_{\mathrm{L}}=50 \mathrm{~mA} \end{aligned}$ |  | 0.003 | 0.015 |  | 0.002 | 0.015 | \%/ ${ }^{\circ} \mathrm{C}$ |

## NOTES

1. $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}+=\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}, \mathrm{R}_{\mathrm{SC}}=0, \mathrm{C}_{1}=100 \mathrm{pF}, \mathrm{C}_{\mathrm{REF}}=0$ and divider impedance as seen by error amplifier $\leq 10 \mathrm{k} \Omega$ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL APPLICATIONS


## TYPICAL APPLICATIONS (Cont'd)




HIGH VOLTAGE REGULATOR (V OUT $=7$ TO 37 VOLTS)

$v_{\text {out }}=\left[V_{\text {REF }} \times \frac{R_{1}+R_{2}}{R_{2}}\right]$
$R_{3}=\frac{R_{1} R_{2}}{R_{1}+R_{2}}$ for minimum temperature drift
$R_{3}$ may be eliminated for minimum component count

## DESCRIPTION

The $\mu$ A78L00 series of 3-Terminal Positive Voltage Regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on card regulation for elimination of noise and distribution problems associated with single point regulation. In addition, they can be used with power pass elements to make high current voltage regulators. The $\mu$ A78L00 used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

## FEATURES

- Output curent up to 100 mA
- No external components
- Internal thermal overload protection
- Internal short circuit current limiting
- Available in JEDEC TO-92 and low profile TO-39 packages
- Output voltages of $2.6 \mathrm{~V}, 5 \mathrm{~V}, 6.2 \mathrm{~V}, 8.2 \mathrm{~V}$, 12 V and 15 V
- Output voltage tolerances or $\pm 5 \%$ (78LOO-A) and $\pm 10 \%$ ( 78 LOO ) over the temperature range


## EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Input voltage |  |  |
| $2.6 \mathrm{~V}, 5 \mathrm{~V}, 6.2 \mathrm{~V}$ and 8.2V | 30 | V |
| 12 V and 15 V ( | 35 | V |
| Internal power dissipation | Internally limited |  |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Metal can (TO-39 type) | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Molded TO-92 | 0 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating junction temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperatures | ${ }^{\circ} \mathrm{C}$ |  |
| Metal can (soldering, 60s time limit) | 260 |  |
| Molded TO-92 (soldering, 10s time limit) |  |  |

## CONNECTION DIAGRAMS



DC ELECTRICAL CHARACTERISTICS
IOUT $=40 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{COUT}=0.1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78L02AC |  |  | 78L02C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\mathrm{V}_{\text {IN }}=9.0 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=9.0 \mathrm{~V}$ |  |  |  |
|  |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $\begin{aligned} & 2.5\|2.6\| \\ & 4.75 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V} \end{aligned}$ |  |  | $\begin{array}{c\|c\|c} 2.4 & 2.6 \\ 4.75 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V} \end{array}$ |  |  | v |
|  |  |  |  |  |  |  |  |
|  |  | $1 \mathrm{~mA} \leq$ lout $\leq 70 \mathrm{~mA}$ | $\left.\begin{aligned} & 4.75 \mathrm{~V} \leq \mathrm{VIN}^{5} \leq 20 \mathrm{~V} \\ & 2.45 \end{aligned} \right\rvert\, \begin{aligned} & 2.75 \end{aligned}$ |  |  |  |  |  | 2.35 |  | 2.85 | v |
|  |  | $1 \mathrm{~mA} \leq$ lout $\leq 40 \mathrm{~mA}$ | 2.45 |  | 2.75 | 2.35 |  | 2.85 | v |
|  | Line regulation | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\begin{gathered} 4.75 \leq V_{\text {IN }} \leq 20 \mathrm{~V} \\ 40 \mid 100 \\ 5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 4.75 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V} \\ 40 \quad \mid 125 \\ 5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V} \end{gathered}$ |  |  |  |
|  |  |  |  |  |  | mV |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  | 30 | 75 |  |  |  |  | 30 | 100 | mV |
|  | Load regulation | $\begin{gathered} 1 \mathrm{~mA} \leq \text { lout } \leq 100 \mathrm{~mA}, T_{J}=25^{\circ} \mathrm{C} \\ 1 \mathrm{~mA} \leq \text { Iout } \leq 40 \mathrm{~mA}, \mathrm{TJ}_{J}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 10 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ |  |  |  |  | $\begin{aligned} & \hline 10 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{~mW} \end{aligned}$ |
| Icc |  | $\begin{aligned} & T_{J}=25^{\circ} \mathrm{C} \\ & T_{J}=125^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ |  | 3.6 | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ |  | 3.6 | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\Delta \mathrm{lcc}$ |  | With line <br> With load, $1 \mathrm{~mA} \leq$ lout $\leq 40 \mathrm{~mA}$ | $5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V}$ |  |  | $5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V}$ |  |  |  |
|  |  |  |  | $\begin{aligned} & 2.5 \\ & 0.1 \end{aligned}$ |  |  | $\begin{aligned} & 2.5 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |  |
| Output noise voltage |  |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 30 |  |  | 30 |  | $\mu \mathrm{V}$ |
| Long term stability |  |  |  | 10 |  |  | 10 |  | mV |
| Ripple rejection |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{f}=120 \mathrm{~Hz}$ | $6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 16 \mathrm{~V}$ |  |  | $6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 16 \mathrm{~V}$ |  |  |  |
|  |  | 43 | 51 |  | 42 | 51 |  | dB |  |
| Dropout voltage |  |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.7 |  |  | 1.7 |  | V |
| Vout | Output temperature drift | lout $=5 \mathrm{~mA}$ |  | -0.4 |  |  | -0.4 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Isc |  | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 140 |  |  | 140 |  | mA |

DC ELECTRICAL CHARACTERISTICS (Cont'd)

| PARAMETER |  | TEST CONDITIONS | 78L05AC |  |  | 78L05C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $\begin{gathered} 4.8 \mid{ }_{2.0} 5.0 .2 \\ 7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V} \end{gathered}$ |  |  | $4.6 \|$$7 \mathrm{~V} \leq \mathrm{V}$ IN $\leq 20 \mathrm{~V}$ |  |  | V |
|  |  | $\begin{gathered} 1 \mathrm{~mA} \leq \text { lout } \leq 70 \mathrm{~mA} \\ 1 \mathrm{~mA} \leq \text { lout } \leq 40 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & 4.75 \\ & 4.75 \end{aligned}$ |  | $\begin{aligned} & 5.25 \\ & 5.25 \end{aligned}$ |  |  | $\begin{aligned} & 5.50 \\ & 5.50 \end{aligned}$ | v |
|  | Line regulation | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $\begin{aligned} & 7 V \leq V_{\text {IN }} \leq 20 \mathrm{~V} \\ & \mid=155 \\ & 8 \mathrm{~V} \leq V_{\text {IN }} \leq 20 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & 7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{N}} \leq 20 \mathrm{~V} \\ & \mid=5 \\ & 8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V} \end{aligned}$ |  |  | $\mathrm{mV}$ |
|  |  |  |  | 45 | 100 |  | 45 | 150 | mV |
|  | Load regulation | $\begin{gathered} 1 \mathrm{~mA} \leq \text { lout } \leq 100 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ 1 \mathrm{~mA} \leq \text { IouT } \leq 40 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ \hline \end{gathered}$ |  | $\begin{aligned} & 11 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 60 \\ & 30 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 11 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 60 \\ & 30 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{~mW} \end{aligned}$ |
| Icc |  | $\begin{gathered} T_{J}=25^{\circ} \mathrm{C} \\ T_{J}=125^{\circ} \mathrm{C} \end{gathered}$ |  | 3.8 | $\begin{aligned} & 6.0 \\ & 5.5 \\ & \hline \end{aligned}$ |  | 3.8 | $\begin{aligned} & 6.0 \\ & 5.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\Delta \mathrm{lcc}$ |  | With line <br> With load, $1 \mathrm{~mA} \leq$ lout $\leq 40 \mathrm{~mA}$ |  | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} \hline 20 \mathrm{~V} \\ 1.5 \\ 0.1 \\ \hline \end{gathered}$ |  | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} \hline 20 \mathrm{~V} \\ 1.5 \\ 0.2 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Output noise voltage |  | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 40 |  |  | 40 |  | $\mu \mathrm{V}$ |
| Long term stability |  |  |  | 12 |  |  | 12 |  | mV |
| Ripple rejection |  | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{f}=120 \mathrm{~Hz}$ | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 18 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 18 \mathrm{~V}$ |  |  | dB |
| Dropout voltage |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.7 |  |  | 1.7 |  | V |
| Vout Output temperature drift |  | lout $=5 \mathrm{~mA}$ |  | -0.65 |  |  | -0.65 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
|  |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 140 |  |  | 140 |  | mA |

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=40 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=0.1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78L06AC |  |  | 78L06C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}$ |  |  | V |
|  |  | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $5.95\|6.2\| 6.45$$8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V}$ |  |  | $\begin{array}{c\|c\|c} 5.7 & 6.2 & 6.7 \\ 8.5 \mathrm{~V} \leq \mathrm{V} \mathrm{~N} \leq 20 \mathrm{~V} \end{array}$ |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  | $1 \mathrm{~mA} \leq$ IOUT $\leq 70 \mathrm{~mA}$ | 5.90 |  | 6.50 | 5.60 |  | 6.80 | V |  |
|  |  | $1 \mathrm{~mA} \leq 1$ OUT $\leq 40 \mathrm{~mA}$ | 5.90 |  | 6.50 | 5.6 |  | 6.8 | V |  |
|  | Line regulation | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $8.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V}$ |  |  | $8.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V}$ |  |  |  |  |
|  |  |  |  | 65 | 175 | $9 V \leq V_{I N} \leq 20 V$ |  |  | mV |  |
|  |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V}$ |  |  |  |  |  |  |  |
|  |  |  |  | 55 | 125 |  | 55 | 150 | mV |  |
|  | Load regulation | $\begin{gathered} 1 \mathrm{~mA} \leq \mathrm{IOUT} \leq 100 \mathrm{~mA}, T_{J}=25^{\circ} \mathrm{C} \\ 1 \mathrm{~mA} \leq \text { IOUT } \leq 40 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 13 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 80 \\ & 40 \end{aligned}$ |  | $\begin{aligned} & 13 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 80 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |  |
| ICC |  | $\begin{gathered} T_{J}=25^{\circ} \mathrm{C} \\ T_{J}=125^{\circ} \mathrm{C} \end{gathered}$ |  | 3.9 | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ |  | 3.9 | $\begin{aligned} & \hline 6.0 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{~mA} \end{aligned}$ |  |
| $\Delta \mathrm{lcC}$ |  | With line <br> With load, $1 \mathrm{~mA} \leq$ lout $\leq 40 \mathrm{~mA}$ | $9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V}$ |  |  | $9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V}$ |  |  |  |  |
|  |  |  |  | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ |  |  | 1.5 0.2 | $\mathrm{mA}$ $\mathrm{mA}$ |  |  |
| Output noise voltage |  |  | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 50 |  |  | 50 | $\mu \mathrm{A}$ |  |
| Long term stability |  |  |  | 14 |  |  | 14 |  | mV |  |
| Ripple rejection |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{f}=120 \mathrm{~Hz}$ | $10 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V}$ |  |  | $10 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V}$ |  |  |  |  |
|  |  | 40 | 46 |  | 39 | 46 |  | dB |  |  |
|  | Dropout voltage |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.7 |  |  | 1.7 |  | V |
| VOUT | Output temperature drift | IOUT $=5 \mathrm{~mA}$ |  | -0.75 |  |  | -0.75 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |  |
| Isc |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 140 |  |  | 140 |  | mA |  |

DC ELECTRICAL CHARACTERISTICS (Cont'd)

| PARAMETER |  | TEST CONDITIONS | 78L08AC |  |  | 78L08C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$ |  |  | V |
|  |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $\begin{aligned} & 7.87\|8.2\| 8.53 \\ & 11 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 23 \mathrm{~V} \end{aligned}$ |  |  | $7.54\|8.20\| 8.86$$11 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 23 \mathrm{~V}$ |  |  |  |  |
|  |  | $\begin{aligned} & 1 \mathrm{~mA} \leq \text { IOUT } \leq 70 \mathrm{~mA} \\ & 1 \mathrm{~mA} \leq \text { IOUT } \leq 40 \mathrm{~mA} \end{aligned}$ |  |  |  |  |  |  |  |  |
|  |  |  | 7.8 |  | 8.60 | 7.40 |  | 9.0 | V |  |
|  |  |  | 7.8 |  | 8.6 | 7.40 |  | 9.0 | V |  |
|  | Line regulation | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $11 V^{\prime} \leq V_{\text {IN }} \leq 23 V$$80 \mid 175$$12 V \leq V_{\text {IN }} \leq 23 V$ |  |  | $11 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 23 \mathrm{~V}$$\left.\left\lvert\, \begin{array}{c\|c}80 & 200 \\ 12 \mathrm{~V} & \leq \mathrm{V}_{\text {IN }} \leq 23 \mathrm{~V}\end{array}\right.\right)$ |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 70 | 125 |  | 70 | 150 |  |  |
|  | Load regulation | $\begin{gathered} 1 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 100 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ 1 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{OUT}} \leq 40 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ \hline \end{gathered}$ | , | $\begin{aligned} & 15 \\ & 8.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 80 \\ & 40 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 90 \\ & 45 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |  |
| ICC |  | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J}=125^{\circ} \mathrm{C} \end{gathered}$ |  | 3.9 | $\begin{aligned} & 6.0 \\ & 5.5 \\ & \hline \end{aligned}$ |  | 4.2 | $\begin{aligned} & 6.5 \\ & 6.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{~mA} \end{aligned}$ |  |
| $\Delta \mathrm{lcc}$ |  | With line <br> With load, $1 \mathrm{~mA} \leq$ lout $\leq 40 \mathrm{~mA}$ | $12 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 23 \mathrm{~V}$ |  |  | $12 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 23 \mathrm{~V}$ |  |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |  |
|  |  |   <br>   <br>  0.1 |  1.5 <br>  0.2 |  |  |  |  |  |  |  |
|  | Output noise voltage |  | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 60 |  |  | 60 |  | $\mu \mathrm{A}$ |
|  | Long term stability |  |  | 19 |  |  | 19 |  | mV |  |
|  | Ripple rejection | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{f}=120 \mathrm{~Hz}$ | $12 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 22 \mathrm{~V}$ |  |  | $12 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 22 \mathrm{~V}$ |  |  | dB |  |
|  |  |  | 39 | 45 |  | 38 | 49 |  |  |  |
|  | Dropout voltage | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.7 |  |  | 1.7 |  | V |  |
| Vout | Output temperature drift | IOUT $=5 \mathrm{~mA}$ |  | -0.8 |  |  | -0.8 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |  |
| Isc |  | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 140 |  |  | 140 |  | mA |  |

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=40 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=0.1 \mu \mathrm{~F}$ unless otherwise specified.


DC ELECTRICAL CHARACTERISTICS (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS


## HIGH DISSIPATION APPLICATION



When it is necessary to operate a $\mu \mathrm{A} 78 \mathrm{~L} 00$ regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total dissipation between R1 and the regulator.
R1 may be calculated from

$$
\begin{gathered}
R 1=\begin{array}{l}
V_{\text {IN }}(M I N)-V_{O U T}-2.0 V \\
\\
I_{L(M A X)}+I_{Q}
\end{array}
\end{gathered}
$$

where $I Q$ is the regulator quiescent current.
Regulator power dissipation at maximum input voltage and maximum load current is now

$$
P_{D}(\text { MAX })=\left(V_{1}-V_{\text {OUT }}\right) I_{L(M A X}+V_{1} I_{Q}
$$

where

$$
V_{1}=V_{I N}(M A X)-\left(I L(M A X)+I_{Q}\right) R 1
$$

The presence of R1 will affect load regulation according to the equation:
$\begin{array}{ll}\text { load regulation } & =\text { load regulation } \\ \left.\text { (at constant } V_{I N}\right) & \text { (at constant } V_{1} \text { ) }\end{array}$

+ (line regulation, mV per V ) X (R1) $\mathrm{X}(\Delta \mathrm{l})$.
As an example, consider a 15 V regulator with a supply voltage of $30 \pm 5 \mathrm{~V}$, required to supply a maximum load current of 30 mA . 1 Q is 4.3 mA , and minimum load current is to be 10 mA .

$$
\mathrm{R} 1=\frac{25-15-2}{30+4.3} \frac{8}{34.3}=240 \Omega
$$

$$
V_{1}=35-(30+4.3) .24=35-8.2=26.8 \mathrm{~V}
$$

$$
P_{D}(\mathrm{MAX})=(26.8-15) 30+26.8
$$

$$
=354+115
$$

$=470 \mathrm{~mW}$, which will permit operation up to $70^{\circ} \mathrm{C}$ in most applications.


Line regulation of this circuit is typically 110 mV for an input range of $25-35 \mathrm{~V}$ at a constant load current, i.e. $11 \mathrm{mV} / \mathrm{V}$.

Load regulation $=$ constant $\mathrm{V}_{1}$ load regulation (typically $10 \mathrm{mV}, 10-30 \mathrm{~mA} / \mathrm{L}$ ) $+(11 \mathrm{mV} / \mathrm{V}) \times 0.24 \times 20 \mathrm{~mA}$ (typically 53 mV )
$=63 \mathrm{mV}$ for a load current change of 20 mA at a constant Vin of 30V.

## THERMAL CONSIDERATIONS

The TO-92 molded package is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1 cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.
An explanation of the thermal paths of the TO-92 and comparison of the thermal equivalent circuit of the TO-39 metal package with that of the TO-92 will allow the designer to determine the thermal stress he is applying in any give application.

## THE METAL CAN THERMAL MODEL

In the TO-39 case, where the die is attached directly to the base of a metal package, the thermal equivalent circuit is often represented simply as a series connection of the juntion-to-case thermal resistance, $\theta \mathrm{Jc}$, and the case-to-ambient thermal resistance, $\theta C A$, as shown in Figure 1.
In this model, the current source represents the thermal energy source; $T J$ is the junction temperature, assuming a constant surface temperature across the die; $\theta \mathrm{Jc}$ is the junction-to-case thermal resistance, measured at a point on the case directly beneath the die location; $\theta C A$ is the thermal resistance from the case to the ultimate heat sink, ambient temperature, as represented by the battery. The heat flow is analogous to electrical current, and temperature to voltage. The total thermal resistance from junction to ambient is then:

$$
\theta \mathrm{JA}=\theta \mathrm{JC}+\theta \mathrm{CA}
$$

The maximum power dissipation is a function of the maximum permissible junction temperature (which is a function of the package materials and construction) and the total thermal resistance from the junction to ambient temperature. Junction temperature is assumed to the limiting factor.

$$
\begin{aligned}
& \text { Thus: maximum power dissipation } \\
& \qquad \begin{array}{l}
P_{D}=\frac{T_{J(M A X)}-T_{A}}{\theta_{J C}+\theta_{C A}} \\
\text { Since } \\
\text { then } \quad \theta_{J A}=\theta_{J C}+\theta_{C A} \\
\theta J A
\end{array} \\
& \text { or } \quad T_{J(M A X)}-T_{A} \\
& P_{D}
\end{aligned} \theta_{J A} P_{D}=T_{J}-T_{A} .
$$

Therefore, using the $V_{B E}$ method of junction temperature sensing, and attaching a thermocouple to the case at the location specified, the relative values of $\theta \mathrm{Jc}$, and $\theta \mathrm{CA}$ can readily be determined.
The thermal ratings of the metal can package are normally presented with the case attached to an infinite heat sink at still air ambient temperature. This causes $\theta \mathrm{CA}$ to go to zero resulting in $\theta \mathrm{Jc}$ representing the total $\theta \mathrm{JA}$. The infinite heat sink is an unrealizable condition in the practical world, but serves to project a goal.

## THE TO-92 PACKAGE

The TO-92 package thermal paths are considerably more complex than those of the TO-39 metal can package. In addition to the path through the molding compound to ambient temperature, there is another path through the leads in parallel with the case path, to ambient temperature, as shown in Figure 2.

The total thermal resistance in this model is then:

$$
\theta_{\mathrm{JA}}=\frac{\left(\theta_{\mathrm{JC}}+\theta_{\mathrm{CA}}\right)\left(\theta_{\mathrm{JL}}+\theta_{\mathrm{LA}}\right)}{\theta_{\mathrm{JC}}+\theta_{\mathrm{CA}}+\theta_{\mathrm{JL}} \theta_{\mathrm{LA}}}
$$

Where: $\quad \theta_{\mathrm{Jc}}=$ thermal resistance of the case between the regulator die and a point on the case directly above the die location.
$\theta C A=$ thermal resistance between the case and air at ambient temperature.
$\theta_{\mathrm{JL}}=$ thermal resistance from transistor die through the collector lead to a point $1 / 16^{\prime \prime}$ below the regulator case.
$\theta \mathrm{LA}=$ total thermal resistance of the collector-baseemitter leads to ambient temperature.

As one can see from Figure 1, the metal can package generally does not have the lead cooling path because of the high thermal resistances resulting from the construction of the header, case and leads. Normally, this material is kovar. Now, $\theta_{\mathrm{JC}}$ and $\theta_{\mathrm{JL}}$ are within the package and not variable by the user. However, $\theta$ CA and $\theta$ LA are outside the package and can be effectively used to control the total thermal resistance and, therefore, junction temperature.

Replacing $\theta_{J A}$ of equation (1) with $\theta_{J A}$ equation (3) gives:

$$
\theta_{J A}=\frac{\left(\theta_{J \mathrm{C}}+\theta_{\mathrm{CA}}\right)\left(\theta_{\mathrm{JL}} \alpha \theta_{\mathrm{LA}}\right)}{\theta_{\mathrm{JC}}+\theta_{\mathrm{CA}}+\theta_{\mathrm{JL}}+\theta_{\mathrm{LA}}} \frac{\mathrm{~T}_{\mathrm{J}}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}}
$$

The maximum $T_{J}$ allowed in equation (4) is $150^{\circ} \mathrm{C}$. The maximum power dissipation is determined by the net total thermal resistance $\theta J A$, the parallel equivalent networks of the case series path and lead series path, divided into the difference of the maximum junction temperature, $150^{\circ} \mathrm{C}$, and ambient temperature generally specified as $25^{\circ} \mathrm{C}$. In the case of the 78LXX, the maximum dissipation of a .4 inch condition is:

$$
\begin{aligned}
& P_{D}=\frac{150-25}{\theta_{J A}}, \theta j \mathrm{JA}=180^{\circ} \mathrm{C} / \mathrm{W} \\
& P_{D}=0.7 \mathrm{~W}
\end{aligned}
$$

If lead length is reduced to .125 inch $\theta \mathrm{JA}$ becomes $160^{\circ} \mathrm{C}$, and $\mathrm{PD}_{\mathrm{D}}(\mathrm{MAX})=0.78 \mathrm{~W}$.

## METHODS OF HEAT SINKING

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small $72^{\circ} \mathrm{C} / \mathrm{W}$ flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the $\theta_{C A}$ (Figure 2) and the new thermal resist-
ance, $\theta J A$, is:
$\theta_{\mathrm{JA}}=145^{\circ} \mathrm{C} / \mathrm{W}$ (assuming .125 inch lead length)


Figure 2

The net change of $15^{\circ} \mathrm{C} / \mathrm{W}$ increases the allowable power dissipation to 0.86 W with an inserted cost of 1-2 cents. A still further decrease in $\theta$ JA could be achieved by using a sink rated at $46^{\circ} \mathrm{C} / \mathrm{W}$, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total $\theta_{\mathrm{JA}}$, the other external thermal resistance, $\theta$ LA,
may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, $\theta$ SA, from the leads at the mounting point to ambient, that is, the mouriting medium, $\theta$ LA is then equal to $\theta$ LS + $\theta \mathrm{SA}$. The new model is shown in Figure 3.


Figure 3
In the case of a socket, $\theta$ SA could be as high as $270^{\circ} \mathrm{C} / \mathrm{W}$, thus causing a net increase in $\theta$ JA and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net $\theta$ JA to the original value, but lead sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the leads. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additonal resistors are not significantly effective; beyond some point, additional copper area is not effective.

## DESCRIPTION

The 78M00 series of monolithic Three Terminal Positive Voltage Regulators employs internal current limiting, thermal shut down, and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, the device can deliver over 500 mA output current. They are intended as fixed voltage regulators, but used with external components, can provide adjustable output voltages and currents.

FEATURES

- Output current up to 500 mA
- No external components
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Available in the TO-220 and the TO-39 package
- Output voltages of $\mathbf{5 , 6 , 8}, 12,15,20$, and 24 volts


## SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Input voltage ( 5 V through 15 V ) $(20 \mathrm{~V}, 24 \mathrm{~V}) 1$ <br> Internal power dissipation <br> Storage temperature range <br> TO-39 TO-220 <br> Operating junction temperature range ${ }^{2}$ <br> 78M00 <br> SA78M00C <br> 78M00C <br> Lead temperature <br> TO-39 package (soldering, 60 second time limit) TO-220 package (soldering, 10 second time limit) | $\begin{gathered} 35 \\ 40 \\ \text { Internally limited } \\ -65 \text { to }+150 \\ -55 \text { to }+125 \\ \\ -55 \text { to }+150 \\ -40 \text { to }+125 \\ 0 \text { to }+125 \\ 300 \\ 230 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} \end{gathered}$ |

## NOTES

1. Thermal resistance of the packages (without a heat sink)

Junction to case: TO-220 package $2^{\circ} \mathrm{C} / \mathrm{W}$ TO-39 package $20^{\circ} \mathrm{C} / \mathrm{W}$.
Junction to ambient: TO-220 package $50^{\circ} \mathrm{C} / \mathrm{W}$ TO-39 package $170 \mathrm{C} / \mathrm{W}$.
2. Operating ambient temperature range
$78 \mathrm{M} 00 \quad-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
SA78M00C $\quad-40^{\circ} \mathrm{C}$ to $-125^{\circ} \mathrm{C}$
$78 \mathrm{MOOC} \quad 0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

## PIN CONFIGURATIONS

## OUTPUT vOLTAGE

78M05CU/SA78M05 $8 \mathrm{~V} \quad 78 \mathrm{M06CU} / \mathrm{SA} 78 \mathrm{M} 06 \mathrm{CU}$ $12 \mathrm{~V} \quad 78 \mathrm{M} 12 \mathrm{CU} / \mathrm{SA} 78 \mathrm{M} 12 \mathrm{CU}$ 15 V 78M15CU/SA78M15CU 78M20CU/SA78M20CU 78M24CU/SA78M24CU

DB PACKAGE (TO-39)


| OUTPUT <br> VOLTAGE | ORDER <br> PART NO. |
| :---: | :--- |
| 5 V | 78 M 05 DB |
| 6 V | 78 M 06 DB |
| 8 V | 78 M 08 DB |
| 12 V | 78 M 12 DB |
| 15 V | 78 M 15 DB |
| 20 V | 78 M 20 DB |
| 24 V | 78 M 24 DB |
| 5 V | 78 M 05 CDB |
| 6 V | 78 M 06 CDB |
| 8 V | 78 M 08 CDB |
| 12 V | 78 M 12 CDB |
| 15 V | 78 M 15 CDB |
| 20 V | 78 M 20 CDB |
| 24 V | 78 M 24 CDB |

## DC ELECTRICAL CHARACTERISTICS

Iout $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}$, Cout $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.


DC ELECTRICAL CHARACTERISTICS
(Cont'd)

| PARAMETER |  | TEST CONDITIONS | 78M061 |  |  | 78M06C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{IN}}=11 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=11 \mathrm{~V}$ |  |  | V |
|  |  | 5.75 |  | 6.0 | 6.25 | 5.75 |  | 6.25 |  |  |
|  |  | $9 \mathrm{~V} \leq \mathrm{VIN} \leq 21 \mathrm{~V}$ |  |  | $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 21 \mathrm{~V}$ |  |  |  |  |
|  |  | 5.7 |  |  | 6.3 | 5.7 |  | 6.3 | V |  |
|  | Line regulation | $\mathrm{IOUT}=200 \mathrm{~mA}$ |  |  |  |  | $\begin{gathered} 8 \mathrm{~V} \leq \mathrm{VIN}_{\mathrm{IN}} \leq 25 \mathrm{~V} \\ 5 \\ 9 \mathrm{~V} \leq \mathrm{VIN}^{2} \leq 25 \mathrm{~V} \\ 1.5 \end{gathered}$ |  |  |  |
|  |  |  | mV |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 1.5 | 30 | mV |  |  |  |  |  |
|  | Load regulation | $5 \mathrm{~mA} \leq$ IOUT $\leq 500 \mathrm{~mA}$ |  | 20 | 60 |  | 20 | 120 | mV |  |
|  |  | $5 \mathrm{~mA} \leq$ lout $\leq 200 \mathrm{~mA}$ |  | 10 | 30 |  | 10 | 60 | mV |  |
| Icc |  |  |  | 4.5 | 6.0 |  | 4.5 | 8.0 | mA |  |
| $\Delta \mathrm{lcc}$ <br> $\Delta \mathrm{lcc}$ | With line | Over temp., Iout $=200 \mathrm{~mA}$ | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |  |
|  |  |  |  |  | 0.8 |  0.8 <br>  0.5 |  |  | mA |  |
|  | With load | $5 \mathrm{~mA} \leq$ IOUT $\leq 350 \mathrm{~mA}$ |  |  | 0.5 |  |  |  | mA |  |
| Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 45 |  |  | 45 |  | $\mu \mathrm{V}$ |  |
| Voltage drift |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 24 |  |  | 24 | mV |  |
| Ripple rejection |  | Over temp., $\mathrm{f}=120 \mathrm{~Hz}$ | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 19 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\mathbb{N}} \leq 19 \mathrm{~V}$ |  |  |  |  |
| Dropout voltage |  |  | 59 | 80 |  | 59 | 80 |  | dB |  |
|  |  |  |  | 2.0 |  |  | 2.0 |  | V |  |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 270 |  |  | 270 |  | mA |  |
| Peak output current |  |  |  | 700 |  |  | 700 |  | mA |  |
| Vout | Output temperature drift | $\mathrm{IOUT}=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}^{\prime} \leq 150^{\circ} \mathrm{C}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |  |

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78M081 |  |  | 78M08C1 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $5 \mathrm{~mA} \leq$ IOUT $\leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ |  |  | V |
|  |  | 7.7 |  | 8.0 | 8.3 |  | 8.0 | 8.3 |  |  |
|  |  | $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 23 \mathrm{~V}$ |  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 23 \mathrm{~V}$ |  |  |  |  |
|  |  | 7.6 |  |  | 8.4 | 7.6 |  | 8.4 | V |  |
|  | Line regulation | IOUT $=200 \mathrm{~mA}$ |  | $\begin{gathered} 10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V} \\ \mid \quad 6 \\ 11 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V} \end{gathered}$ |  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | mV |
|  |  |  | $11 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | 2 | 30 |  | 2 | 50 | mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq 1 \text { OUT } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq 1 \text { OUT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 80 \\ & 40 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{gathered} 160 \\ 80 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |  |
| Icc |  |  |  <br> $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  |  | 4.6 | 6.0 | mA |  |
| $\Delta \mathrm{ICC}$ <br> $\Delta \mathrm{lcc}$ | With line | Over temp., IOUT $=200 \mathrm{~mA}$ | $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  |  |  |
|  |  |  |  |  | $0.8$ |  |  | 0.8 | mA |  |
|  | With load | $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ |  |  | $0.5$ |  |  | 0.5 | mA |  |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 52 |  |  | 52 |  | $\mu \mathrm{V}$ |  |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 32 |  |  | 32 | mV |  |
| Ripple rejection |  | Over temp., $\mathrm{f}=120 \mathrm{~Hz}$ | $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 21.5 \mathrm{~V}$ |  |  | $11.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 21.5 \mathrm{~V}$ |  |  |  |  |
|  |  | 56 | 80 |  | 56 | 80 |  | dB |  |  |
|  | Dropout voltage |  |  |  | 2.0 |  |  | 2.0 |  | V |
| ISC |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 250 |  |  | 250 |  | mA |  |
|  | Peak output current |  |  | 700 |  |  | 700 |  | mA |  |
| VOUT Output temperature drift |  | IOUT $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \\ -0.5 \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \mid \\ \|-0.5\| \\ \hline \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |  |

## DC ELECTRICAL CHARACTERISTICS (Cont'd)

| PARAMETER |  | TEST CONDITIONS | 78M12 ${ }^{1}$ |  |  | 78M12C ${ }^{1}$ |  |  | 78M151 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\text {IN }}=19 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=19 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=23 \mathrm{~V}$ |  |  |  |
|  |  | 11.5 |  |  | 12.5 | 11.5 |  | 12.5 | 14.4 |  | 15.6 | v |
|  |  | $\begin{aligned} & 15.5 \mathrm{~V} \leq \mathrm{V}_{\text {I }} \leq 27 \mathrm{~V} 14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 27 \mathrm{~V} \\ & 11.4\|12.6\| 11.4 \mid \end{aligned}$ |  |  |  |  |  | $\begin{gathered} 18.5 \mathrm{~V} \leq \mathrm{V}_{\mathbb{N}} \leq 30 \mathrm{~V} \\ 14.5 \mid 15.75 \end{gathered}$ |  |  |  |  |
|  | Line regulation | $104 T=200 \mathrm{~mA}$ |  |  |  |  |  |  |  | $\begin{array}{\|c} 17.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ \|10\| 60 \\ 20 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \end{array}$ |  |  |  |
|  |  | 住 $=200 \mathrm{~mA}$ | mV |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | mV |  |  |  |  |  |  |  |  |  |  |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { IouT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 120 \\ & 60 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{gathered} 150 \\ 75 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.8 | 6.0 |  4.8 6.0 <br> $14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$   |  |  |  4.8 6.0 <br> $18.5 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 30 \mathrm{~V}$   |  |  | mA |
| SICC <br> $\Delta I c c$ | With line | $\begin{gathered} \text { Over temp., Iout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { Iout } \leq 350 \mathrm{~mA} \end{gathered}$ | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $18.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  |  |  |  |  | 0.8 |  |  | 0.8 |  |  | 0.8 |  |
|  | With load |  |  |  | 0.5 |  |  | 0.5 |  |  | 0.5 |  |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 75 |  |  | 75 |  |  | 90 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 48 |  |  | 48 |  |  | 60 | mV |
| Ripple rejection |  | Over temp., $\mathrm{f}=120 \mathrm{~Hz}$ | $\begin{aligned} & 15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V} \\ & 55 \\ & \hline 0 \end{aligned}$ |  |  | $\begin{aligned} & \begin{array}{l} 15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V} \\ 55 \\ 55 \\ \hline \end{array} \\ & \hline \end{aligned}$ |  |  | $\begin{gathered} 18.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 28.5 \mathrm{~V} \\ 54 \\ 70 \end{gathered}$ |  |  | dB |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Dropout voltage |  |  |  | 2.0 |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\mathrm{IN}}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  |  | 240 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | Iout $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} \\ \|-1.0\| \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ \|-1.0\| \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \|-1.0\| \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{CoUT}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 78M15C1 |  |  | 78M201 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout Output voltage | Over temp., $5 \mathrm{~mA} \leq$ IOUT $\leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{IN}}=23 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=29 \mathrm{~V}$ |  |  | VV |
|  |  | 14.4 | 15.0 | 15.6 | 19.2 | 20 | 20.8 |  |
|  |  | $\begin{array}{c\|c} 17.5 \mathrm{~V} \leq \mathrm{VIN} \leq 30 \mathrm{~V} \\ 14.25 & 15.75 \\ \hline \end{array}$ |  |  | $24 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 35 \mathrm{~V}$ |  |  |  |
|  |  |  |  |  | 19 |  | 21 |  |
| Line regulation | IOUT $=200 \mathrm{~mA}$ | $\begin{gathered} 17.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ \|\quad 10\| 100 \\ 20 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V} \end{gathered}$ |  |  | $23 V \leq V_{I N} \leq 35 V$$\|0\| r$$24 V \leq V_{I N} \leq 35 V$ |  |  | mV |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  | 3 | 50 |  | 5 | 30 | mV |
| Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { IOUT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} 150 \\ 75 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 30 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 200 \\ & 100 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Icc |  |  | 4.8 | 6.0 |  | 4.9 | 6.0 | mA |
| $\Delta \mathrm{ICC} \quad$ With line | Over temp!, Iout $=200 \mathrm{~mA}$ | $17.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V}$ |  |  | $24 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 35 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 0.8 |  |  | 0.8 | mA |
| $\Delta \mathrm{l}$ CC With load | $5 \mathrm{~mA} \leq$ IOUT $\leq 350 \mathrm{~mA}$ |  |  | 0.5 |  |  | 0.5 | mA |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 90 |  |  | 110 |  | $\mu \mathrm{V}$ |
| Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 60 |  |  | 80 | mV |
| Ripple rejection | Over temp., $f=120 \mathrm{~Hz}$ | $\begin{gathered} 18.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 28.5 \mathrm{~V} \\ 54 \\ 70 \end{gathered}$ |  |  | $24 \mathrm{~V} \leq \mathrm{VIN}_{\text {IN }} \leq 34 \mathrm{~V}$ |  |  | dB |
|  |  |  |  |  |  | 70 |  |  |
| Dropout voltage |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc | $V_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  | mA |
| Peak output current |  |  | 700 |  |  | 700 |  | mA |
| Vout Output temperature drift | $\mathrm{I}_{\mathrm{OUT}}=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C}$ | $\begin{aligned} & T_{J} \leq \\ & -1.0 \end{aligned}$ | $25^{\circ} \mathrm{C}$ |  | $\begin{aligned} & T_{J} \leq \\ & -1.1 \end{aligned}$ | $50^{\circ} \mathrm{C}$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS
(Cont'd)

| PARAMETER |  | TEST CONDITIONS | 78M20C ${ }^{1}$ |  |  | 78M241 |  |  | 78M24C1 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $5 \mathrm{~mA} \leq 1$ OUT $\leq 350 \mathrm{~mA}$ | $V_{\text {IN }}=29 \mathrm{~V}$ |  |  | V IN $=33 \mathrm{~V}$ |  |  | $V_{\text {IN }}=33 \mathrm{~V}$ |  |  | VV |
|  |  | 19.2 |  | 20 | 20.8 | 23.0 | 24.0 | 25.0 | 23.0 | 24.0 | 25.0 |  |  |
|  |  | $\begin{array}{c\|c\|c} 23 \mathrm{~V} \leq \mathrm{VIN} \leq 35 \mathrm{~V} \\ 19 & 21 \\ \hline \end{array}$ |  |  | $\begin{aligned} & 28 \mathrm{~V} \leq \mathrm{V} \mathbb{N} \leq 38 \mathrm{~V} \\ & 22.8 \mid \\ & 25.2 \end{aligned}$ |  |  | $27 \mathrm{~V} \leq \mathrm{V}_{1 N} \leq 38 \mathrm{~V}$ |  |  |  |  |
|  |  |  |  |  |  | 22.8 |  | 25.2 |  |  |
| Line regulation |  | IOUT $=200 \mathrm{~mA}$ |  | $\begin{gathered} 23 \mathrm{~V} \leq \mathrm{VIN}_{\text {IN }} \leq 35 \mathrm{~V} \\ \|10\| 100 \\ 24 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 35 \mathrm{~V} \end{gathered}$ |  |  | $\begin{array}{\|c\|c\|c} \hline 27 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V} \\ \mid & 10 & 60 \\ 30 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 36 \mathrm{~V} \end{array}$ |  |  | $\begin{gathered} 27 \mathrm{~V} \leq \mathrm{V}_{\mathrm{N}} \leq 38 \mathrm{~V} \\ \|10\| 100 \\ 28 \mathrm{~V} \leq \mathrm{V}_{\mathrm{N}} \leq 38 \mathrm{~V} \end{gathered}$ |  |  | mV |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 5 | 50 |  | 5 | 30 |  | 5 | 50 | mV |  |  |
| Load regulation |  |  | $5 \mathrm{~mA} \leq 1 \mathrm{CuT} \leq 500 \mathrm{~mA}$ |  | 30 | 400 |  | 30 | 240 |  | 30 | 480 | mV |
|  |  | $5 \mathrm{~mA} \leq 1 \mathrm{l}$ OUT $\leq 200 \mathrm{~mA}$ |  | 10 | 200 |  | 10 | 120 |  | 10 | 240 | mV |  |
| Icc |  |  |  | 4.9 | 6.0 | $\begin{gathered} 28 \mathrm{~V} \leq \mathrm{VIN} \leq 38 \mathrm{~V} \\ \\ \\ \\ \hline \end{gathered} \begin{aligned} & 0.8 \\ & 0.5 \\ & \hline \end{aligned}$ |  |  | - 5 5 6.0 |  |  | mA |  |
| $\Delta \mathrm{ICC}$ <br> $\Delta \mathrm{ICC}$ | With line | $\text { Over temp., IOUT }=200 \mathrm{~mA}$ | $23 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 35 \mathrm{~V}$ |  |  |  |  |  | $27 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | mA <br> mA |  |
|  |  |  |  0.8  <br>   0.5 |  |  |  |  |  |  |  | 0.8 |  |  |
|  | With load | $5 \mathrm{~mA} \leq 1 \mathrm{l}$ OT $\leq 350 \mathrm{~mA}$ |  |  |  |  |  |  |  |  | 0.5 |  |  |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 110 |  |  | 170 |  |  | 170 |  | $\mu \mathrm{V}$ |  |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 80 |  |  | 96 |  |  | 96 | mV |  |
| Ripple rejection |  | Over temp., $f=120 \mathrm{~Hz}$ | $\begin{aligned} & 24 \mathrm{~V} \leq \mathrm{V}_{1 \mathrm{~N}} \leq 34 \mathrm{~V} \\ & 53\|70\| \\ & \hline \end{aligned}$ |  |  | $$ |  |  | $\begin{aligned} & \begin{array}{l} 28 \mathrm{~V} \leq \mathrm{VIN}_{\mathrm{N}} \leq 38 \mathrm{~V} \\ 50 \\ \hline \end{array} \\ & \hline \end{aligned}$ |  |  | dB |  |
| Dropout voltage |  |  |  | 2.0 |  |  | 2.0 |  |  | 2.0 |  | V |  |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  |  | 240 |  | mA |  |
|  | Peak output current |  |  | 700 |  |  | 700 |  |  | 700 |  | mA |  |
| VOUT Output temperature drift |  | IOUT $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \|-1.1\| \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} \\ -1.2 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \|-1.2\| \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |  |

DC ELECTKICAL CHARACTERISTICS (Cont'd) lout $=350 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78M05C ${ }^{2}$ |  |  | SA78M06C2 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $5 \mathrm{~mA} \leq 1$ lout $\leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=11 \mathrm{~V}$ |  |  | V |
|  |  | $\begin{array}{c\|c\|c} 4.8 \mid & 5.0 \mid \\ 7 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq 25 \mathrm{~V} \end{array}$ |  |  | 5.75 | 6.0 | 6.25 |  |  |
|  |  |  |  |  |  | $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 21 \mathrm{~V}$ |  |  |  |  |
|  |  | 4.7 |  |  | 5.3 | 5.7 |  | 6.3 | V |  |
|  | Line regulation | $1 \mathrm{IOUT}=200 \mathrm{~mA}$ |  | $\begin{gathered} 7 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 25 \mathrm{~V} \\ 3 \left\lvert\, \begin{array}{c} \mid 100 \\ 8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V} \end{array}\right. \end{gathered}$ |  |  |  |  |  |  |
|  |  |  | mV |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 1 | 50 | mV |  |  |  |  |  |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { Iout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { Iout } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{gathered} 100 \\ 50 \end{gathered}$ |  | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 120 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |  |
| Icc |  |  |  | 4.5 | 6.0 |  | 4.5 | 8.0 | mA |  |
| $\Delta \mathrm{I} \mathrm{Cc}$ <br> $\Delta \mathrm{lcc}$ | With line | Over temp?, l Out $=200 \mathrm{~mA}$ | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |  |
|  |  |  |  |  |  |  | 0.6 0.3 |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |  |
| Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 40 |  |  | 45 |  | $\mu \mathrm{V}$ |  |
| Voltage drift |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 20 |  |  | 24 | mV |  |
| Ripple rejection |  | Over temp ${ }^{2}$, $\mathrm{f}=120 \mathrm{~Hz}$ | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 18 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 19 \mathrm{~V}$ |  |  |  |  |
|  |  | 62 | 80 |  | 59 | 80 |  | dB |  |  |
| Dropout voltage |  |  |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 300 |  |  | 270 |  | mA |  |
| Peak output current |  |  |  | 700 |  |  | 700 |  | mA |  |
| Vout | Output temperature drift | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$, Iout $=5 \mathrm{~mA}$ |  | -1.0 |  |  | -0.5 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |  |

## DC ELECTRICAL CHARACTERISTICS <br> (Cont'd)

| PARAMETER |  | TEST CONDITIONS | SA78M08C ${ }^{2}$ |  |  | SA78M12C ${ }^{\text {2 }}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $5 \mathrm{~mA} \leq 1 \mathrm{lout} \leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=19 \mathrm{~V}$ |  |  |  |
|  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 23 \mathrm{~V}$ |  |  | 11.5 |  | 12.5 | v |  |
|  |  |  |  |  |  | $14.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 27 \mathrm{~V}$ |  |  |  |
|  |  | 7.6 |  |  | 8.4 | 11.4 |  | 12.6 | V |
| Line regulation | Line regulation | IOUT $=200 \mathrm{~mA}$ |  | $\begin{gathered} 10.5 \mathrm{~V} \leq \mathrm{VIN}_{\mathrm{IN}} \leq 25 \mathrm{~V} \\ 6 \text { \| } 100 \\ 11 \mathrm{~V} \leq \mathrm{VIN} \leq 25 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ 8 \quad \mid 100 \\ 16 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \end{gathered}$ |  |  |  |
|  |  |  | mv |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 2 | 50 |  |  |  | mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { IOUT } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { IOUT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 160 \\ & 80 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.6 | 8.0 |  | 4.8 | 8.0 | mA |
| $\Delta \mathrm{Icc}$ <br> $\Delta \mathrm{Icc}$ | With line | Over temp., Iout $=200 \mathrm{~mA}$ | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  |  |
|  |  |  |  | $\begin{aligned} & 0.6 \\ & 0.3 \end{aligned}$ |  |  | 0.6 0.3 |  | mA mA |
| Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 52 |  |  | 75 |  | $\mu \mathrm{V}$ |
| Voltage drift |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 32 |  |  | 48 | mV |
| Ripple rejection |  | Over temp., $\mathrm{f}=120 \mathrm{~Hz}$ | $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 21.5 \mathrm{~V}$ |  |  | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  | 56 | 80 |  | 55 | 80 |  | dB |  |
| Dropout voltage |  |  |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 250 |  |  | 240 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$, lout $=5 \mathrm{~mA}$ |  | -0.5 |  |  | -1.0 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{CoUT}^{\mathrm{C}}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78M15C2 |  |  | SA78M20C2 |  |  | SA78M24C2 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $5 \mathrm{~mA} \leq$ Iout $\leq 350 \mathrm{~mA}$ |  |  |  | $\begin{array}{\|c} \mathrm{V}_{\text {III }}^{\prime} \\ 19.2 \\ 23 \mathrm{~V} \\ \hline 19 \end{array}$ | $\mathrm{N}=29$ 20 $\leq V_{\text {IN }} \leq$ | $\begin{array}{\|l} 9 \mathrm{~V} \\ 20.8 \\ \leq 35 \mathrm{~V} \\ \hline 21 \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline \mathrm{V}_{\mathrm{IN}}=33 \mathrm{~V} \\ 23.0\|24.0\| 25.0 \\ 27 \mathrm{~V} \leq \mathrm{V}_{\mathrm{N}} \leq 38 \mathrm{~V} \\ 22.8 \mid \\ \hline \end{array}$ |  |  | V V |
|  | Line regulation | IOUT $=200 \mathrm{~mA}$ |  |  |  | $\begin{gathered} 23 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 35 \mathrm{~V} \\ \|10\| 100 \\ 24 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 35 \mathrm{~V} \\ \left\lvert\, \begin{array}{\|c\|c}  & 50 \end{array}\right. \\ \hline \end{gathered}$ |  |  |  |  |  | mV <br> mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq 1 \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq 1 \text { OuT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 150 \\ & 75 \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 10 \end{aligned}$ | $\begin{aligned} & 400 \\ & 200 \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 10 \end{aligned}$ | $\begin{array}{\|l\|} \hline 480 \\ 240 \end{array}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.8 | 8.0 |  | 4.9 | 6.5 |  | 5 | 7 | mA |
| $\Delta \mathrm{Icc}$ <br> $\Delta \mathrm{Icc}$ | With line With load | $\begin{aligned} & \text { Over temp?, Iout }=200 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq 1 \text { Out } \leq 350 \mathrm{~mA} \end{aligned}$ |  |  |  |  |  |  | $\begin{array}{\|c\|} \hline 27 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V} \\ \hline 0.6 \\ 0.3 \\ \hline \end{array}$ |  |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 90 |  |  | 110 |  |  | 170 |  | ${ }^{\mu} \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 60 |  |  | 80 |  |  | 96 | mV |
|  | Ripple rejection | Over temp?, $\mathrm{f}=120 \mathrm{~Hz}$ |  |  |  |  |  |  | $\begin{array}{l\|l\|l\|} \hline 28 \mathrm{~V} \leq \mathrm{VIN} \leq 38 \mathrm{~V} \\ 50 & 70 & \\ \hline \end{array}$ |  |  | dB |
|  | Dropout voltage |  |  | 2.0 |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  |  | 240 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift $0^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq+125^{\circ} \mathrm{C}$, Iout $=5 \mathrm{~mA}$ |  |  | -1.0 |  |  | -1.1 |  |  | -1.2 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$ for 78 M 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ for 78 MOOC
2. $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ for SA78MOOC

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00C)


MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00)


## DESCRIPTION

The 7800 series of monolithic ThreeTerminal Positive Voltage Regulators employ internal current limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.
ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Input voltage |  |  |
| 5 V through 12V | 35 | V |
| 14 V through 24V | 40 | V |
| Internal power dissipation1 | Internally limited |  |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating junction temperature range ${ }^{2}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| 7800 | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| SA7800C | 0 to +125 | ${ }^{\circ} \mathrm{C}$ |
| 7800 C |  | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature | 300 |  |
| TO-3 package (soldering, 60 second time limit) | 230 | ${ }^{\circ} \mathrm{C}$ |
| TO-220 package (soldering, 60 second time limit) |  |  |

1. Thermal resistance of the packages (without a heat sink)

Junction to case: TO-3 package $4^{\circ} \mathrm{C} / \mathrm{W}$; TO-220 package $2^{\circ} \mathrm{C} / \mathrm{W}$
Junction to ambient: TO-3 package $35^{\circ} \mathrm{C} / \mathrm{W}$; TO-220 package $50^{\circ} \mathrm{C} / \mathrm{W}$
2. Operating ambient temperature range $7800-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$7800 \mathrm{C} 0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
SA7800C $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

## SCHEMATIC DIAGRAM



## PIN CONFIGURATION



DC ELECTRICAL CHARACTERISTICS
IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$
unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 78051 |  |  | 7805C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout Output voltage |  | V IN $=10 \mathrm{~V}$ |  |  | $V_{I N}=10 \mathrm{~V}$ |  |  |  |
|  |  | 4.8 | 5.0 | 5.2 | 4.8 | 5.0 | 5.2 | V |
|  | Over temp., $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$, | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V}$ |  |  | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  | $\mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}$ | 4.65 |  | 5.35 | 4.75 |  | 5.25 | V |
| Line regulation |  | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $7 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  | 3 | 50 |  | 3 | 100 | mV |
|  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 12 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 12 \mathrm{~V}$ |  |  |  |
|  |  |  | 1 | 25 |  | 1 | 50 | mV |
| Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 15 \\ 5 \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ |  | $\begin{gathered} 15 \\ 5 \end{gathered}$ | $\begin{gathered} 100 \\ 50 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  | 4.2 | 6.0 |  | 4.2 | 8.0 | mA |
| $\Delta \mathrm{lCC}$ | Over temp., with line | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 0.8 |  |  | 1.3 | mA |
|  | With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ |  |  | 0.5 |  |  | 0.5 | mA |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 40 |  |  | 40 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  |  | 20 |  |  | 20 | $\mathrm{mV} / 1000 \mathrm{hrs}$. |
| Ripple rejection | Over temp., ${ }^{1} \mathrm{f}=120 \mathrm{~Hz}$ | $8 \mathrm{~V} \leq \mathrm{V}$ IN $\leq 18 \mathrm{~V}$   <br> 68   <br> 88   |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 18 \mathrm{~V}$ |  |  |  |
|  |  |  |  |  |  | $78$ |  | dB |
| Dropout voltage | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance | $f=1 \mathrm{kHz}$ |  | 17 |  |  | 17 |  | $\mathrm{m} \Omega$ |
| Isc |  |  | 750 |  |  | 750 |  | mA |
| Peak output current |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout Output temperature drift | IOUT $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 1.150^{\circ} \mathrm{C}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ -1.1 \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) lout $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}_{\mathrm{O}}=0.1 \mu \mathrm{~F}, \mathrm{TJ}=25^{\circ} \mathrm{C}$ unless otherwise specified

| PARAMETER | TEST CONDITIONS | 78061 |  |  | 7806C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout Output voltag | Over temp., $5 \mathrm{~mA} \leq$ Iout $\leq 1.0 \mathrm{~A}$, $P_{D} \leq 15 W$ | $\mathrm{V}_{\text {IN }}=11 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=11 \mathrm{~V}$ |  |  | V |
|  |  | 5.75 | 6.0 | 6.25 | 5.75 | 6.0 | 6.25 |  |
|  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 21 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{VIN} \leq 21 \mathrm{~V}$ |  |  |  |
|  |  | 5.65 |  | 6.35 | 5.7 |  | 6.3 | V |
| Line regulation |  | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  | $9 V \leq V_{I N} \leq 13 V$ |  |  | $\begin{gathered} 5 \\ 9 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq \end{gathered}$ |  | $120$ | mV |
|  |  |  |  |  | $13 \mathrm{~V}$ |  |  |
|  |  |  | 1.5 | 30 |  |  |  | 1.5 | 60 | mV |
| Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \mathrm{IOUT} \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \mathrm{IOUT} \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 14 \\ 4 \end{gathered}$ | $\begin{aligned} & 60 \\ & 30 \end{aligned}$ |  | $\begin{gathered} 14 \\ 4 \end{gathered}$ | $\begin{gathered} 120 \\ 60 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| ICC |  |  | 4.3 | 6.0 |  | 4.3 | 8.0 | mA |
| $\Delta \mathrm{ICC}$ | Over temp., with line | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{1 N} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 0.8 |  |  | 1.3 | mA |
|  | With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ |  |  | 0.5 |  |  | 0.5 | mA |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 45 |  |  | 45 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  |  | 24 |  |  | 24 | $\mathrm{mV} / 1000 \mathrm{hrs}$. |
| Ripple rejection | Over temp.1 f $=120 \mathrm{~Hz}$ |  |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 19 \mathrm{~V}$ |  |  | dB |
|  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 19 \mathrm{~V}$65 |  |  | 59 | $\leq \mathrm{V}_{\text {IN }} \leq$ 75 |  |  |
| Dropout voltage | lout $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 19 |  |  | 19 |  | $\mathrm{m} \Omega$ |
| Isc |  |  | 550 |  |  | 550 |  | mA |
| Peak output current |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout Output temperature drift | lout $=5 \mathrm{~mA}$ |  | $\begin{aligned} & T_{J} \leq \\ & -0.8 \end{aligned}$ | $50^{\circ} \mathrm{C}$ |  | $\begin{aligned} & \mathrm{T}_{\mathrm{J}} \leq \\ & -0.8 \end{aligned}$ | $125^{\circ} \mathrm{C}$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}$, Cout $^{\mathrm{C}}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 78081 |  |  | 7808C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout Output voltage | Over temp., $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$,$P_{D} \leq 15 W$ | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$ |  |  | VV |
|  |  |  | 8.0 | 8.3 | 7.7 | 8.0 | 8.3 |  |
|  |  | $11.5 \mathrm{~V} \leq \mathrm{VIN} \leq 23 \mathrm{~V}$ |  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 23 \mathrm{~V}$ |  |  |  |
|  |  | 7.6 |  | 8.4 | 7.6 |  | 8.4 |  |
| Line regulation |  | $\begin{array}{c\|r} \hline 10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V} \\ 6 & 80 \\ 11 \mathrm{~V} \leq \mathrm{VIN} \leq 17 \mathrm{~V} \end{array}$ |  |  | $\begin{array}{c\|c} \hline 10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V} \\ \mid \quad 6 & 160 \\ 11 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V} \end{array}$ |  |  | mV |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  | 2 | 40 |  | 2 | 80 | mV |
| Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { I OUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | 12 4 | $\begin{aligned} & 80 \\ & 40 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{gathered} 160 \\ 80 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Icc |  |  <br> $11.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  4.3 8.0 |  |  | mA |
| $\Delta \mathrm{I} C \mathrm{C}$ | Over temp., with line <br> With load, $5 \mathrm{~mA} \leq$ IOUT $\leq 1.0 \mathrm{~A}$ | $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  |  |   0.8 <br>   0.5 |  |  |  1.0 <br>  0.5 |  |  |  |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 52 |  |  | 52 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  |  | 32 |  |  |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |
| Ripple rejection | Over temp., $\mathrm{f}=120 \mathrm{~Hz}$ | $11.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 21.5 \mathrm{~V}$ |  |  | $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 21.5 \mathrm{~V}$ |  |  | dB |
|  |  | 62 | 72 |  | 56 | 72 |  |  |
| Dropout voltage | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 16 |  |  | 16 |  | $\mathrm{m} \Omega$ |
| Isc |  |  | 450 |  |  | 450 |  | mA |
| Peak output current |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout Output temperature drift | IOUT $=5 \mathrm{~mA}$ |  | $\begin{aligned} & T_{J} \leq \\ & -0.8 \end{aligned}$ | $50^{\circ} \mathrm{C}$ |  | $\begin{gathered} =T_{J} \leq \\ -0.8 \end{gathered}$ | $25^{\circ} \mathrm{C}$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}$, $\mathrm{Cout}^{\prime}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.


DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}$, COUT $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| PARAMETER | TEST CONDITIONS | 78141 |  |  | 7814C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout Output voltage | $\begin{gathered} \text { Over temp., } 5 \mathrm{~mA} \leq \mathrm{I} \text { OUT } \leq 1.0 \mathrm{~A}, \\ P_{D} \leq 15 \mathrm{~W} \end{gathered}$ | $\mathrm{V}_{\text {IN }}=22 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=22 \mathrm{~V}$ |  |  | VV |
|  |  | 13.3 | 13.8 | 14.3 | 13.3 | 13.8 | 14.3 |  |
|  |  | $17.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 29 \mathrm{~V}$ |  |  | $16.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 29 \mathrm{~V}$ |  |  |  |
|  |  | 13.15 |  | 14.45 | 13.15 |  | 14.95 |  |
| Line regulation |  | $16.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $16.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V}$ |  |  | mV |
|  |  |  | 10 | 140 |  | 10 | 280 |  |
|  |  | $19 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $19 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  | 3 | 70 |  | 3 | 140 | mV |
| Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{gathered} 140 \\ 70 \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 280 \\ & 140 \end{aligned}$ | $\begin{aligned} & m V \\ & m V \end{aligned}$ |
| Icc |  |  | 4.3 | 6.0 |  | 4.3 | 8.0 | mA |
| $\Delta \mathrm{lCC}$ | Over temp., with line | $17 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V}$ |  |  | $16.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 0.8 |  |  | 1.0 | mA |
|  | With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ |  |  | 0.5 |  |  | 0.5 | mA |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 85 |  |  | 85 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  |  | 56 |  |  | 56 | $\mathrm{mV} / 1000 \mathrm{hrs}$. |
| Ripple rejection | Over temp., $\mathrm{f}=120 \mathrm{~Hz}$ | $17 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 27 \mathrm{~V}$ |  |  | $17 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 27 \mathrm{~V}$ |  |  |  |
|  |  | 54 | 70 |  | 60 | 70 |  | dB |
| Dropout voltage | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 18 |  |  | 18 |  | $\mathrm{m} \Omega$ |
| Isc |  |  | 350 |  |  | 350 |  | mA |
| Peak output current |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout Output temperature drift | $\mathrm{IOUT}=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \mid \quad 1.0 \\ \hline \end{gathered}$ |  |  | $\begin{array}{c\|c\|l} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ & 1.0 & \\ \hline \end{array}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{I}_{\mathrm{OUT}}=500 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78151 |  |  | 7815C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $\begin{gathered} \text { Over temp., } 5 \mathrm{~mA} \leq \mathrm{lout} \leq 1.0 \mathrm{~A}, \\ \mathrm{PD}_{\mathrm{D}} \leq 15 \mathrm{~W} \end{gathered}$ | $\begin{array}{\|c\|} \hline 14.4 \\ 18.5 \\ 14.25 \\ \hline \end{array}$ | $\mathrm{N}=23$ 15.0 $\leq \mathrm{V}_{\text {IN }}$ | $\begin{aligned} & 15.6 \\ & 30 \mathrm{~V} \\ & 15.75 \end{aligned}$ | 14.4 17.5 14.25 | $\mathrm{N}=2$ 15.0 $\leq \mathrm{V}_{\text {IN }}$ | $\begin{array}{r} 15.6 \\ \leq 30 \mathrm{~V} \\ 15.75 \end{array}$ | V <br> V |
|  | Line regulation |  | $\begin{gathered} 17.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V} \\ \mid \\ 11 \\ 20 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V} \end{gathered}$ |  |  | $\begin{array}{c\|c} 17.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ 11 & 300 \\ 20 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V} \end{array}$ |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
|  | Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \mathrm{IOUT} \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \mathrm{IOUT} \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \\ \hline \end{gathered}$ | $\begin{aligned} & 150 \\ & 75 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 12 \\ 4 \\ \hline \end{gathered}$ | $\begin{aligned} & 300 \\ & 150 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Icc |  |  |  | 4.4 | 6.0 |  | 4.4 | 8.0 | mA |
| $\Delta \mathrm{lcc}$ |  | Over temp., with line <br> With load, $5 \mathrm{~mA} \leq$ IOUT $\leq 1.0 \mathrm{~A}$ | 18.5V | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{array}{r} 30 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{array}$ | 17.5 | $\leq \mathrm{V}_{\mathrm{IN}}$ | $\begin{array}{r} \leq 30 \mathrm{~V} \\ 1.0 \\ 0.5 \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 90 |  |  | 90 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  |  |  | 60 |  |  | 60 | $\mathrm{mV} / 1000 \mathrm{hrs}$. |
| Ripple rejection |  | Over temp., $\dagger \mathrm{f}=120 \mathrm{~Hz}$ | $18.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 28.5 \mathrm{~V}$ |  |  | $18.5 \mathrm{~V} \leq \mathrm{V}$ IN $\leq 28.5 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage | lout $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
|  | Output resistance | $f=1 \mathrm{kHz}$ |  | 19 |  |  | 19 |  | $\mathrm{m} \Omega$ |
| Isc |  |  |  | 230 |  |  | 230 |  | mA |
| Peak output current |  |  |  | 2.1 |  |  | 2.1 |  | A |
| Vout | Output temperature drift | lout $=5 \mathrm{~mA}$ |  | $\begin{aligned} & T_{J} \leq \\ & -1.0 \\ & \hline \end{aligned}$ | $50^{\circ} \mathrm{C}$ |  | $\begin{aligned} & T_{J} \leq \\ & -1.0 \\ & \hline \end{aligned}$ | $25^{\circ} \mathrm{C}$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}$, COUT $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| PARAMETER | TEST CONDITIONS | 78181 |  |  | 7818C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout Output voltage | Over temp. ${ }^{1} 5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$, | $\begin{gathered} 17.3 \\ 22 \mathrm{~V} \\ 17.1 \end{gathered}$ | $\begin{aligned} & \mathrm{N}=27 \\ & 18.0 \\ & \mathrm{~V} \text { IN } \leq \end{aligned}$ | $\begin{gathered} 18.7 \\ 33 V \\ 18.9 \end{gathered}$ | 17.3 21 V 17.1 | N $=2$ 18.0 $\leq \mathrm{V}_{\text {IN }}$ | $18.7$ $33 \mathrm{~V}$ $18.9$ | v <br> V |
| Line regulation |  | $\begin{gathered} 21 \mathrm{~V} \leq \mathrm{VIN}^{2} \leq 33 \mathrm{~V} \\ 15 \\ 24 \mathrm{~V} \leq \mathrm{VIN}^{2} \leq 30 \mathrm{~V} \end{gathered}$ |  |  |  |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \mathrm{IOUT} \leq 750 \mathrm{~mA} \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline 12 \\ 4 \\ \hline \end{gathered}$ | $\begin{gathered} 180 \\ 90 \\ \hline \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 360 \\ & 180 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  | 4.5 | 6.0 |  | 4.5 | 8.0 | mA |
| $\Delta \mathrm{lcc}$ | Over temp., with line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | 22 V | Vin $\leq$ | $\begin{gathered} \hline 33 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{gathered}$ | 21 V | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{array}{r} 33 \mathrm{~V} \\ 1.0 \\ 0.5 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 110 |  |  | 110 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  |  | 72 |  |  | 72 | mV/1000hrs. |
| Ripple rejection | Over temp., $\mathrm{f}=12 \mathrm{~Hz}$ | $\begin{gathered}22 \mathrm{~V}\end{gathered} \mathrm{~V}_{1 \mathrm{~N}} \leq 32 \mathrm{~V}$ |  |  | $22 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 32 \mathrm{~V}$ |  |  | dB |
| Dropout voltage | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 22 |  |  | 22 |  | $\mathrm{m} \Omega$ |
| Isc |  |  | 200 |  |  | 200 |  | mA |
| Peak output current |  |  | 2.1 |  |  | 2.1 |  | A |
| Vout Output temperature drift | Iout $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \|-1.0\| \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \|\quad-1.0\| \\ \hline \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}$, Cout $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$

| PARAMETER | TEST CONDITIONS | 78241 |  |  | 7824C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout Output voltage | $\begin{gathered} \text { Over temp. } 1,5 \mathrm{~mA} \leq \text { lout } \leq 1.0 \mathrm{~A}, \\ P \mathrm{PD} \leq 15 \mathrm{~W} \end{gathered}$ | $\begin{gathered} 23.0 \\ 28 \mathrm{~V} \\ 22.8 \\ \hline \end{gathered}$ | $\mathrm{N}=33$ 24.0 $\mathrm{~V}_{\text {IN }} \leq$ | $\begin{gathered} 25.0 \\ 38 \mathrm{~V} \\ 25.2 \\ \hline \end{gathered}$ | $\begin{gathered} 23.0 \\ 28 \mathrm{~V} \\ 22.8 \\ \hline \end{gathered}$ | N $=3$ 24.0 VIN | $\begin{gathered} 25.0 \\ 38 \mathrm{~V} \\ 25.2 \\ \hline \end{gathered}$ | v <br> V |
| Line regulation |  | $\begin{array}{c\|c} 27 \mathrm{~V} \leq V_{\text {IN }} \leq 38 \mathrm{~V} \\ \mid 18 & \mid 240 \\ 30 \mathrm{~V} \leq V_{\text {IN }} \leq 36 \mathrm{~V} \end{array}$ |  |  | $\begin{array}{cc\|c} 27 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V} \\ \mid & 18 & 480 \\ 30 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} & \leq 36 \mathrm{~V} \end{array}$ |  |  | mV <br> mV |
| Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IouT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 240 \\ & 120 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & \hline 480 \\ & 240 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  | 4.6 | 6.0 |  | 4.6 | 8.0 | mA |
| $\Delta \mathrm{lcc}$ | Over temp.! with line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | 28 V | VIN | $\begin{array}{r} \hline 38 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{array}$ | 27 V | $\leq \mathrm{V}$ IN | $\begin{array}{r} 38 \mathrm{~V} \\ 1.0 \\ 0.5 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 170 |  |  | 170 |  | ${ }_{\mu} \mathrm{V}$ |
| Voltage drift |  |  |  | 96 |  |  | 96 | $\mathrm{mV} / 1000 \mathrm{hrs}$. |
| Ripple rejection | Over temp., $\mathrm{f}=12 \mathrm{~Hz}$ | $28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | 50 | 66 |  | dB |
| Dropout voltage | lout $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 28 |  |  | 28 |  | $\mathrm{m} \Omega$ |
| Isc |  |  | 150 |  |  | 150 |  | mA |
| Peak output current |  |  | 2.1 |  |  | 2.1 |  | A |
| Vout Output temperature drift | IOUT $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq 125^{\circ} \mathrm{C}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}$, Cout $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.


DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathbb{I N}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.


## TIIRE-TRRMINAL POSTIVE VOTTAGE REGULATOR

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}$, Cout $^{\mathrm{C}}=0.1 \mu \mathrm{~F}, \mathrm{TJ}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.


DC ELECTRICAL CHARACTERISTICS (Cont'd) Iout $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$
unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA7818C ${ }^{2}$ |  |  | SA7824C ${ }^{2}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $\begin{gathered} \text { Over temp., } 5 \mathrm{~mA} \leq \text { lout } \leq 1.0 \mathrm{~A}, \\ P_{D} \leq 15 \mathrm{~W} \end{gathered}$ | $\begin{gathered} 17.3 \mid \\ 21 \mathrm{~V} \\ 17.1 \end{gathered}$ | IN $=27$ 18.0 VIN | $\begin{gathered} 18.7 \\ : 33 \mathrm{~V} \\ 18.9 \end{gathered}$ | $\begin{gathered} 23.0 \\ 28 \mathrm{~V} \\ 22.8 \end{gathered}$ | $\begin{gathered} 1 \mathrm{~N}=3 \\ 24.0 \\ \leq \mathrm{VIN} \end{gathered}$ | $\begin{gathered} 25.0 \\ =38 \mathrm{~V} \\ 25.2 \end{gathered}$ | v v |
| Line regulation |  |  | $\begin{array}{c\|c\|c} 21 \mathrm{~V} & \leq V_{\text {IN }} \leq 33 V \\ 15 & 360 \\ 24 \mathrm{~V} & \leq V_{\text {IN }} & \leq 30 \mathrm{l} \end{array}$ |  |  | $\begin{array}{c\|c} 27 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V} \\ 18 & 480 \\ 30 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 36 \mathrm{~V} \end{array}$ |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
|  | Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 360 \\ & 180 \end{aligned}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 480 \\ & 240 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.5 | 8.0 |  | 4.6 | 8.0 | mA |
| Icc |  | Over temp., with line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | 21 V | $\quad$ ViN 0.8 0.3 | 33 V | 27 V | ¢ $\mathrm{V}_{\text {IN }}$ 0.8 0.3 | 38 V | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 110 |  |  | 170 |  | $\mu \mathrm{V}$ |
|  | Voltage drift |  |  |  | 72 |  |  | 96 | mV/1000hrs. |
|  | Ripple rejection | Over temp., $\mathrm{f}=120 \mathrm{~Hz}$ | $22 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 32 \mathrm{~V}$ |  |  | $27 \mathrm{~V} \leq \mathrm{ViN} \leq 38 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | $\checkmark$ |
|  | Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 22 |  |  | 28 |  | m , |
| Isc |  |  |  | 200 |  |  | 150 |  | mA |
|  | Peak output current |  |  | 2.1 |  |  | 2.1 |  | A |
| Vout | Output temperature drift | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ \text { IOUT }=5 \mathrm{~mA} \end{gathered}$ |  | -1.0 |  |  | -1.5 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7800C)


RIPPLE REJECTION AS A FUNCTION OF FREQUENCY


CURRENT LIMITING
CHARACTERISTICS


DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE


OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE


LOAD TRANSIENT RESPONSE


PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE


DROPOUT CHARACTERISTICS


LINE TRANSIENT RESPONSE


## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



## EQUIVALENT TEST CIRCUITS



RIPPLE REJECTION TEST CIRCUIT


## DESCRIPTION

The $\mu \mathrm{A} 7900$ series of monolithic ThreeTerminal Negative Voltage Regulators employs internal current limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage complements to the $\mu \mathrm{A} 7800$ positive regulators.

## FEATURES

- Output current in excess of 1 amp
- No external components
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Available in the TO-220 and the TO-3 packages
- Output voltages of $-5,-5.2,-6,-8,-12$, $-15,-18$ and -24 volts
- Mil std 883A,B,C available


## ABSOLUTE MAXIMUM RATINGS



## NOTES

1. Thermal resistance of the packages (without a heat sink)

Junction to case: TO-3 Package $4^{\circ} \mathrm{C} / \mathrm{W}$; TO-220 Package $2^{\circ} \mathrm{C} / \mathrm{W}$ Junction to ambient: TO-3 Package $35^{\circ} \mathrm{C} / \mathrm{W}$; TO-220 Package $50^{\circ} \mathrm{C} / \mathrm{W}$
2. Operating Ambient Temperature Range
$7900-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$7900 \mathrm{C} 0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

## PIN CONFIGURATION



DA PACKAGE (TO-3)


ORDER INFORMATION

| Output <br> voltage | Order <br> part no. |
| :--- | ---: |
| -5 V | 7905 DA |
| -5.2 V | 7905.2 DA |
| -6 V | 7906 DA |
| -8 V | 7908 DA |
| -12 V | 7912 DA |
| -15 V | 7915 DA |
| -18 V | 7918 DA |
| -24 V | 7924 DA |
| -5 V | 7905 CDA |
| -5.2 V | 7905.2 CDA |
| -6 V | 7906 CDA |
| -8 V | 7908 CDA |
| -12 V | 7912 CDA |
| -15 V | 7915 CDA |
| -18 V | 7918 CDA |
| -24 V | 7924 CDA |

DC ELECTRICAL CHARACTERISTICS
lout $=500 \mathrm{~mA},-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 1$
$\mathrm{C}_{\mathrm{IN}}=2 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=1 \mu \mathrm{~F}$ unless otherwise specified.


NOTE

1. $7900 \mathrm{C}-0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$

## 

DC ELECTRICAL CHARACTERISTICS
(Cont'd) Iout $=500 \mathrm{~mA},-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 1$
$\mathrm{C}_{\mathrm{IN}}=2 \mu \mathrm{~F}$, Cout $=1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 7905.2C |  |  | 7906 |  |  | 7906C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vout | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \mathrm{P} \leq 15 \mathrm{~W} \\ 5 \mathrm{~mA} \leq \text { Iout } \leq 1.0 \mathrm{~A} \end{gathered}$ | $\begin{aligned} & -5.0 \\ & -7.2 \mathrm{~V} \\ & -4.94 \end{aligned}$ | $\begin{aligned} & V=-1 \\ & -5.2 \\ & \leqslant \text { VIN } \end{aligned}$ | $\begin{gathered} -5.4 \\ -20 \mathrm{~V} \\ -5.46 \end{gathered}$ | $\begin{gathered} V \\ -5.75 \\ -9 V \\ -5.65 \end{gathered}$ | $\begin{aligned} & =-11 \\ & -6.0 \\ & \text { VIN } \leq \end{aligned}$ | $\begin{aligned} & -6.25 \\ & 1 \mathrm{~V} \\ & -6.35 \end{aligned}$ | $\begin{gathered} -5.75 \\ -8 \mathrm{~V} \\ -5.7 \end{gathered}$ | $\begin{aligned} & N=-1 \\ & -6.0 \\ & V_{\text {IN }} \leq \end{aligned}$ | $\begin{aligned} & -6.25 \\ & 25 \mathrm{~V} \\ & -6.3 \end{aligned}$ | v |
| Line regulation | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $\begin{gathered} -7.2 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-25 \mathrm{~V} \\ 3 \\ -8 \mathrm{~V} \leq \mathrm{VIN} \leq-12 \mathrm{~V} \end{gathered}$ |  |  | $\begin{array}{c\|c\|c} -8 V & V_{\text {IN }} \leq-25 V \\ -9 V & 60 \\ -9 V_{I N} \leq-13 V \end{array}$ |  |  | $-8 V \leq V_{I N} \leq-25 V$5$-9 V \leq V_{\text {IN }} \leq-13 V$ |  |  | mV |
| Load regulation | $\begin{aligned} \mathrm{T}_{J} & =25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} & \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} & \leq \text { Iout } \leq 750 \mathrm{~mA} \end{aligned}$ |  | 15 5 | $\begin{gathered} 105 \\ 52 \end{gathered}$ |  | 14 4 | 60 30 |  | 14 4 | $\begin{aligned} & 120 \\ & 60 \end{aligned}$ | mV |
| Icc with line with load | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \text { Iout } \leq 1.0 \mathrm{~A} \end{gathered}$ | $-7.2 \mathrm{~V}$ | $\begin{gathered} 1 \\ \leq V_{I N} \\ 0.1 \end{gathered}$ | $\begin{array}{r} 2 \\ -25 \mathrm{~V} \\ 1.3 \\ 0.5 \end{array}$ | -9V | 1 $\mathrm{~V}_{\text {IN }} \leq$ 0.1 | $\begin{gathered} 2 \\ 25 \mathrm{~V} \\ 1.3 \\ 0.5 \end{gathered}$ | -8V | 1 $V_{\text {IN }} \leq$ 0.1 | $\begin{gathered} 2 \\ 25 \mathrm{~V} \\ 1.3 \\ 0.5 \end{gathered}$ | mA |
| Output noise voltage | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{gathered}$ |  | 130 |  |  | 150 |  |  | 150 |  | $\mu \mathrm{V}$ |
| Long term stability |  |  | 22 |  |  | 24 |  |  | 24 |  | mV |
| Ripple rejection | $\begin{gathered} \mathrm{f}=120 \mathrm{~Hz} \\ \mathrm{IOUT}=20 \mathrm{~mA} \end{gathered}$ | $-8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-18 \mathrm{~V}$ |  |  | $-9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-19 \mathrm{~V}$ |  |  | $-9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-19 \mathrm{~V}$ |  |  | dB |
| Dropout voltage | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \text { Iout }=1.0 \mathrm{~A} \end{gathered}$ |  | 1.1 |  |  | 1.1 |  |  | 1.1 |  | v |
| Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 17 |  |  | 19 |  |  | 19 |  | $\mathrm{m} \Omega$ |
| los | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 500 |  |  | 500 |  |  | 500 |  | mA |
| Peak output current | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 2.1 |  |  | 2.1 |  |  | 2.1 |  | A |
| Average temperature coefficient of input voltage | lout $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ -0.4 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} \\ -0.4 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ -0.4 \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE

1. $7900-0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA},-55^{\circ} \mathrm{C} \leq T_{J} \leq 150^{\circ} \mathrm{C}, 1$
$\mathrm{C}_{\mathrm{IN}}=2 \mu \mathrm{~F}$, Cout $=1 \mu \mathrm{~F}$ unless otherwise specified.


NOTE

1. $7900 \mathrm{C}-0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$

DC ELECTRICAL CHARACTERISTICS
(Cont'd) lout $=500 \mathrm{~mA},-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C},{ }^{1}$ $\mathrm{C}_{\mathrm{IN}}=2 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 7912C |  |  | 7915 |  |  | 7915C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vout | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \mathrm{P} \leq 15 \mathrm{~W} \\ 5 \mathrm{~mA} \leq \mathrm{IOUT} \leq 1.0 \mathrm{~A} \end{gathered}$ | $\begin{aligned} & -11.5-12.0-12.5 \\ & -14.5 \mathrm{~V} \leq \mathrm{VIN}_{\mathrm{IN}} \leq-27 \mathrm{~V} \\ & -11.4 \end{aligned}$ |  |  | $\begin{aligned} & -14.4 \quad-15.0 \quad-15.6 \\ & -18.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-30 \mathrm{~V} \\ & -14.25 \mathrm{l} \end{aligned}$ |  |  | $\begin{aligned} & -14.4 \quad-15.0-15.6 \\ & -17.5 \mathrm{~V} \leq \mathrm{V} \mathrm{IN} \leq-30 \mathrm{~V} \\ & -14.25 \quad \Gamma^{-5.75} \end{aligned}$ |  |  | V |
| Line regulation | $\mathrm{T}, ~ 25^{\circ} \mathrm{C}$ | $\begin{array}{r} -14.5 V \leq V_{I N} \leq-30 V \\ \|10 \quad\| 240 \\ -16 V \leq V_{I N} \leq-22 V \end{array}$ |  |  | $\begin{gathered} -17.5 \mathrm{~V} \leq \mathrm{V}_{\mathbb{N}} \leq-30 \mathrm{~V} \\ \left\lvert\, \begin{array}{l} 11 \\ -20 \mathrm{~V} \leq \mathrm{V}_{\mathbb{N}} \leq-26 \mathrm{~V} \end{array}\right. \end{gathered}$ |  |  | $\begin{gathered} -17.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-30 \mathrm{~V} \\ \|11\| 300 \\ -20 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-26 \mathrm{~V} \end{gathered}$ |  |  | mV |
| Load regulation | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | 12 4 | 240 120 |  | 12 4 | $\begin{gathered} 150 \\ 75 \end{gathered}$ |  | 12 4 | 300 150 | mV |
| ICC with line with load | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ $5 \mathrm{~mA} \leq \mathrm{IOUT} \leq 1.0 \mathrm{~A}$ | $-14.5$ | $\begin{gathered} 1.5 \\ \leq \mathrm{V}_{\mathrm{IN}} \\ .1 \end{gathered}$ | $\begin{array}{r} 3.0 \\ -30 \mathrm{~V} \\ 1.0 \\ 0.5 \end{array}$ | $-18.5$ | $\begin{gathered} 1.5 \\ \leq \mathrm{V}_{\mathrm{IN}} \\ .1 \end{gathered}$ | $\begin{gathered} 3.0 \\ -30 \mathrm{~V} \\ 1.0 \\ 0.5 \end{gathered}$ | $-17.5$ | $\begin{gathered} 1.5 \\ \leq \mathrm{V}_{\text {IN }} 5 \\ .1 \end{gathered}$ | $\begin{array}{r} 3.0 \\ -30 \mathrm{~V} \\ 1.0 \\ 0.5 \end{array}$ | mA |
| Output noise voltage | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{gathered}$ |  | 300 |  |  | 375 |  |  | 375 |  | $\mu \mathrm{V}$ |
| Long term stability |  |  | 48 |  |  | 60 |  |  | 60 |  | mV |
| Ripple rejection | $\begin{gathered} \mathrm{f}=120 \mathrm{~Hz} \\ \text { Iout }=20 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} -15 \mathrm{~V} \\ 54 \end{gathered}$ | $\begin{aligned} & \mathrm{V}_{\text {IN }} \leq \\ & 60 \end{aligned}$ |  | $\begin{gathered} 18.5 \mathrm{~V} \\ 54 \end{gathered}$ | $\begin{gathered} \mathrm{V}_{\text {IN }} \leq \\ 60 \end{gathered}$ | $28.5 \mathrm{~V}$ | $\begin{gathered} -18.5 \mathrm{~V} \\ 54 \end{gathered}$ | $\begin{gathered} V_{\text {IN }} \leq \\ 60 \end{gathered}$ | $28.5 \mathrm{~V}$ | dB |
| Dropout voltage | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \text { IOUT }=1.0 \mathrm{~A} \end{gathered}$ |  | 1.1 |  |  | 1.1 |  |  | 1.1 |  | V |
| Output resistance | $f=1 \mathrm{kHz}$ |  | 18 |  |  | 19 |  |  | 19 |  | $\mathrm{m} \Omega$ |
| los | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 500 |  |  | 500 |  |  | 500 |  | mA |
| Peak output current | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 2.1 |  |  | 2.1 |  |  | 2.1 |  | A |
| Average temperature coefficient of input voltage | $\mathrm{IOUT}=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \mid-0.8 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} \\ \|-1.0\| \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \mid-1.0 \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE

1. $7900 \mathrm{C}-0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$

DC ELECTRICAL CHARACTERISTICS (Cont'd) Iout $=500 \mathrm{~mA},-55^{\circ} \mathrm{C} \leq T_{J} \leq 150^{\circ} \mathrm{C}, 1$
$\mathrm{C}_{\mathrm{IN}}=2 \mu \mathrm{~F}$, Cout $=1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 7918 |  |  | 7918C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | $\begin{gathered} \mathrm{TJ}=25^{\circ} \mathrm{C} \\ \mathrm{P} \leq 15 \mathrm{~W} \\ 5 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 1.0 \mathrm{~A} \end{gathered}$ | $\begin{aligned} & -17.3\|-18.0 \quad\|-18.7 \\ & -22 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq-33 \mathrm{~V} \\ & -17.1 \mid \end{aligned}$ |  |  | $\begin{array}{cc} -17.3 \quad\|-18.0 \quad\|-18.7 \\ -21 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq-33 \mathrm{~V} \\ -17.1 \quad \mid \end{array}$ |  |  | V |
| Line regulation | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $\begin{array}{r} -21 V \leq V_{I N} \leq-33 V \\ -24 V \leq V_{I N} \leq-30 V \end{array}$ |  |  | $\begin{gathered} -21 V \leq V_{I N} \leq-33 V \\ \|15 \quad\| 360 \\ -24 V \leq V_{\mathbb{N}} \leq-30 V \end{gathered}$ |  |  | mV |
| Load regulation | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | 12 4 | 180 90 |  | 12 4 | 360 180 | mV |
| Icc with line with load | $T_{J}=25^{\circ} \mathrm{C}$ | $\begin{array}{c\|r} 1.5 & 3.0 \\ -22 V \leq V_{\text {IN }} \leq-33 V \end{array}$ |  |  | $-21.5 \mid 3.0$ |  |  | mA |
| Output noise voltage | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ 1.0 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{gathered}$ |  | 450 |  |  | 450 |  | $\mu \mathrm{V}$ |
| Long term stability |  |  | 72 |  |  | 72 |  | mV |
| Ripple rejection | $\begin{gathered} f=120 \mathrm{~Hz} \\ \text { IOUT }=20 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & -22 V \leq V_{\text {IN }} \leq-32 V \\ & 54 \end{aligned} 60$ |  |  | $\begin{array}{c\|c\|} \hline-22 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-32 \mathrm{~V} \\ 54 & 60 \\ \hline \end{array}$ |  |  | dB |
| Drupout voltage | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \text { IOUT }=1.0 \mathrm{~A} \end{gathered}$ |  | 1.1 |  |  | 1.1 |  | V |
| Output resistance | $f=1 \mathrm{kHz}$ |  | 22 |  |  | 22 |  | $\mathrm{m} \Omega$ |
| los | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 500 |  |  | 500 |  | mA |
| Peak output current | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 2.1 |  |  | 2.1 |  | A |
| Average temperature coefficient of input voltage | $\mathrm{IOUT}=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \mid-1.0 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ -1.0 \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE

[^1]DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA},-55^{\circ} \mathrm{C} \leq T_{J} \leq 150^{\circ} \mathrm{C}, 1$
$\mathrm{C}_{\mathrm{IN}}=2 \mu \mathrm{~F}$, COUT $=1 \mu \mathrm{~F}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 7924 |  |  | 7924C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | $\begin{gathered} \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ \mathrm{P} \leq 15 \mathrm{~W} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.0 \mathrm{~A} \end{gathered}$ | $\begin{gathered} -23.0 \\ -28 \mathrm{~V} \\ -22.8 \end{gathered}$ | N $=-38$ -24.0 VIN | $\begin{aligned} & -25.0 \\ & -38 \mathrm{~V} \\ & -25.2 \end{aligned}$ | $\begin{gathered} -23.0 \\ -27 \mathrm{~V} \\ -22.8 \end{gathered}$ | $=-3$ -24.0 VIN $\leq$ | $\begin{aligned} & V \\ & 1-25.0 \\ & -38 \mathrm{~V} \\ & -25.2 \end{aligned}$ | V |
| Line regulation | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\begin{array}{r} -27 V \leq V_{I N} \leq-38 V \\ 18 \\ 1840 \\ -30 V \leq V_{\text {IN }} \leq-36 V \end{array}$ |  |  | $\begin{array}{r} -27 V \leq V_{I N} \leq-38 V \\ \|18\| 480 \\ -30 V \leq V_{I N} \leq-36 V \end{array}$ |  |  | mV |
| Load regulation | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \text { IouT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IouT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | 12 4 | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ |  | $\begin{gathered} 120 \\ 4 \end{gathered}$ | $\begin{aligned} & 480 \\ & 240 \end{aligned}$ | mV |
| Icc with line with load | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.0 \mathrm{~A} \end{gathered}$ | $-28 \mathrm{~V}$ | $\begin{aligned} & 1.5 \\ & \mathrm{VIN} \\ & 0.1 \end{aligned}$ | $\begin{array}{r} 3.0 \\ -38 \mathrm{~V} \\ 1.0 \\ 0.5 \end{array}$ | $-27 v$ | $\begin{array}{r} 1.5 \\ \leq V_{\text {IN }} \\ 0.1 \end{array}$ | $\begin{array}{r} 3.0 \\ -38 \mathrm{~V} \\ 1.0 \\ 0.5 \end{array}$ | mA |
| Output noise voltage | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{gathered}$ |  | 600 |  |  | 600 |  | $\mu \mathrm{V}$ |
| Long term stability |  |  | 96 |  |  | 96 |  | mV |
| Ripple rejection | $\begin{gathered} f=120 \mathrm{~Hz} \\ \text { IOUT }=20 \mathrm{~mA} \end{gathered}$ | $\begin{array}{l\|l\|l} -28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-38 \mathrm{~V} \\ 54 & 60 \\ \hline 5 \end{array}$ |  |  | $\begin{aligned} & -28 \mathrm{~V} \leq \mathrm{V}_{\mathbb{N}} \leq-38 \mathrm{~V} \\ & 54 \\ & \hline \end{aligned}$ |  |  | dB |
| Dropout voltage | $\begin{gathered} \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ \text { lout }=1.0 \mathrm{~A} \end{gathered}$ |  | 1.1 |  |  | 1.1 |  | v |
| Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 28 |  |  | 28 |  | $\mathrm{m} \Omega$ |
| los | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 500 |  |  | 500 |  | mA |
| Peak output current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 2.1 |  |  | 2.1 |  | A |
| Average temperature coefficient of input voltage | $\mathrm{lout}=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \mid-1.0 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T} \leq 125^{\circ} \mathrm{C} \\ -1.0 \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE

1. $7900 \mathrm{C}-0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$

## EQUIVALENT CIRCUIT


resistor values in $\Omega$ unless otherwise noted.

## TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES (Cont'd)


## TYPICAL PERFORMANCE CURVES (Cont'd)



NOTE
The other $\mu \mathrm{A} 7900$ series devices have similar performance curves.

## DESCRIPTION

The $\mu A 78 G$ and $\mu A 79 G$ are Four-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 1.0 A with a maximum input voltage of 40 V for the positive regulator 78 G and -40 V for the negative regulator 79 G . Output current capability can be increased to greater than 1.0A through use of one or more external transistors. The output voltage range of the 78 G positive voltage regulator is 5 V to 30 V and the output voltage range of the negative 79 G is -30 V to -2.2 V . For systems requiring both positive and negative voltages, the 78 G and 79 G are excellent for use as a dual tracking regulator with appropriate external circuitry.

EQUIVALENT SCHEMATIC


FEATURES

- Output current in excess of 1.0A
- $\mu A 78$ G positive output voltages 5 to 30 V
- $\mu A 79 G$ negative output voltage -30 to $-2.2 \mathrm{~V}$
- Internal thermal overload protection
- Internal short circuit current protection
- Output transistor safe area protection
- Available in 4-Pin TO-202 package

PIN CONFIGURATIONS


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Input voltage $\mu \mathrm{A} 78 \mathrm{GC}$ $\mu \mathrm{A} 9 \mathrm{GGC}$ <br> Control pin voltage $\mu \text { A78GC }$ $\mu \mathrm{A} 79 \mathrm{GC}$ <br> Power dissipation <br> Operating junction temperature range <br> Commercial ( $\mu$ A78GC, $\mu$ A79GC) <br> Storage temperature range <br> 4 -pin power TAB (U1) <br> Lead temperature <br> 4-pin power TAB (U1) (Soldering, 10s) | $\begin{gathered} 40 \\ -40 \\ 0 \leq \mathrm{V} \leq \mathrm{V} \text { OUT } \\ -\mathrm{V} \text { OUT } \leq-\mathrm{V} \leq 0 \\ \text { Internally limited } \\ 0 \text { to } 150 \\ -55 \text { to }+150 \\ 230 \end{gathered}$ | V <br> V <br> ${ }^{\circ} \mathrm{C}$ <br> ${ }^{\circ} \mathrm{C}$ <br> ${ }^{\circ} \mathrm{C}$ |

BLOCK DIAGRAM


DC ELECTRICAL CHARACTERISTICS $\mu \mathrm{A} 78 \mathrm{GC}-0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}$, Iout $=500 \mathrm{~mA}$,
Test circuit 1, unless otherwise specified. $1,2,3$

| PARAMETER | TEST CONDITIONS | $\mu \mathrm{A} 8 \mathrm{GGC}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Input voltage range | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | 7.5 |  | 40 | V |
| Output voltage range Output voltage tolerance | $\begin{gathered} \hline V_{\text {IN }}=V_{\text {OUT }}+5 \mathrm{~V} \\ \left(V_{\text {OUT }}+3 \mathrm{~V}\right) \leq V_{\text {IN }} \leq\left(V_{\text {OUT }}+15 \mathrm{~V}\right), \\ T_{J}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq I_{\mathrm{A}} \\ \text { PO } \leq 15 \mathrm{~W}, \mathrm{~V}_{\text {IN }}(\mathrm{MAX})=38 \mathrm{~V} \end{gathered}$ | 5.0 |  | $\begin{aligned} & 30 \\ & 4.0 \\ & 5.0 \end{aligned}$ | V <br> \%VOUT <br> \%Vout |
| Line regulation |  |  |  | $\begin{gathered} 1.0 \\ 0.75 \\ 0.67 \\ \hline \end{gathered}$ | \%VOUT <br> \%Vout <br> \%Vout |
| Load regulation | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C}, 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \\ \mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}+5 \mathrm{~V} \\ \mathrm{~T}_{J}=25^{\circ} \mathrm{C}, \mathrm{~V}_{\text {IN }}=\mathrm{VOUT}^{2}+5 \mathrm{~V} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \end{gathered}$ |  |  | $\begin{aligned} & 1.0 \\ & 2.0 \end{aligned}$ | \%Vout <br> \%Vout |
| Control pin current | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 1.0 | $\begin{aligned} & \hline 5.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Quiescent current | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 3.2 | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple rejection | $\begin{gathered} 8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 18 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz} \\ \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V} \\ \hline \end{gathered}$ | 62 | 78 |  | dB |
| Output noise voltage | $\begin{gathered} T_{J}=25^{\circ} \mathrm{C}, \\ 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \text { VOUT }=5 \mathrm{~V} \end{gathered}$ |  | 40 |  | $\mu \mathrm{V}$ |
| Dropout voltage |  |  |  | 2.5 | V |
| Short circuit current Peak output current | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{~V}_{1 \mathrm{~N}}=30 \mathrm{~V} \\ \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{array}{r} 750 \\ 2.2 \end{array}$ |  | $\underset{A}{\mathrm{~mA}}$ |
| Temperature coefficient of Vout | $\mathrm{V}_{\text {OUT }}=5 \mathrm{~V}$, IOUT $=5 \mathrm{~mA}$ |  | -1.1 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Control pin voltage ( reference) | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ | $\begin{gathered} \hline 4.8 \\ 4.75 \end{gathered}$ | 5.0 | $\begin{gathered} \hline 5.2 \\ 5.25 \end{gathered}$ | $\begin{aligned} & \hline v \\ & v \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS $\begin{aligned} \mu \mathrm{A} 79 \mathrm{GC}-0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=-10 \mathrm{~V}, \text { lout }=500 \mathrm{~mA}, \\ \text { Test circuit } 2 \text {, unless otherwise specified } 1,2,3\end{aligned}$

| PARAMETER | TEST CONDITIONS | $\mu A 79 \mathrm{CC}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Input voltage range Output voltage range | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}-5 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & -40 \\ & -30 \end{aligned}$ |  | $\begin{gathered} \hline-7.0 \\ -2.23 \end{gathered}$ | $\begin{aligned} & \hline \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Output voltage tolerance | $\begin{gathered} \left(V_{\text {OUT }}-15 \mathrm{~V}\right) \leq \mathrm{V}_{\text {IN }} \leq(\text { VOUT }-3 \mathrm{~V}), \\ T_{J}=25^{\circ} \mathrm{C} \end{gathered}$ |  |  |  | \%(Vout) |
|  | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IOUT } \leq 1 \mathrm{~A} \\ \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}, \mathrm{~V}_{\text {IN }}(\mathrm{MAX})=-38 \mathrm{~V} \end{gathered}$ |  |  | 5.0 | \%(Vout) |
| Line regulation | $\begin{gathered} T_{J}=25^{\circ} \mathrm{C}, \text { VOUT } \geq-10 \mathrm{~V} \\ \text { (VOUT }-20 \mathrm{~V}) \leq \mathrm{V}_{\text {IN }} \leq(\text { V OUT }-2.5 \mathrm{~V} \text { ) } \\ T_{J}=25^{\circ} \mathrm{C}, \text { VOUT } \leq-10 \mathrm{~V} \\ \text { (VOUT }-15 \mathrm{~V}) \leq \mathrm{V}_{\text {IN }} \leq \text { (VOUT }-3 \mathrm{~V} \text { ) } \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 1.0 \\ 0.75 \\ \hline \end{gathered}$ | $\%$ (VOUT) <br> \%(Vout) |
| Load regulation | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{VOUT} \leq-10 \mathrm{~V} \\ \text { (VOUT }-7 \mathrm{~V}) \leq \mathrm{V}_{\text {IN }} \leq(\text { VOUT }-3 \mathrm{~V}) \\ \mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{~V}_{\text {IN }}=V_{\text {OUT }}-5 \mathrm{~V} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \\ \hline \end{gathered}$ |  |  | $\begin{array}{r} 0.67 \\ 1.0 \end{array}$ | $\%$ (VOUT) <br> \%(VOUT) |
|  | $\begin{gathered} \mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}-5 \mathrm{~V} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ \hline \end{gathered}$ |  |  | 2.0 | \%(Vout) |
| Control pin current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 0.4 | $\begin{aligned} & 2.0 \\ & 3.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Quiescent current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | . 5 | $\begin{aligned} & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple rejection | $\begin{aligned} -18 \mathrm{~V} & \leq \mathrm{V}_{\text {IN }} \leq-8 \mathrm{~V} \\ \mathrm{~V}_{\text {OUT }} & =-5 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz} \end{aligned}$ | 50 | 60 |  | dB |
| Output noise voltage | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, |  |  |  |  |
| Dropout voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$, V ${ }_{\text {OUT }}=-5 \mathrm{~V}$ |  | 125 | 2.3 | $\begin{aligned} & \hline \mu \mathrm{V} \\ & \mathrm{~V} \\ & \hline \end{aligned}$ |
| Short circuit current | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{V}_{\text {IN }}=-30 \mathrm{~V}$ |  | 500 |  | mA |
| Peak output current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 2.2 |  | A |
| Temperature coefficient of output voltage | $\mathrm{V}_{\text {OUT }}=-5 \mathrm{~V}$, IOUT $=5 \mathrm{~mA}$ |  | -0.4 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Control pin voltage (reference) | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\begin{aligned} & -2.32 \\ & -2.35 \\ & \hline \end{aligned}$ | -2.23 | $\begin{aligned} & -2.14 \\ & -2.11 \end{aligned}$ | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |

NOTES

1. VOUT is defined for the 78 GC as $\mathrm{V}_{\text {OUT }}=\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 2}$ (5.0); The 79 GC as
$V_{\text {OUT }}=\frac{R 1+R 2}{R 2}(-2.23)$.
2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by $5 \%$ of its initial value.
3. The convention for negative is the algebraic value, thus -15 is less than -10 V .

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


## DESCRIPTION

The 78HV00 series of monolithic ThreeTerminal Positive Voltage Regulators employ 60 volt input breakdown, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current, (78HV00 series) and 500mA ( 78 MHV 00 series). They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

## FEATURES

- Input voltage greater than $\mathbf{6 0}$ volts
- No external components
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Available in the TO-220, the TO-3, and the TO-39 package
- Output voltages of $5,6,8,12,13.8,15,18$, and 24 volts

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Input voltage (5V through 24V) <br> Internal power dissipation1 <br> Storage temperature range <br> Operating junction temperature range 2 <br> 78HVO0, 78MHV00 | 60 | V |
| 78HVO0C, 78MHV00C <br> SA78HV00C, SA78MHV00C <br> Lead temperature <br> TO-3 package <br> (soldering, 60 second time limit) <br> TO-220 package <br> (soldering, 10 second time limit) | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. Thermal resistance of the packages (without a heat sink)

Junction to case: TO-3 package $4^{\circ} \mathrm{C} / \mathrm{W}$; TO-220 package $2^{\circ} \mathrm{C} / \mathrm{W}$, TO-39 package $20^{\circ} \mathrm{C} / \mathrm{W}$
Junction to ambient: $T O-3$ package $35^{\circ} \mathrm{C} / \mathrm{W}$; TO-220 package $50^{\circ} \mathrm{C} / \mathrm{W}$,
TO-39 package $170^{\circ} \mathrm{C} / \mathrm{w}$
2. Operating ambient temperature range
$\begin{array}{ll}78 \mathrm{HV} 00 & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ 78 \mathrm{HV} 00 \mathrm{C} & 0^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}\end{array}$
SA 78 HVOOC $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

PIN CONFIGURATIONS


## DA PACKAGE (TO-3)



ORDER INFORMATION

| OUTPUT | ORDER |
| :---: | :---: |
| VOLTAGE | PART NO. |
| 5 V | 78HV05DA |
| 6 V | 78HV06DA |
| 8 V | 78HV08DA |
| 12 V | 78HV12DA |
| 13.8 V | 78HV14DA |
| 15 V | 78HV15DA |
| 18 V | 78HV18DA |
| 24 V | 78HV24DA |
| 5 V | 78HV05CDA/SA78HV05CDA |
| 6 V | 78HV06CDA/SA78HV06CDA |
| 8 V | 78HV08CDA/SA78HV08CDA |
| 12 V | 78HV12CDA/SA78HV12CDA |
| 13.8 V | 78HV14CDA/SA78HV14CDA |
| 15 V | 78HV15CDA/SA78HV15CDA |
| 18 V | 78HV18CDA/SA78HV18CDA |
| 24 V | 78HV24CDA/SA78HV24CDA |

DB PACKAGE (TO-39)

EQUIVALENT SCHEMATIC


DC ELECTRICAL CHARACTERISTICS IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78HV051 |  |  | 78HV05C 1 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $\begin{gathered} \text { Over temp., } 15 \mathrm{~mA} \leq \text { lout } \leq 1.0 \mathrm{~A}, \\ P_{D} \leq 15 \mathrm{~W} \end{gathered}$ | $\begin{gathered} 4.8 \\ 8 \mathrm{~V} \\ 4.65 \\ \hline \end{gathered}$ | $\begin{aligned} & N=10 \\ & 5.0 \\ & V_{\text {IN }} \leq \end{aligned}$ | $\begin{gathered} 5.2 \\ 20 \mathrm{~V} \\ 5.35 \end{gathered}$ | $\begin{array}{r} 4.8 \\ 7 \backslash \\ 4.75 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{IN}=1 \\ & 5.0 \\ & \mathrm{~V}_{\mathrm{IN}} \end{aligned}$ | $\begin{gathered} 5.2 \\ 25 \mathrm{~V} \\ 5.25 \end{gathered}$ | v V |
|  | Line regulation |  |  | $\mathrm{V}_{\text {IN }} \leq$ 3 $\mathrm{~V}_{\text {IN }} \leq$ 1 | $\begin{gathered} 25 \mathrm{~V} \\ 50 \\ 2 \mathrm{~V} \\ 25 \end{gathered}$ |  | VIN 3 $\mathrm{~V}_{\text {IN }}$ 1 | $\begin{gathered} 25 \mathrm{~V} \\ 100 \\ 12 \mathrm{~V} \\ 50 \end{gathered}$ | mV <br> mV |
|  | Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq 1 \text { OUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq 1 \text { OUT } \leq 750 \mathrm{~mA} \\ \hline \end{gathered}$ |  | $\begin{gathered} 15 \\ 5 \end{gathered}$ | $\begin{aligned} & 50 \\ & 25 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 15 \\ 5 \\ \hline \end{gathered}$ | $\begin{gathered} 100 \\ 50 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Icc |  |  |  | 4.2 | 6.0 |  | 4.2 | 8.0 | mA |
| $\Delta \mathrm{ICC}$ |  | Over temp., 1 with line With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ |  | $\mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} 5 \mathrm{~V} \\ 0.8 \\ 0.5 \end{gathered}$ |  | VIN | $\begin{gathered} 25 \mathrm{~V} \\ 1.3 \\ 0.5 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 40 |  |  | 40 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 20 |  |  | 20 | mV |
|  | Ripple rejection | Over temp., $1 \mathrm{f}=120 \mathrm{~Hz}$ | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 18 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 18 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
|  | Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 17 |  |  | 17 |  | $\mathrm{m} \Omega$ |
| Isc |  |  |  | 750 |  |  | 750 |  | mA |
|  | Peak output current |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout | Output temperature drift | IOUT $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} \\ -1.1 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ -1.1 \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}$, Cout $^{\mathrm{C}}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.


NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{TJ}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00 $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{COUT}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.


## NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00 $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS (Cont'd) lout $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.


NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00 $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{I N}=0.33 \mu \mathrm{~F}$, Cout $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{j}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78HV141 |  |  | 78HV14C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
|  | utput voltag |  |  | $\mathrm{V}_{\mathrm{IN}}=22 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=22 \mathrm{~V}$ |  |  | V |
|  |  |  | 13.3 | 13.8 |  | 13.3 | 13.8 |  |  |
|  |  | $\begin{gathered} \text { Over temp. }, 15 \mathrm{~mA} \leq \text { lout } \leq 1.0 \mathrm{~A}, \\ \mathrm{PD}_{\mathrm{D}} \leq 15 \mathrm{~W} \end{gathered}$ | $17.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 29 \mathrm{~V}$ |  |  | $16.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 29 \mathrm{~V}$ |  |  | V |
|  | Line regulation |  | $16.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $16.5 \mathrm{~V} \leq \mathrm{V}_{10} \leq 30 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 10 | 140 |  | 10 | 280 | mV |
|  |  |  | $19 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $19 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 3 | 70 |  | 3 | 140 | mV |
|  | Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { lout } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { lout } \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 140 \\ & 70 \end{aligned}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 280 \\ & 140 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.3 | 6.0 | 4.3 8.0 |  |  | mA |
| $\Delta \mathrm{lcc}$ |  | Over temp., 1 with line With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ |  | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} 30 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{gathered}$ | 16.5 | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{array}{r} \leq 30 \mathrm{~V} \\ 1.0 \\ 0.5 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 85 |  |  | 85 |  | $\mu \mathrm{V}$ |
| Voltage drift |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 56 |  |  | 56 | mV |
| Ripple rejection |  | Over temp., $1 \mathrm{f}=120 \mathrm{~Hz}$ | $17 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 27 \mathrm{~V}$ |  |  | $17 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 27 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage | lout $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | $\checkmark$ |
|  | Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 18 |  |  | 18 |  | $\mathrm{m} \Omega$ |
| Isc |  |  |  | 350 |  |  | 350 |  | mA |
|  | Peak output current |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout | Output temperature drift | lout $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \mid-1.0 \end{gathered}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \|-1.0\| \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

notes

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00
$0^{\circ} \mathrm{C} \leq T_{J} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{Cout}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.


NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00
$0^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}_{\mathrm{O}}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78HV181 |  |  | 78HV18C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\mathrm{V}_{1 \mathrm{~N}}=27 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=27 \mathrm{~V}$ |  |  |  |
|  |  | Over temp., $15 \mathrm{~mA} \leq$ IOUT $\leq 1.0 \mathrm{~A}$, $\mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}$ | $\begin{gathered} 17.3\|18.0\| 18.7 \\ 22 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 33 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 17.3\|18.0\| 18.7 \\ 21 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 33 \mathrm{~V} \end{gathered}$ |  |  | V |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | 17.1 |  | 18.9 | v |
| Line regulation |  |  | $21 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 33 \mathrm{~V}$$\|15\| 180$$24 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $\begin{array}{c\|c} 21 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq 33 \mathrm{~V} \\ \|15\| 360 \\ 24 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V} \end{array}$ |  |  |  |
|  |  |  |  |  |  | mV |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  | 5 | 90 |  |  |  |  | 5 | 180 | mV |
| Load regulation |  | $5 \mathrm{~mA} \leq$ IOUT $\leq 1.5 \mathrm{~A}$ |  | 12 | 180 |  |  |  |  | 12 | 360 | mV |
|  |  | $250 \mathrm{~mA} \leq$ IOUT $\leq 750 \mathrm{~mA}$ |  | 4 | 90 |  | 4 | 180 | mV |
| Icc |  |  |  | 4.5 | 6.0 |  | 4.5 | 8.0 | mA |
| $\Delta \mathrm{lcc}$ |  | Over temp., 1 with line With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | $22 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 33 \mathrm{~V}$ |  |  | $21 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 33 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 0.8 |  |  | 1.0 | mA |  |
|  |  |  |  | 0.5 |  |  | 0.5 | mA |  |
| Output noise voltage |  |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 110 |  |  | 110 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 72 |  |  | 72 | mV |
| Ripple rejection |  | Over temp., $1 \mathrm{f}=120 \mathrm{~Hz}$ | $22 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 32 \mathrm{~V}$ |  |  | $22 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 32 \mathrm{~V}$ |  |  | dB |
|  |  | 59 | 69 |  | 53 | 69 |  |  |
|  | Dropout voltage |  | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance |  | $\mathrm{f}=1 \mathrm{kHz}$ |  | 22 |  |  | 22 |  | $\mathrm{m} \Omega$ |
| Isc |  |  |  | 200 |  |  | 200 |  | mA |
| Peak output current |  |  |  | 2.1 |  |  | 2.1 |  | A |
| Vout | Output temperature drift | Iout $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ -1.0 \mid \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

## NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}$, Cout $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78HV241 |  |  | 78HV24C ${ }^{1}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $\begin{gathered} \text { Over temp., } 15 \mathrm{~mA} \leq \text { lout } \leq 1.0 \mathrm{~A}, \\ P_{D} \leq 15 \mathrm{~W} \\ \hline \end{gathered}$ | $\mathrm{V}_{\mathrm{IN}}=33 \mathrm{~V}$ |  |  | $\mathrm{VIN}=33 \mathrm{~V}$ |  |  |  |
|  |  | 23.0 |  | 24.0 | 25.0 | 23.0 |  | 25.0 | v |
|  |  | $\begin{aligned} & 28 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 38 \mathrm{~V} \\ & 22.8 \mathrm{l} \mid \\ & \hline 25.2 \end{aligned}$ |  |  | $28 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 38 \mathrm{~V}$ |  |  |  |  |
|  | Line regulation |  |  | $\begin{gathered} 27 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 38 \mathrm{~V} \\ 18 \quad \mid 240 \\ 30 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 36 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 27 V \leq V_{\text {IN }} \leq 38 V \\ \mid 18 \\ \mid \quad 480 \\ 30 V \leq V_{\text {IN }} \leq 36 V \end{gathered}$ |  |  |  |
|  |  |  | mV |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 6 | 120 |  | 6 | 240 | mV |
|  | Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IOUT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq 1 \text { Out } \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 480 \\ & 240 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.6 | 6.0 |  | 4.6 | 8.0 | mA |
| $\Delta \mathrm{lcc}$ |  | Over temp., ${ }^{1}$ with line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | $28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | $27 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  |  |
|  |  |  |  |  |  |  | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |  |
| Output noise voltage |  |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 170 |  |  | 170 |  | $\mu \mathrm{V}$ |
| Voltage drift |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 96 |  |  | 96 | mV |
| Ripple rejection |  | Over temp., $1 \mathrm{f}=120 \mathrm{~Hz}$ | $28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | $28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | dB |
|  |  | 56 | 66 |  | 50 | 66 |  |  |
|  | Dropout voltage |  | IOUT $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance |  | $\mathrm{f}=1 \mathrm{kHz}$ |  | 28 |  |  | 28 |  | $\mathrm{m} \Omega$ |
| Isc |  |  |  | 150 |  |  | 150 |  | mA |
| Peak output current |  |  |  | 2.1 |  |  | 2.1 |  | A |
| Vout | Output temperature drift | IOUT $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \|-1.5\| \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

## NOTES

1. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 HV 00 $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78 HVOOC

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}$, COUT $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78HV05C2 |  |  | SA78HV06C ${ }^{2}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $25 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$,$P_{D} \leq 15 W$ | $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=11 \mathrm{~V}$ |  |  |  |
|  |  | $4.8 \left\lvert\, \begin{aligned} & \mid \\ & 7 V \leq V_{I N} \leq 25 \mathrm{~V} \end{aligned}\right.$ |  |  | $5.75 \mid$ $6.0 \mid$ <br> $8 \mathrm{~V} \leq \mathrm{V}$ IN $\leq 25 \mathrm{~V}$  |  |  | v |  |
|  |  |  |  |  |  |  |  |
|  |  | 4.65 |  |  |  |  |  | 5.35 | 5.65 |  | 6.35 | V |
|  | Line regulation |  |  |  |  |  | $\begin{aligned} & 8 V \leq V_{I N} \leq 25 \mathrm{~V} \\ & 5 \\ & 9 \mathrm{~V} \leq V_{I N} \leq 13 \mathrm{~V} \end{aligned}$ |  |  |  |
|  |  |  | mV |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 1 | 50 |  | 1.5 |  | mV |
|  | Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { lout } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \leq \text { IOUT } \leq 750 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 15 \\ 5 \end{gathered}$ | $\begin{aligned} & 100 \\ & 50 \end{aligned}$ |  | $\begin{gathered} 14 \\ 4 \end{gathered}$ | $\begin{aligned} & 120 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.2 | 8.0 |  | 4.3 | 8.0 | mA |
| $\Delta \mathrm{lcc}$ |  | Over temp., 2 with line With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | $7 \mathrm{~V} \leq \mathrm{V}_{1 \times} \leq 25 \mathrm{~V}$ |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  | 0.8 |  |  | 0.8 |  | mA |  |
|  |  |  | 0.3 |  |  | 0.3 |  | mA |  |
| Output noise voltage |  |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 40 |  |  | 45 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 20 |  |  | 24 | mV |
| Ripple rejection |  | Over temp., $2 \mathrm{f}=120 \mathrm{~Hz}$ | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 18 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 19 \mathrm{~V}$ |  |  |  |
|  |  | 62 | 78 |  | 59 | 75 |  | dB |  |
| Dropout voltage |  |  | lout $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
| Output resistance |  | $\mathrm{f}=1 \mathrm{kHz}$ |  | 17 |  |  | 19 |  | $\mathrm{m} \Omega$ |
| Isc |  |  |  | 750 |  |  | 550 |  | mA |
| Peak output current |  |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout | Output temperature drift | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \text { lout }=5 \mathrm{~mA} \end{gathered}$ |  | -1.1 |  |  | -0.8 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

notes
2. $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ for SA78HVOOC

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{CoUt}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78HV08C2 |  |  | SA78HV12C2 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=19 \mathrm{~V}$ |  |  |  |
|  |  | $\begin{gathered} \text { Over temp., } 25 \mathrm{~mA} \leq \text { lout } \leq 1.0 \mathrm{~A}, \\ P_{D} \leq 15 \mathrm{~W} \\ \hline \end{gathered}$ | $\begin{array}{l\|l\|l} 7.7\|8.0\| & 8.3 \\ 10.5 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq 23 \mathrm{~V} \\ 7.6 & 8.4 \end{array}$ |  |  | $\begin{gathered} 11.5\|12.0\| 12.5 \\ 14.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{N}} \leq 27 \mathrm{~V} \end{gathered}$ |  |  | v |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | 11.4 |  | 12.6 | V |
|  |  |  | $10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V}$ |  |  |  |  |  | $14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  |  |
| Line regulation |  |  |  | 6 | 160 |  | 10 | 240 | mV |
|  |  |  | $11 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ |  |  | $16 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 22 \mathrm{~V}$ |  |  |  |
|  |  |  |  | 2 | 80 |  | 3 | 120 | mV |
|  | Load regulation | $\begin{gathered} 5 \mathrm{~mA} \leq \text { IouT } \leq 1.5 \mathrm{~A} \\ 250 \mathrm{~mA} \end{gathered} \leq \text { Iout } \leq 750 \mathrm{~mA} .$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & 160 \\ & 80 \end{aligned}$ |  | $\begin{gathered} 12 \\ 4 \end{gathered}$ | $\begin{aligned} & \hline 240 \\ & 120 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.3 | 8.0 |  | 4.3 | 8.0 | mA |
| $\Delta \mathrm{lcc}$ |  | Over temp., 2 with line With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  |  |
|  |  |  |  |  |  | $\begin{aligned} & 0.8 \\ & 0.3 \end{aligned}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |  |
|  | Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 52 |  |  | 75 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 32 |  |  | 48 | mV |
| Ripple rejection |  |  | $11.5 \mathrm{~V} \leq \mathrm{V}_{1 \mathrm{~N}} \leq 21.5 \mathrm{~V}$ |  |  | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  | Over temp., $2 \mathrm{f}=120 \mathrm{~Hz}$ | 56 | 72 |  | 61 | 71 |  | dB |
|  | Dropout voltage | Iout $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
|  | Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 16 |  |  | 18 |  | $\mathrm{m} \Omega$ |
| Isc |  |  |  | 450 |  |  | 350 |  | mA |
|  | Peak output current |  |  | 2.2 |  |  | 2.2 |  | A |
| Vout | Output temperature drift | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ \text { IOUT }=5 \mathrm{~mA} \end{gathered}$ |  | -0.8 |  |  | -1.0 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES
2. $-40^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq+125^{\circ} \mathrm{C}$ for SA78HVOOC

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=5 \mathrm{~mA} \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}$, CoUT $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78HV14C2 |  |  | SA78HV15C² |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | $\mathrm{V}_{\mathrm{IN}}=22 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=23 \mathrm{~V}$ |  |  |  |
|  |  | $\begin{gathered} \text { Over temp., } 25 \mathrm{~mA} \leq \text { lout } \leq 1.0 \mathrm{~A} \\ P_{D} \leq 15 \mathrm{~W} \end{gathered}$ | $\begin{array}{c\|c\|c} 13.3 \mid 13.8 & 14.3 \\ 16.5 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq 29 \mathrm{~V} \\ 13.15 & & 14.95 \end{array}$ |  |  | 14.4 |  | 15.6 | v |
|  |  |  |  |  |  | 17.5 | $\leq \mathrm{V}_{\mathrm{IN}}$ | 30 V |  |
|  |  |  |  |  |  | 14.25 |  | 15.75 | v |
|  | Line regulation |  | $\begin{gathered} 16.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ 10 \mid 280 \\ 19 \mathrm{~V} \leq \mathrm{VIN} \leq 25 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 17.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V} \\ 11 \\ 20 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V} \end{gathered}$ |  |  |  |
|  |  |  |  |  |  | mV |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  | 3 | 140 |  |  |  |  | 3 | 150 | mV |
|  | Load regulation | $5 \mathrm{~mA} \leq$ IOUT $\leq 1.5 \mathrm{~A}$ |  | 12 | 280 |  |  |  |  | 12 | 150 | mV |
|  |  | $250 \mathrm{~mA} \leq 1$ IOUT $\leq 750 \mathrm{~mA}$ |  | 4 | 140 |  | 4 | 75 | mV |
| ICC |  |  |  | 4.3 | 8.0 |  | 4.4 | 8.0 | mA |
| Icc |  | Over temp., 2 with line With load, $5 \mathrm{~mA} \leq$ lout $\leq 1.0 \mathrm{~A}$ | $16.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $17.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  |  |
|  |  |  | 0.8 |  |  | 0.8 |  | mA |  |
|  |  |  | 0.3 |  |  | 0.3 |  | mA |  |
| Output noise voltage |  |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 85 |  |  | 90 |  | $\mu \mathrm{V}$ |
| Voltage drift |  |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 56 |  |  | 60 | mV |
| Ripple rejection |  |  | $17 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 27 \mathrm{~V}$ |  |  | $18.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 28.5 \mathrm{~V}$ |  |  | dB |
|  |  | Over temp., $2 \mathrm{f}=120 \mathrm{~Hz}$ | 60 | 70 |  | 60 | 70 |  |  |
|  | Dropout voltage | Iout $=1.0 \mathrm{~A}$ |  | 2.0 |  |  | 2.0 |  | V |
|  | Output resistance | $\mathrm{f}=1 \mathrm{kHz}$ |  | 18 |  |  | 19 |  | $\mathrm{m} \Omega$ |
| ISC | Peak output current |  |  | 350 |  |  | 230 |  | mA |
|  |  |  |  | 2.2 |  |  | 2.1 |  | A |
| Vout | Output temperature drift | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} \\ \text { IOUT }=5 \mathrm{~mA} \end{gathered}$ |  | -1.0 |  |  | -1.0 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES
2. $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ for SA78HVOOC

## 

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUt $=5 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{\mathrm{I}}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.


NOTES
2. $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ for SA 78 HV 00 C

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{COUT}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78MHV053 |  |  | 78MHV05C3 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., ${ }^{5} 5 \mathrm{~mA} \leq 1$ Out $\leq 350 \mathrm{~mA}$ | $\begin{gathered} V_{\text {IN }}=10 \mathrm{~V} \\ 4.8 \mathrm{~V} .0 \text { । } 5.2 \\ 8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 4.8 \\ 7 V \end{gathered}$ | IN $=1$ 5.0 $\leq V_{\text {IN }}$ | $5.2$ <br> 20 V 525 | V |
|  | Line regulation | lout $=200 \mathrm{~mA}$ | $\begin{aligned} & 7 V \leq V_{\text {IN }} \leq 25 V \\ & 1 \\ & 8 V \leq V_{\text {IN }} \leq 20 V \end{aligned}$ |  |  | $\begin{array}{c\|c} 7 \mathrm{~V} \leq \mathrm{VIN}_{\mathrm{IN}} \leq 25 \mathrm{~V} \\ 3 & 100 \\ 8 \mathrm{~V} \leq \mathrm{VIN}_{\text {IN }} \leq 25 \mathrm{~V} \\ \hline \end{array}$ |  |  | mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { lout } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 1 \\ & \hline 20 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{array}{r} 25 \\ \hline 50 \\ 25 \\ \hline \end{array}$ |  | $\begin{aligned} & \frac{1}{20} \\ & 10 \end{aligned}$ | $\begin{gathered} 50 \\ \hline 100 \\ 50 \\ \hline \end{gathered}$ | $\frac{m V}{m V}$ |
| Icc |  |  |  | 4.5 | 6.0 |  | 4.5 | 6.0 | mA |
| $\begin{aligned} & \Delta \mathrm{Icc} \\ & \Delta \mathrm{Icc} \end{aligned}$ | With line With load | $\begin{gathered} \text { Over temp., } 3 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { IouT } \leq 350 \mathrm{~mA} \\ \hline \end{gathered}$ |  | $\mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} 25 \mathrm{~V} \\ 0.8 \\ 0.5 \end{gathered}$ |  | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{gathered} 25 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 40 |  |  | 40 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 20 |  |  | 20 | mV |
| Ripple rejection |  | Over temp., $3 \mathrm{f}=120 \mathrm{~Hz}$ |  |  |  | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 18 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage |  |  | 2.0 |  |  | 2.0 |  | $\checkmark$ |
| Isc |  | $\mathrm{V}_{\mathrm{IN}}=35 \mathrm{~V}$ |  | 300 |  |  | 300 |  | mA |
| Peak output current |  |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | Iout $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE
3. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 MHV 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78MHVOOC

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{COUT}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78MHV063 |  |  | 78MHV06C3 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., ${ }^{\text {5 }} 5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | V VIN $=11 \mathrm{~V}$ |  |  | VIN $=11 \mathrm{~V}$ |  |  |  |
|  |  |  |  |  |  |  |  | 6.25 | v |
|  |  | $9{ }^{9} \mathrm{~V}$ |  |  |  | 8.0 | $\leq \mathrm{V}_{\text {IN }}$ |  |  |
|  |  | 5.7 |  |  | 6.3 | 5.7 |  | 6.3 | V |
|  | Line regulation | lout $=200 \mathrm{~mA}$ | $8 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$$1 \leq 5 \quad 160$$9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 20 \mathrm{~V}$ |  |  |  |  |  |  |
|  |  |  |  |  |  | mV |  |
|  |  |  |  | 1.5 | 30 |  |  |  | mV |
|  | Load regulation | $5 \mathrm{~mA} \leq$ IOUT $\leq 500 \mathrm{~mA}$ |  | 20 | 60 |  |  |  |  | 20 | 120 | mV |
|  |  | $5 \mathrm{~mA} \leq$ IOUT $\leq 200 \mathrm{~mA}$ |  | 10 | 30 |  | 10 | 60 | mV |
| Icc |  |  |  | 4.5 | 6.0 |  | 4.5 | 8.0 | mA |
| $\begin{array}{r} \Delta \mathrm{ICc} \\ \Delta \mathrm{Icc} \\ \hline \end{array}$ | With line With load | $\begin{gathered} \text { Over temp., } 3 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { Iout } \leq 350 \mathrm{~mA} \end{gathered}$ | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  |   0.8 <br>   0.5 |  |  |  0.8 <br>  0.5 |  |  | mA |
|  |  |  |  |  |  | mA |  |
| Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 45 |  |  |  |  |  | 45 |  | $\mu \mathrm{V}$ |
| Voltage drift |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 24 |  |  | 24 | mV |
| Ripple rejection |  | Over temp., $3 \mathrm{f}=120 \mathrm{~Hz}$ | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 19 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 19 \mathrm{~V}$ |  |  |  |
|  |  | 59 | 80 |  | 59 | 80 |  | dB |  |
| Dropout voltage |  |  |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 270 |  |  | 270 |  | mA |
| Peak output current |  |  |  | 700 |  |  | 700 |  | mA |
|  |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ |  |  |  |
| Vout | Output temperature drift | lout $=5 \mathrm{~mA}$ |  | -0.5 |  |  | -0.5 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE
3. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 MHV 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78 MHV 00 C

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{CoUT}^{\mathrm{I}}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78MHV083 |  |  | 78MHV08C3 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $35 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ |  |  |  | $7.7 \mid{ }^{\mathrm{V} / \mathrm{N}=14 \mathrm{~V}} 8.0$8.3 $10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 23 \mathrm{~V}$,7.6 |  |  | $\begin{aligned} & v \\ & \mathrm{v} \\ & \hline \end{aligned}$ |
| Line regulation |  | lout $=200 \mathrm{~mA}$ | $\begin{gathered} 10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V} \\ 6 \\ 6 \\ 11 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 20 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 10.5 \leq V_{\text {IN }} \leq 25 V \\ 6 \\ 11 V \leq V_{\text {IN }} \leq 25 V \end{gathered}$ |  |  | mV |
| Load regulation |  | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { I OUT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 80 \\ & 40 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} 160 \\ 80 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| ICC |  |  |  | 4.6 | 6.0 |  | 4.6 | 6.0 | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{lcc}$ | With line With load | $\begin{gathered} \text { Over temp., } 3 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { lout } \leq 350 \mathrm{~mA} \\ \hline \end{gathered}$ | 11.5 | $\leq \mathrm{V}_{\mathrm{IN}}$ | $\begin{array}{r} 25 \mathrm{~V} \\ 0.8 \\ 0.5 \end{array}$ | 10.5 | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{array}{r} 25 \mathrm{~V} \\ 0.8 \\ 0.5 \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 52 |  |  | 52 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 32 |  |  | 32 | mV |
|  | Ripple rejection | Over temp., $3 \mathrm{f}=120 \mathrm{~Hz}$ | $11.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 21.5 \mathrm{~V}$ |  |  | $11.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 21.5 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 250 |  |  | 250 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | lout $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} \\ \begin{array}{c} -0.5 \\ \hline \end{array} \\ \hline \end{gathered}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ <br> -0.5 |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

## NOTE

3. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 MHV 00 $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78 MHVOOC

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$\mu \mathrm{A} 78 \mathrm{HV} 00 / \mathrm{SA} 78 \mathrm{HV} 00 / 78 \mathrm{MHV00} / 78 \mathrm{MHV} 00 \mathrm{C}-\mathrm{DA}, \mathrm{DB}, \mathrm{U}$
DC ELECTRICAL CHARACTERISTICS (Cont'd) $I_{\text {OUT }}=350 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{CoUT}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78MHV123 |  |  | 78MHV12C3 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $35 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $$ |  |  | 11.5 14.5 11.4 | N $=1$ 12.0 $\leq V_{\text {IN }}$ | $\begin{gathered} 12.5 \\ =27 \mathrm{~V} \\ 12.6 \end{gathered}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| Line regulation |  | IOUT $=200 \mathrm{~mA}$ | $\begin{gathered} 14.5 \mathrm{~V} \leq \mathrm{VIN}_{1 \mathrm{~N}}=30 \mathrm{~V} \\ 1 / 8 \\ 16 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ 16 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \end{gathered}$ |  |  | mV |
|  |  |  | 2 | 30 |  | 2 | 50 | mV |  |
| Load regulation |  |  | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq 1 \text { OUT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 120 \\ & 60 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.8 | 6.0 |  | 4.8 | 6.0 | mA |
| $\Delta \mathrm{lcc}$ <br> $\Delta \mathrm{lcc}$ | With line With load | $\begin{gathered} \text { Over temp., } 3 \text { I OUT }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 350 \mathrm{~mA} \end{gathered}$ | 15 V | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} 30 \mathrm{~V} \\ 0.8 \\ 0.5 \end{gathered}$ | 14. | $\leq \mathrm{V}_{\text {IN }}$ | 30V 0.8 0.5 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 75 |  |  | 75 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 48 |  |  | 48 | mV |
| Ripple rejection |  | Over temp., $3 \mathrm{f}=120 \mathrm{~Hz}$ | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | dB |
| Dropout voltage |  |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  | mA |
| Peak output current |  |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | lout $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ |  |  | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C} \\ -1.0 \end{gathered}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE
3. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 1.50^{\circ} \mathrm{C}$ for 78 MHV 00 $0^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq 125^{\circ} \mathrm{C}$ for 78 MHV 00 C

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78MHV153 |  |  | 78MHV15C3 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  |  | VIN $=23 \mathrm{~V}$ |  |  | $\mathrm{V}_{\mathrm{IN}}=23 \mathrm{~V}$ |  |  |  |
|  |  | Over temp., ${ }^{\text {a }} 5 \mathrm{~mA} \leq 10 \mathrm{UT} \leq 350 \mathrm{~mA}$ | $14.4$ | 15.0 | 15.6 30 V |  |  | $15.6$ | v |
|  |  |  | 18.5 |  | 15.75 | 14.25 |  | 15.75 | V |
| Line regulation |  | IOUT $=200 \mathrm{~mA}$ | $\begin{gathered} 17.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ 10 \\ 20 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 17.5 V \leq V_{I N} \leq 30 V \\ 10 \mid 100 \\ 20 V \leq V_{\text {IN }} \leq 30 V \end{gathered}$ |  |  |  |
|  |  | mV |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  | 3 | 30 |  | 3 | 50 | mV |  |
| Load regulation |  |  | $\begin{aligned} & 5 \mathrm{~mA} \leq 1 \text { out } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq 1 \text { lout } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 150 \\ & 75 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} 150 \\ 75 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  |  | 4.8 | 6.0 |  | 4.8 | 6.0 | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{lcc}$ | With line With load |  | $\begin{gathered} \text { Over temp., } 3 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { IouT } \leq 350 \mathrm{~mA} \\ \hline \end{gathered}$ | $18.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  | $17.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  |  |
|  |  |  0.8  <br>   0.5 |  |  |  |  | 0.8 | mA |  |
|  |  |  |  |  |  |  |  | 0.5 | mA |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  |  | 90 |  |  | 90 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 60 |  |  | 60 | mV |
| Ripple rejection |  | Over temp., ${ }^{\text {f }} \mathrm{f}=120 \mathrm{~Hz}$ | $18.5 \mathrm{~V} \leq \mathrm{V}_{1 \mathrm{~N}} \leq 28.5 \mathrm{~V}$ |  |  | $18.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 28.5 \mathrm{~V}$ |  |  |  |
|  |  | 54 |  |  |  | 70 |  | dB |  |
| Dropout voltage |  |  |  |  | 2.0 |  |  | 2.0 |  | $\checkmark$ |
| Isc |  | $\mathrm{V}_{\mathrm{IN}}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  | mA |
|  |  | Iout $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ |  |  |  |
| Vout | Output temperature drift |  |  | -1.0 |  |  | -1.0 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE
3. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ for 78 MHVOO $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ for 78 MHVOOC

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{COUT}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78MHV203 |  |  | 78MHV20C3 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., ${ }^{\text {5 }} 5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\begin{gathered} 19.21 \\ 24 \mathrm{~V} \\ 19 \end{gathered}$ | $\mathrm{N}=29$ 20 $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} 20.8 \\ 35 \mathrm{~V} \\ 21 \\ \hline \end{gathered}$ | 19.2 23 19 | N $=29$ 20 $\leq V_{\text {IN }}$ | $\begin{gathered} 20.8 \\ 35 \mathrm{~V} \\ 21 \end{gathered}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
|  | Line regulation | Iout $=200 \mathrm{~mA}$ | $\begin{array}{rl} 23 V & \leq V_{\text {IN }} \leq 35 V \\ 10 & 60 \\ 24 V & \leq V_{\text {IN }} \leq 35 V \end{array}$ |  |  |  |  |  | mV mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq 1 \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq 10 \mathrm{~T} \leq 200 \mathrm{~mA} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{array}{r} 200 \\ 100 \\ \hline \end{array}$ |  | $\begin{aligned} & 30 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{array}{r} 400 \\ 200 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.9 | 6.0 |  | 4.9 | 6.0 | mA |
| $\Delta \mathrm{lcc}$ $\Delta \mathrm{lcc}$ | With line With load | $\begin{gathered} \text { Over temp., } 3 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { Iout } \leq 350 \mathrm{~mA} \\ \hline \end{gathered}$ |  | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} \hline 35 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{gathered}$ |  | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} \hline 35 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Output noise voltage |  | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 110 |  |  | 110 |  | $\mu \mathrm{V}$ |
| Voltage drift |  | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 80 |  |  | 80 | mV |
| Ripple rejection |  | Over temp., $3 \mathrm{f}=120 \mathrm{~Hz}$ | $24 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 34 \mathrm{~V}$ |  |  | $24 \mathrm{~V} \leq \mathrm{V}_{1 \mathrm{~N}} \leq 34 \mathrm{~V}$ |  |  | dB |
| Dropout voltage |  |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  | mA |
| Peak output current |  |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | IOUT $=5 \mathrm{~mA}$ | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE
3. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}$ for 78 MHV 00 $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ for 78 MHV 00 C

## DC ELECTRICAL CHARACTERISTICS

(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{=}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 78MHV243 |  |  | 78MHV24C3 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $35 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\begin{array}{r} 23.0 \\ 28 \\ 22.8 \end{array}$ | N $=3$ 24.0 VIN | $\begin{gathered} 25.0 \\ 38 \mathrm{~V} \\ 25.2 \end{gathered}$ | $\begin{array}{r} 23.0 \\ 271 \\ 22.8 \\ \hline \end{array}$ | = 24.0 VIN | 25.0 38 V 25.2 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Line regulation |  | Iout $=200 \mathrm{~mA}$ | $\begin{gathered} 27 \mathrm{~V} \leq \mathrm{V}_{\operatorname{IN}} \leq 38 \mathrm{~V} \\ \mid \quad 10 \quad 60 \\ 30 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 36 \mathrm{~V} \end{gathered}$ |  |  | $\begin{aligned} 27 \mathrm{~V} & \leq V_{\text {IN }} \leq 38 \mathrm{~V} \\ \mid & 10 \\ 28 \mathrm{~V} & \leq V_{I N} \leq 38 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
| Load regulation |  | $\begin{aligned} & 5 \mathrm{~mA} \leq 1 \text { OUT } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 240 \\ & 120 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 480 \\ & 240 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc | , |  |  | 5 | 6.0 |  | 5 | 6.0 | mA |
| $\Delta \mathrm{ICC}$ <br> $\Delta \mathrm{l}$ CC | With line With load | $\begin{gathered} \text { Over temp., } 3 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 350 \mathrm{~mA} \end{gathered}$ |  | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{gathered} \hline 38 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{gathered}$ |  | VIN | $\begin{gathered} \hline 38 \mathrm{~V} \\ 0.8 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 170 |  |  | 170 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 96 |  |  | 96 | mV |
| Ripple rejection |  | Over temp., $3 \mathrm{f}=120 \mathrm{~Hz}$ | $28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | $28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | dB |
| Dropout voltage |  |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | Iout $=5 \mathrm{~mA}$ | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{TJ}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} \\ \\ -1.2 \\ \hline \end{gathered}$ |  |  | $0^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq 125^{\circ} \mathrm{C}$ |  |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE
3. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ for 78 MHV 00 $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ for 78 MHVOOC

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78MHV05C ${ }^{4}$ |  |  | SA78MHV06C4 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., ${ }^{\text {5 }} 5 \mathrm{~mA} \leq$ IOut $\leq 350 \mathrm{~mA}$ |  |  |  | $\begin{gathered} 5.75 \\ 8.0 \\ 5.7 \end{gathered}$ | N $=1$ 6.0 $\leq V_{\text {IN }}$ | $\begin{gathered} 6.25 \\ 21 \mathrm{~V} \\ 6.3 \\ \hline \end{gathered}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
|  | Line regulation | lout $=200 \mathrm{~mA}$ | $\begin{aligned} & 7 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq 25 \mathrm{~V} \\ & 3 \\ & 3 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq 25 \mathrm{~V} \end{aligned}$ |  |  |  |  |  |  |
|  |  |  |  | 1 | 50 |  | 1.5 | 50 | mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { Iout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { Iout } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} 100 \\ 50 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 20 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 120 \\ & 60 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV} \end{gathered}$ |
| Icc |  |  |  | 4.5 | 6.0 |  | 4.5 | 8.0 | mA |
| $\begin{array}{r} \Delta \mathrm{Icc} \\ \Delta \mathrm{Icc} \\ \hline \end{array}$ | With line With load | $\begin{gathered} \text { Over temp., } 4 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { IOUT } \leq 350 \mathrm{~mA} \end{gathered}$ |  | Vin 0.6 0.6 0.3 |  |  | ¢ $\mathrm{V}_{1 \mathrm{~N}} \leq$ 0.6 0.3 |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 40 |  |  | 45 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 20 |  |  | 24 | mV |
|  | Ripple rejection | Over temp., $4 \mathrm{f}=120 \mathrm{~Hz}$ | $8 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 18 \mathrm{~V}$ |  |  | $9 \mathrm{~V} \leq \mathrm{V}_{1 \times} \leq 19 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | V IN $=35 \mathrm{~V}$ |  | 300 |  |  | 270 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}, \\ \text { IOUT }=5 \mathrm{~mA} \end{gathered}$ |  | -1.0 |  |  | -0.5 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

note
4. $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ for SA 78 MH vooc

## DC ELECTRICAL CHARACTERISTICS

(Cont'd) Iout $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}$, Cout $=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78MHV08C4 |  |  | SA78MHV12C4 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $45 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ |  |  | $\mathrm{V}_{\text {IN }}=19 \mathrm{~V}$ |  |  |  |
|  |  | $\begin{array}{cc\|c} 7.7 & 1 & 8.0 \\ 10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 23 \mathrm{~V} \end{array}$ |  |  | $\begin{array}{c\|c\|c} 11.5 \mid & 12.0 & 12.5 \\ 14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} & \leq 27 \mathrm{~V} \end{array}$ |  |  | V |  |
|  |  |  |  |  |  |  |  |
|  |  | $7.6 \mid 18.4$ |  |  |  |  |  | 11.4 |  | 12.6 | V |
|  | Line regulation | lout $=200 \mathrm{~mA}$ |  | $\begin{gathered} \hline 10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V} \\ 6 \\ 11 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 25 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \\ 8 \\ 16 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V} \end{gathered}$ |  |  |  |
|  |  |  |  |  |  |  | mV |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 2 | 50 |  |  |  |  | 2 | 50 | mV |
|  | Load regulation | $5 \mathrm{~mA} \leq$ IOUT $\leq 500 \mathrm{~mA}$ |  | 25 | 160 |  | 25 | 240 | mV |
|  |  | $5 \mathrm{~mA} \leq$ IOUT $\leq 200 \mathrm{~mA}$ |  | 10 | 80 |  | 10 | 120 | mV |
| Icc |  |  |  | 4.6 | 8.0 |  | 4.8 | 8.0 | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{lcc}$ | With line With load | $\begin{gathered} \text { Over temp., } 4 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { Iout } \leq 350 \mathrm{~mA} \end{gathered}$ | $10.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  | $14.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}$ |  |  |  |
|  |  |  |  0.6  <br> 0.3   |  |  |  | 0.6 |  | mA |
|  |  |  |  |  |  |  | 0.3 |  | mA |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 52 |  |  | 75 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 32 |  |  | 48 | mV |
|  | Ripple rejection | Over temp., $4 \mathrm{f}=120 \mathrm{~Hz}$ | $11.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 21.5 \mathrm{~V}$ |  |  | $15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 25 \mathrm{~V}$ |  |  |  |
|  |  |  | 56 | 80 |  | 55 | 80 |  | dB |
|  | Dropout voltage |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc | Peak output current | $\mathrm{V}_{\mathrm{IN}}=35 \mathrm{~V}$ |  | 250 |  |  | 240 |  | mA |
|  |  |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | $0^{\circ} \mathrm{C} \leq \mathrm{T}^{\prime} \leq+125^{\circ} \mathrm{C}$, IOUT $=5 \mathrm{~mA}$ |  | -0.5 |  |  | -1.0 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE

[^2]DC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{IOUT}^{2}=350 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=0.33 \mu \mathrm{~F}, \mathrm{Cout}^{2}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78MHV15C4 |  |  | SA78MHV20C ${ }^{4}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $45 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\begin{gathered} 14.4 \\ 17.5 \\ 14.25 \end{gathered}$ | $\mathrm{N}=23$ 15.0 $\leq \mathrm{V}_{\text {IN }}$ | $\begin{aligned} & 15.6 \\ & 30 \mathrm{~V} \\ & 15.75 \end{aligned}$ | $\begin{gathered} 19.2 \\ 23 \\ 19 \\ \hline \end{gathered}$ | N $=2$ 20 $\leq V_{\text {IN }}$ | $\begin{gathered} 20.8 \\ 35 \mathrm{~V} \\ 21 \\ \hline \end{gathered}$ | $\begin{aligned} & \text { v } \\ & \text { v } \end{aligned}$ |
|  | Line regulation | lout $=200 \mathrm{~mA}$ | $17.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V}$$10 \quad 1100$$20 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 30 \mathrm{~V}$ |  |  | $\begin{aligned} & 23 \mathrm{~V} \leq \mathrm{V} \text { IN } \leq 35 \mathrm{~V} \\ & 10 \text { \| } 100 \\ & 24 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 35 \mathrm{~V} \end{aligned}$ |  |  | mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { IouT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{aligned} & 150 \\ & 75 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \hline 30 \\ & 10 \end{aligned}$ | $\begin{aligned} & 400 \\ & 200 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 4.8 | 8.0 |  | 4.9 | 6.5 | mA |
| $\begin{aligned} & \Delta \mathrm{Icc} \\ & \Delta \mathrm{lcc} \\ & \hline \end{aligned}$ | With line With load | $\begin{gathered} \text { Over temp. }, 4 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { IouT } \leq 350 \mathrm{~mA} \end{gathered}$ | 17.5 | $\leq \mathrm{V}_{\text {IN }}$ 0.6 0.3 | 30 V |  | V $\mathrm{V}^{\text {N }}$ 0.6 0.3 |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 90 |  |  | 110 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 60 |  |  | 80 | mV |
| Ripple rejection |  | Over temp., $4 \mathrm{f}=120 \mathrm{~Hz}$ | 18.5 V 54 | VIN 70 | 28.5 V | $24 \mathrm{~V} \leq \mathrm{V}_{1 \text { I }} \leq 34 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage |  |  | 2.0 |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  |  | 240 |  | mA |
|  | Peak output current |  |  | 700 |  |  | 700 |  | mA |
| Vout | Output temperature drift | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$, Iout $=5 \mathrm{~mA}$ |  | -1.0 |  |  | -1.1 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTE
4. $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ for SA78MHVOOC

DC ELECTRICAL CHARACTERISTICS (Cont'd) Iout $=350 \mathrm{~mA}, \mathrm{C}_{\text {IN }}=0.33 \mu \mathrm{~F}, \mathrm{Cout}_{\mathrm{O}}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SA78MHV24C4 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vout | Output voltage |  | Over temp., $45 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\begin{array}{r} 23.0 \\ 271 \\ 22.8 \\ \hline \end{array}$ | N $=33$ 24.0 $\mathrm{~V}_{\text {IN }} \leq$ | $\begin{gathered} 25.0 \\ 38 \mathrm{~V} \\ 25.2 \end{gathered}$ | v |
|  | Line regulation | lout $=200 \mathrm{~mA}$ |  |  |  | mV |
|  |  |  |  |  |  | mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { IouT } \leq 200 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{array}{r} \hline 480 \\ 240 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 5 | 7 | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{Icc}$ | With line With load | $\begin{gathered} \text { Over temp., } 4 \text { lout }=200 \mathrm{~mA} \\ 5 \mathrm{~mA} \leq \text { lout } \leq 350 \mathrm{~mA} \\ \hline \end{gathered}$ |  | $\mathrm{V}_{\text {IN }} \leq$ <br> 0.6 <br> 0.3 <br> 170 | 38 V | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ |  | 170 |  | $\mu \mathrm{V}$ |
|  | Voltage drift | $\mathrm{mV} / 1000 \mathrm{hrs}$. |  |  | 96 | mV |
| Ripple rejection |  | Over temp., $4 \mathrm{f}=120 \mathrm{~Hz}$ | $28 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 38 \mathrm{~V}$ |  |  | dB |
| Dropout voltage |  |  |  | 2.0 |  | V |
| Isc |  | $\mathrm{V}_{\text {IN }}=35 \mathrm{~V}$ |  | 240 |  | mA |
| Peak output current |  |  |  | 700 |  | mA |
| Vout | Output temperature drift | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$, I OUT $=5 \mathrm{~mA}$ |  | -1.2 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

note
4. $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ for SA78MHVOOC

TYPICAL PERFORMANCE CHARACTERISTICS 78HV00
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7800C)


RIPPLE REJECTION AS A FUNCTION OF FREQUENCY


## CURRENT LIMITING CHARACTERISTICS



DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE


OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE


LOAD TRANSIENT RESPONSE


PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE


DROPOUT CHARACTERISTICS


INPUT VOLTAGE-V

LINE TRANSIENT RESPONSE




# FOUR TERMIMAL POSTIVE AND NEGATIV ADHSTABLE VOLTGE REGUMATOR 

## DESCRIPTION

The $\mu \mathrm{A} 78 \mathrm{MG}$ and $\mu \mathrm{A} 79 \mathrm{MG}$ are 4-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 500 mA with a maximum input voltage of 40 V for the positive regulator 78 MG and 40 V for the negative regulator 79MG. Output current capability can be increased to greater than 10A through use of one or more external transistors. The output voltage range of the 78MG positive voltage regulator is 5 V to 30 V and the output voltage range of the negative 79 MG is -30 V to -2.2 V . For systems requiring both a positive and negative, the 78 MG and 79 MG are excellent for use as a dual tracking regulator.

## FEATURES

- Output current in excess of 0.5A
- $\mu A 78 M G$ positive output voltage 5 to 30V
- $\mu A 79 M G$ negative output voltage -30 V to -2.2V
- Internal thermal overload protection
- Internal short circuit current protection
- Output transistor safe area protection


## PIN CONFIGURATIONS


 substrate.

H PACKAGE


ORDER INFORMATION
TYPE PART NO.
$\mu$ A79MG $\quad \mu \mathrm{A} 79 \mathrm{MGH}$
$\mu$ A79MGC $\mu$ A79MGCH

## t+NOTE

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection. 4A78MG778MGC 4799M679MGC

78MG EQUIVALENT CIRCUIT


79MG EQUIVALENT CIRCUIT

$0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ for $\mu \mathrm{A} 78 \mathrm{MGC},-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ for $\mu \mathrm{A} 78 \mathrm{MG}, \mathrm{V}_{\mathrm{IN}}=10 \mathrm{~V}$, lout $=350 \mathrm{~mA}$ unless otherwise specified. 1,2

| PARAMETER | TEST CONDITIONS ${ }^{1}$ |  | $\mu \mathrm{A} 78 \mathrm{MG}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Input voltage range |  | $25^{\circ} \mathrm{C}$ | 7.5 |  | 40 | v |
| Output voltage range Output voltage tolerance | $\begin{array}{r} \mathrm{V}_{\text {IN }}= \\ \mathrm{V}_{\text {OUT }}+3 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq \\ 5 \mathrm{~mA} \leq \\ \mathrm{PD} \leq 5 \mathrm{~W} \end{array}$ | $\begin{aligned} & \text { OUT }+5 \mathrm{~V} \\ & \text { VOUT }+15 \mathrm{~V}, \quad T_{J}=25^{\circ} \mathrm{C} \\ & \text { UT } \leq 350 \mathrm{~mA} \\ & \text { VINMAX }=38 \mathrm{~V} \\ & \end{aligned}$ | 5.0 |  | $\begin{aligned} & \hline 30 \\ & 4.0 \\ & 5.0 \end{aligned}$ | \%(Vout) \%(VOUT) |
| Line regulation | $\begin{gathered} \hline \mathrm{T}_{J}=25^{\circ} \mathrm{C}, \text { lout } \\ (\mathrm{VOUT}+2.5 \mathrm{~V}) \\ \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text {, louT } \\ \text { (VOUT }+3 \mathrm{~V} \text { ) } \\ \text { (Vout }+3 \mathrm{~V} \text { ) } \end{gathered}$ | 200 mA, VOUT $\leq 10 \mathrm{~V}$ <br> $\leq \mathrm{V}_{\text {IN }} \leq$ (VOUT +20 V ) <br> 200 mA, Vout $\geq 10 \mathrm{~V}$ <br> $\mathrm{V}_{\text {IN }} \leq$ (VOUT +15 V ) <br> $\mathrm{V}_{\text {IN }} \leq(\mathrm{VOUT}+7 \mathrm{~V})$ |  |  | $\begin{aligned} & 1.0 \\ & 0.75 \\ & 0.67 \end{aligned}$ | \%(Vout) <br> \%(Vout) <br> \%(Vout) |
| Load regulation | $5 \mathrm{~mA} \leq \text { lout } \leq$ | $=25^{\circ} \mathrm{C}$ |  |  | 1.0 | \%(VOUT) |
| Control pin current |  | ${ }^{2} 5^{\circ} \mathrm{C}$ |  | 1.0 | $\begin{aligned} & 5.0 \\ & 8.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| Quiescent current |  | $25^{\circ} \mathrm{C}$ |  | 2.8 | $\begin{aligned} & 4.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple rejection | $\begin{gathered} 8 V \leq V_{I N} \leq 18 \mathrm{~V} \\ \text { VOUT }=5 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz} \end{gathered}$ | $\begin{aligned} & \text { lout }=300 \mathrm{~mA}, T_{J}=25^{\circ} \mathrm{C} \\ & \text { lout }=100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 62 \\ & 62 \end{aligned}$ | 80 |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 1$ | \% kHz , V V Out $=5 \mathrm{~V}$ |  | 25 |  | $\mu \mathrm{V}$ |
| Dropout voltage ${ }^{2}$ |  | $\begin{aligned} & 88 \mathrm{MG} \\ & 8 \mathrm{MGC} \end{aligned}$ |  |  | $\begin{aligned} & 3.0 \\ & 2.5 \end{aligned}$ | V |
| Short circuit current Peak output current | $\begin{array}{r} \hline \mathrm{V}_{\mathrm{IN}}=35 \\ \mathrm{~T}_{\mathrm{J}} \end{array}$ | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ = & 25^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & \hline 300 \\ & 800 \end{aligned}$ |  | $\begin{aligned} & \hline \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Average temperature coefficient of output voltage <br> Control pin voltage (reference) |  | $\begin{aligned} & T=5 \mathrm{~V} \\ & =5 \mathrm{~mA} \\ & =25^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} 4.8 \\ 4.75 \end{gathered}$ | -0.5 5.0 | $\begin{gathered} 5.2 \\ 5.25 \end{gathered}$ | $\begin{gathered} \mathrm{mV} /{ }^{\circ} \mathrm{C} \\ \\ \mathrm{~V} \\ \mathrm{~V} \end{gathered}$ |

notes

2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by $5 \%$ of its initial value.

 AD基STABLE VOLTAGE REEUMATMR

DC ELECTRICAL CHARACTERISTICS $0^{\circ} \mathrm{C} \leq T_{j} \leq 125^{\circ} \mathrm{C}$ for $\mu \mathrm{A} 79 \mathrm{MGC},-55^{\circ} \mathrm{C} \leq T_{j} \leq 150^{\circ} \mathrm{C}$ for $\mu$ A79MG VIN $=-10 \mathrm{~V} \mu \mathrm{~A} 79 \mathrm{MG}$ lout $=350 \mathrm{~mA}$, unless otherwise specified.*

| PARAMETER | TEST CONDITIONS ${ }^{1}$ | $\mu \mathrm{A} 9 \mathrm{MG}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Input voltage range | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | -40 |  | -7.0 | V |
| Output voltage range <br> Output voltage tolerance | $\begin{array}{cc} V_{\text {IN }}=\text { VOUT }-5 \mathrm{~V} \\ \text { VOUT }-15 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq \text { VOUT }-3 \mathrm{~V}, & T_{J}=25^{\circ} \mathrm{C} \\ 5 \mathrm{~mA} \leq \text { OUUT } \leq 350 \mathrm{~mA} & \\ P_{D} \leq 5 \mathrm{WW}, V_{\text {IN }}(M A X)=-38 \mathrm{~V} & \\ \hline \end{array}$ | -30 |  | $\begin{gathered} \hline-2.23 \\ 4.0 \\ 5.0 \end{gathered}$ | \%(VOUT) \%(VOUT) |
| Line regulation | $\begin{gathered} \hline T_{J}=25^{\circ} \mathrm{C}, \text { IOUT }=200 \mathrm{~mA}, \text { VOUT } \geq-10 \mathrm{~V} \\ \text { (VOUT } \left.-20 \mathrm{~V}) \leq \mathrm{V}_{\text {IN }} \leq \text { (VOUT }-2.5 \mathrm{~V}\right) \\ \mathrm{TJ}_{J}=25^{\circ} \mathrm{C}, \text { lout }=200 \mathrm{~mA}, V_{\text {OUT }} \leq-10 \mathrm{~V} \\ \text { (VOUT } \left.-15 \mathrm{~V}) \leq \mathrm{V}_{\text {IN }} \leq \text { (VOUT }-3 \mathrm{~V}\right) \\ \text { (VOUT } \left.-7 \mathrm{~V}) \leq \mathrm{V}_{\text {IN }} \leq \text { (VOUT }-3 \mathrm{~V}\right) \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 1.0 \\ 0.75 \\ 0.67 \\ \hline \end{gathered}$ | \%(VOUT) <br> \%(Vout) <br> \%(Vout) |
| Load regulation | $\begin{gathered} \mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}-7 \mathrm{~V}, 5 \mathrm{~mA} \leq \text { IOUT } \leq 500 \mathrm{~mA} \\ T_{J}=25^{\circ} \mathrm{C} \end{gathered}$ |  |  | 1.0 | \%(Vout) |
| Control pin current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  |  | $\begin{aligned} & 3.0 \\ & 2.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| Quiescent current | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 0.5 | $\begin{aligned} & 1.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple rejection | $\begin{array}{cl} -18 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-8 \mathrm{~V} & \mathrm{~T}_{J}=25^{\circ} \mathrm{C}, \text { IOUT }=300 \mathrm{~mA} \\ \text { VOUT }=-5 \mathrm{~V}, f=120 \mathrm{~Hz} & \text { louT }=100 \mathrm{~mA} \end{array}$ | $\begin{aligned} & 54 \\ & 50 \\ & \hline \end{aligned}$ | 65 |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$, VOUT $=-5 \mathrm{~V}$ |  | 125 |  | $\mu \mathrm{V}$ |
| Dropout voltage ${ }^{2}$ | $\begin{gathered} \mu \mathrm{A} 79 \mathrm{MG} \\ \mu \mathrm{~A} 79 \mathrm{MGC} \end{gathered}$ |  |  | $\begin{aligned} & 2.5 \\ & 2.3 \end{aligned}$ | V |
| Short circuit current Peak output current | $\mathrm{V}_{\text {IN }}=-35 \mathrm{~V}$ |  | $\begin{aligned} & 500 \\ & 650 \end{aligned}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Average temperature coefficient of output voltage <br> Control pin voltage (reference) | $\begin{aligned} & \hline \text { VOUT }=-5 \mathrm{~V} \\ & \text { IOUT }=5 \mathrm{~mA} \\ & \mathrm{TJ}_{\mathrm{J}}=25^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & -2.32 \\ & -2.35 \end{aligned}$ | -0.4 -2.23 | $\begin{aligned} & -2.14 \\ & -2.11 \end{aligned}$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ <br> v |

*NOTE
The convention for Negative Regulators is the Algebraic value, thus $\mathbf{- 1 5}$ is less than $\mathbf{- 1 0 V}$.

## TYPICAL PERFORMANCE CHARACTERISTICS FOR $\mu$ A78MG

PEAK OUTPUT CURRENT AS A
FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE


QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE


CONTROL CURRENT AS A FUNCTION OF TEMPERATURE


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## DESCRIPTION

The $\mu \mathrm{A} 79 \mathrm{M} 00$ series of monolithic Three Terminal Negative Regulators employs internal current limiting, thermal shutdown, and safe-area compensation making them essentially indestructable. If adequate heat sinking is provided they can deliver over 500 mA output current. They are intended as fixed voltage regulators, but used uith external components, can provide adjustable output voltages and currents.

## FEATURES

- Output current up to 500 mA
- No external components
- Internal thermal overload protection
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Available in the TO-220 and the TO-39 package
- Output voltages of $-5,-5.2,-6,-8,-12$, $-15,-18$ and -24 volts
- Mil std 883B pending


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Input voltage |  |  |
| ( -5 V through -15 V ) ${ }^{\text {1 }}$ | -35 | V |
| (-20V, -24V) | -40 | V |
| Internal power dissipation | Internally limited |  |
| Storage temperature range |  |  |
| TO-39 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| TO-220 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating junction temperature range ${ }^{2}$ |  |  |
| 79 MOO | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| 79 MOOC | 0 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  |  |
| TO-39 package |  |  |
| (soldering, 60 sec ) | 300 | ${ }^{\circ} \mathrm{C}$ |
| TO-220 package |  |  |
| (soldering, 10 sec ) | 230 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. Thermal resistance of the packages (without a heat sink

Junction to case: TO-220 Package $2^{\circ} \mathrm{C} / \mathrm{W}$ TO-39 Package $20^{\circ} \mathrm{C} / \mathrm{W}$. Junction to ambient: TO-220 Package $50^{\circ} \mathrm{C} / \mathrm{W}$ TO-39 Package $170^{\circ} \mathrm{C} / \mathrm{W}$.
2. Operating ambient temperature range
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

PIN CONFIGURATIONS


EQUIVALENT CIRCUIT


DC ELECTRICAL CHARACTERISTICS
lout $=350 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{IN}}=2 \mu \mathrm{~F}$, Cout $=1 \mu \mathrm{~F}$,
unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 79M05 |  |  | 79M05C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}, \mathrm{PD} \leq 4 \mathrm{~W}$, over temp. ${ }^{*}$ | $\begin{array}{\|l\|l\|l} -5.2 & \mid-5.0 & -4.8 \\ -25 \mathrm{~V} & \leq \mathrm{V} \text { IN } \leq & -7 \mathrm{~V} \\ -5.25 & & \\ \hline \end{array}$ |  |  | $\begin{gathered} -5.2 \\ -25 y \\ -5.25 \\ \hline \end{gathered}$ | $\mathrm{N}=-1$ -5.0 $\leq \mathrm{V}_{\text {IN }}$ | $\begin{aligned} & -4.8 \\ & =-7 \mathrm{~V} \\ & -4.75 \end{aligned}$ | v |
|  | Line regulation |  | $\begin{array}{r} -25 \mathrm{~V} \leq \mathrm{VIN}^{\leq} \leq-7 \mathrm{~V} \\ 7.0 \mid 50 \\ -18 \mathrm{~V} \leq \mathrm{VIN} \leq-8 \mathrm{~V} \end{array}$ |  |  |  |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { louT } \leq 350 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 75 \\ & 50 \end{aligned}$ | 100 |  | $\begin{aligned} & 75 \\ & 50 \end{aligned}$ | 100 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| ICC |  |  |  | 1.0 | 2.0 |  | 1.0 | 2.0 | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{Icc}$ |  | With line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | -25 | $\leq$ VIN | $\begin{gathered} \hline-8 \mathrm{~V} \\ 0.4 \\ 0.4 \end{gathered}$ | -25 | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{array}{r} \hline-8 \mathrm{~V} \\ 0.4 \\ 0.4 \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{KHz}$ |  | 125 |  | 125 |  |  | $\mu \mathrm{V}$ |
| Ripple rejection |  | $f=120 \mathrm{~Hz}$ lout $=100 \mathrm{~mA}$, over temp.* |  |  |  | 50 |  |  | dB |
|  | Dropout voltage |  |  | 1.1 |  |  | 1.1 |  | V |
|  | Peak output current |  |  | 650 |  |  | 650 |  | mA |
|  | Average temperature coefficient of output voltage | IOUT $=5 \mathrm{~mA}$ |  | -0.4 |  |  | -0.4 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Isc |  | V IN $=-30 \mathrm{~V}$ |  | 140 |  |  | 140 |  | mA |

DC ELECTRICAL CHARACTERISTICS
(Cont'd)

| PARAMETER |  | TEST CONDITIONS | 79M05.2 |  |  | 79M05.2C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $5 \mathrm{~mA} \leq 10 \mathrm{~T}$, $\leq 350 \mathrm{~mA}, \mathrm{PD} \leq 4 \mathrm{~W}$, over temp. | $$ | $\mathrm{N}=-10 \mathrm{~V}$ -5.2 $\leq \mathrm{V}_{\text {IN }}$ | $\begin{aligned} & -5.4 \\ & -7 V \\ & -4.95 \\ & \hline \end{aligned}$ | -5.0 -25 -5.00 | $\mathrm{N}=-1$ -5.2 $\leq \mathrm{V}_{\text {IN }}$ | $\begin{aligned} & -5.4 \\ & -7 V \\ & -5.4 \end{aligned}$ | v v |
|  | Line regulation |  | $\begin{aligned} & -25 \mathrm{~V} \leq \mathrm{V}_{\mathbb{N}} \leq-7 \mathrm{~V} \\ & \|=7.0\| 50 \\ & -18 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-8 \mathrm{~V} \end{aligned}$ |  |  | $\begin{array}{r\|r\|r} \hline-25 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-7 \mathrm{~V} \\ \mid & 7.0 & 50 \\ -18 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-8 \mathrm{~V} \\ \mid & 3.0 & 30 \\ \hline \end{array}$ |  |  | mV mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \mathrm{louT} \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { lout } \leq 350 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 75 \\ & 52 \\ & \hline \end{aligned}$ | 100 |  | $\begin{aligned} & 75 \\ & 52 \end{aligned}$ | 100 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 1.0 | 2.0 |  | 1.0 | 2.0 | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{Icc}$ |  | With line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | -25V | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{gathered} \hline-8 \mathrm{~V} \\ 0.4 \\ 0.4 \\ \hline \end{gathered}$ |  | $\leq \mathrm{V}_{\text {IN }}$ | $\begin{array}{r} \hline-8 \mathrm{~V} \\ 0.4 \\ 0.4 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{KHz}$ |  | 125 |  |  | 125 |  | $\mu \mathrm{V}$ |
|  | Ripple rejection | $f=120 \mathrm{~Hz}$ lout $=100 \mathrm{~mA}$, over temp.* | $-18 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-8 \mathrm{~V}$ |  |  | $-18 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-8 \mathrm{~V}$ |  |  | dB |
|  | Dropout voltage |  |  | 1.1 |  |  | 1.1 |  | V |
|  | Peak output current |  |  | 650 |  |  | 650 |  | mA |
|  | Average temperature coefficient of output voltage | Iout $=5 \mathrm{~mA}$ |  | -0.4 |  |  | -0.4 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Isc |  | $\mathrm{V}_{\text {IN }}=-30 \mathrm{~V}$ |  | 140 |  |  | 140 |  | mA |

$-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$ for 79 M 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ for 79 M 00 C

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}, \mathrm{CIN}_{\mathrm{IN}}=2 \mu \mathrm{~F}$, Cout $=1 \mu \mathrm{~F}$, unless otherwise specified.


## DC ELECTRICAL CHARACTERISTICS

(Cont'd)

| PARAMETER |  | TEST CONDITIONS | 79M08 |  |  | 79M08C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}, \mathrm{PD} \leq 4 \mathrm{~W}$, over temp. | $\begin{aligned} & -8.3 \\ & -25 \mathrm{~V} \\ & -8.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { IN }=-1 \\ & -8.0 \\ & \text { VIN } \leq \end{aligned}$ | $\begin{gathered} \hline \mathrm{V} \\ -7.7 \\ -10.5 \mathrm{~V} \\ -7.6 \end{gathered}$ | $\begin{aligned} & -8.3 \\ & -25 \mathrm{~V} \\ & -8.4 \\ & \hline \end{aligned}$ | N $=-1$ -8.0 VIN $\leq$ | $\begin{gathered} \hline \mathrm{V} \\ -7.7 \\ -10.5 \mathrm{~V} \\ 7.6 \end{gathered}$ | $\begin{aligned} & \text { v } \\ & \text { v } \end{aligned}$ |
|  | Line regulation |  |  |  |  | $\begin{array}{r\|r\|c\|} \hline-25 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq & -10.5 \mathrm{~V} \\ \mid & 8.0 & 80 \\ -21 \mathrm{~V} & \leq \mathrm{V}_{\text {IN }} \leq & -11 \mathrm{~V} \\ \mid & 4.0 & 50 \end{array}$ |  |  | mV <br> mV |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { IouT } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { lout } \leq 350 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 90 \\ & 60 \end{aligned}$ | 160 |  | $\begin{aligned} & 90 \\ & 60 \end{aligned}$ | 160 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  |  | 1.0 | 2.0 |  | 1.0 | 2.0 | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{ICC}$ |  | With line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | -25V | $\leq \mathrm{V}_{\text {IN }} \leq$ | $\begin{gathered} \hline-10.5 \mathrm{~V} \\ 0.4 \\ 0.4 \\ \hline \end{gathered}$ | -25V | $\leq \mathrm{V}_{\mathrm{IN}} \leq$ | $\begin{gathered} -10.5 \mathrm{~V} \\ 0.4 \\ 0.4 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
|  | Output noise voltage <br> Ripple rejection | $\begin{gathered} 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{KHz} \\ \mathrm{f}=120 \mathrm{~Hz} \text { lout }=100 \mathrm{~mA}, \text { over temp.* } \end{gathered}$ |  |  |  |  |  |  | $\mu \mathrm{V}$ <br> dB |
|  | Dropout voltage |  |  | 1.1 |  |  | 1.1 |  | V |
|  | Peak output current | $\square$ |  | 650 |  |  | 650 |  | mA |
|  | Average temperature coefficient of output voltage | IOUT $=5 \mathrm{~mA}$ |  | -0.6 |  |  | -0.6 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Isc |  | $\mathrm{VIN}=-30 \mathrm{~V}$ |  | 140 |  |  | 140 |  | mA |

$-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$ for 79 M 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ for 79 MOO C

DC ELECTRICAL CHARACTERISTICS
(Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}, \mathrm{CIN}^{\mathrm{IN}}=2 \mu \mathrm{~F}$, COUT $=1 \mu \mathrm{~F}$,
unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 79M12 |  |  | 79M12C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $5 \mathrm{~mA} \leq$ IOUT $\leq 350 \mathrm{~mA}, \mathrm{PD} \leq 4 \mathrm{~W}$, over temp. | $\begin{array}{\|l\|l\|r} -12.5 & -12 & -11.5 \\ -30 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq & -14.5 \mathrm{~V} \\ -12.6 & & -11.4 \\ \hline \end{array}$ |  |  | $\begin{array}{r} -12.5 \\ -30 \mathrm{~V} \\ -12.6 \\ \hline \end{array}$ | $\mathrm{N}=-1$ -12 $\mathrm{~V}_{\text {IN }} \leq$ | $\begin{aligned} & -11.5 \\ & -14.5 \mathrm{~V} \\ & -11.4 \end{aligned}$ | V <br> V |
| Line regulation |  |  | $\begin{array}{r} -30 \mathrm{~V} \leq \mathrm{VIN} \leq-14.5 \mathrm{~V} \\ \left\lvert\, \begin{array}{r\|r} 8.0 & 80 \\ -25 \mathrm{~V} \leq \mathrm{VIN}^{2} \leq-15 \mathrm{~V} \end{array}\right. \end{array}$ |  |  | $\begin{array}{r\|c\|c} -30 \mathrm{~V} \leq \mathrm{VIN} \leq-14.5 \mathrm{~V} \\ \mid & 9.0 & 80 \\ -25 \mathrm{~V} & \leq \mathrm{V}_{\text {IN }} \leq-15 \mathrm{~V} \\ \left\lvert\, \begin{array}{c\|c\|c}  & 5.0 & 50 \\ \hline \end{array} \mathrm{~m}\right. \end{array}$ |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \hline \end{aligned}$ |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { IOUT } \leq 350 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 65 \\ & 45 \end{aligned}$ | 240 |  | $\begin{aligned} & 65 \\ & 45 \end{aligned}$ | 240 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| ICC |  |  |  | 1.5 | 3.0 |  | 1.5 | 3.0 | mA |
| $\begin{aligned} & \Delta \mathrm{I} \mathrm{CC} \\ & \Delta \mathrm{ICC} \end{aligned}$ |  | With line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\begin{aligned} & -30 \mathrm{~V} \leq \mathrm{V} \mathbb{N} \leq-14.5 \mathrm{~V} \\ & \\ & \\ & \hline \begin{array}{l} 0.4 \\ 0.4 \\ \hline \end{array} \end{aligned}$ |  |  | $\begin{gathered} -30 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-14.5 \mathrm{~V} \\ \\ \\ \end{gathered}$ |  |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{KHz}$ |  | 300 |  |  | 300 |  | $\mu \mathrm{V}$ |
|  | Ripple rejection | $f=120 \mathrm{~Hz}$ IOUT $=100 \mathrm{~mA}$, over temp.* | $\begin{gathered} -28.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-18.5 \mathrm{~V} \\ 50 \end{gathered}$ |  |  | $\begin{aligned} & -28.5 \mathrm{~V} \leq \mathrm{VIN} \leq-18.5 \mathrm{~V} \\ & 50 \\ & \hline \end{aligned}$ |  |  | dB |
|  | Dropout voltage |  |  | 1.1 |  |  | 1.1 |  | V |
|  | Peak output current |  |  | 650 |  |  | 650 |  | mA |
|  | Average temperature coefficient of output voltage | $\mathrm{IOUT}=5 \mathrm{~mA}$ |  | -0.8 |  |  | -0.8 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Isc |  | $\mathrm{V}_{\text {IN }}=-30 \mathrm{~V}$ |  | 140 |  |  | 140 |  | mA |

DC ELECTRICAL CHARACTERISTICS (Cont'd)

| PARAMETER |  | TEST CONDITIONS | 79M15 |  |  | 79M15C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $5 \mathrm{~mA} \leq$ IOUT $\leq 350 \mathrm{~mA}, \mathrm{PD} \leq 4 \mathrm{~W}$, over temp. ${ }^{*}$ | $\left\lvert\, \begin{gathered} V \\ -15.6 \\ -30 \mathrm{~V} \\ -15.75 \end{gathered}\right.$ | $\begin{gathered} N=-23 \\ -15 \\ \text { VIN } \leq \end{gathered}$ | $\begin{gathered} -14.4 \\ -17.5 \mathrm{~V} \\ -14.25 \end{gathered}$ | $\begin{array}{r} -15.6 \\ -30 \mathrm{~V} \\ -15.75 \end{array}$ | $\begin{gathered} N=-2 \\ -15 \\ V_{\text {IN }} \leq \end{gathered}$ | $\begin{aligned} & \mathrm{l} V \\ & -14.4 \\ & -17.5 \mathrm{~V} \\ & -14.25 \end{aligned}$ | V <br> V |
|  | Line regulation |  | $\begin{gathered} -30 \mathrm{~V} \leq \mathrm{VIN} \leq-17.5 \mathrm{~V} \\ \left\lvert\, \begin{array}{c} \text { \| } \\ 9.0 \\ -28 \mathrm{~V} \leq \mathrm{VIN} \leq-18 \mathrm{~V} \end{array}\right. \end{gathered}$ |  |  | $\begin{array}{r} -30 V \leq V_{I N} \leq-17.5 \mathrm{~V} \\ 9.0 \quad 80 \\ -28 \mathrm{~V} \leq \mathrm{VIN} \leq-18 \mathrm{~V} \end{array}$ |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { IouT } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { IouT } \leq 350 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 65 \\ & 45 \end{aligned}$ | 240 |  | $\begin{aligned} & 65 \\ & 45 \end{aligned}$ | 240 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| ICC |  |  |  | 1.5 | 3.0 |  | 1.5 | 3.0 | mA |
| $\Delta \mathrm{Icc}$ <br> $\Delta \mathrm{lcc}$ |  | With line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ | $\begin{gathered} -30 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-17.5 \mathrm{~V} \\ \\ \\ \\ \hline \end{gathered}$ |  |  | $\begin{array}{\|c\|c} -30 \mathrm{~V} \leq \mathrm{VIN} \leq-17.5 \mathrm{~V} \\ & 0.4 \\ & 0.4 \\ \hline \end{array}$ |  |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage <br> Ripple rejection | $\begin{gathered} 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{KHz} \\ \mathrm{f}=120 \mathrm{~Hz} \text { IOUT }=100 \mathrm{~mA}, \text { over temp.* } \end{gathered}$ | $$ |  |  | 375 <br> $-28.5 \mathrm{~V} \leq \mathrm{V}$ IN $\leq-18.5 \mathrm{~V}$ <br> 50    |  |  | $\mu \mathrm{V}$ $\mathrm{dB}$ |
|  | Dropout voltage |  |  | 1.1 |  |  | 1.1 |  | V |
|  | Peak output current |  |  | 650 |  |  | 650 |  | mA |
|  | Average temperature coefficient of output voltage | $\mathrm{IOUT}=5 \mathrm{~mA}$ |  | -1.0 |  |  | -1.0 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Isc |  | $\mathrm{V}_{\text {IN }}=-30 \mathrm{~V}$ |  | 140 |  |  | 140 |  | mA |

*NOTE
$-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$ for 79 M 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ for 79 M 00 C

## 

DC ELECTRICAL CHARACTERISTICS (Cont'd) IOUT $=350 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}, \mathrm{CIN}_{\mathrm{IN}}=2 \mu \mathrm{~F}, \mathrm{Cout}^{2}=1 \mu \mathrm{~F}$, unless otherwise specified.


DC ELECTRICAL CHARACTERISTICS
(Cont'd)

| PARAMETER |  | TEST CONDITIONS | 79M24 |  |  | 79M24C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vout | Output voltage |  | $5 \mathrm{~mA} \leq 1$ Iout $\leq 350 \mathrm{~mA}, \mathrm{PD} \leq 4 \mathrm{~W}$, over temp.* | $\begin{gathered} \mathrm{V} \\ -25 \\ -38 \mathrm{~V} \\ -25.2 \end{gathered}$ | N $=-33 \mathrm{l}$ -24 $\leq$ VIN $\leq$ | $\begin{gathered} -23 \\ -27 \mathrm{~V} \\ -22.8 \end{gathered}$ | $\begin{gathered} -25 \\ -38 \mathrm{~V} \\ -25.2 \end{gathered}$ | N $=-3$ -24 $\leq V_{\text {IN }} \leq$ | $\begin{aligned} & \mathrm{V} \\ & -23 \\ & -27 \mathrm{~V} \\ & -22.8 \end{aligned}$ | $\begin{aligned} & \text { v } \\ & \text { v } \end{aligned}$ |
|  | Line regulation |  | $\begin{array}{r} -38 V \leq V_{\text {IN }} \leq-27 V \\ 12 \\ 12 \\ -38 V \leq V_{\text {IN }} \leq-28 V \end{array}$ |  |  | $\begin{gathered} -38 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-27 \mathrm{~V} \\ \|=12\| r \\ -38 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-28 \mathrm{~V} \end{gathered}$ |  |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
|  | Load regulation | $\begin{aligned} & 5 \mathrm{~mA} \leq \text { lout } \leq 500 \mathrm{~mA} \\ & 5 \mathrm{~mA} \leq \text { lout } \leq 350 \mathrm{~mA} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 75 \\ & 50 \end{aligned}$ | 300 |  | $\begin{aligned} & \hline 75 \\ & 50 \\ & \hline \end{aligned}$ | 300 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Icc |  |  | $\begin{array}{r\|r} 1.5 & 3.5 \\ -38 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-27 \mathrm{~V} \\ \hline \end{array}$ |  |  | $-38 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq-27 \mathrm{~V}$ |  |  | mA |
| $\Delta \mathrm{Icc}$ $\Delta \mathrm{Icc}$ |  | With line <br> With load, $5 \mathrm{~mA} \leq$ lout $\leq 350 \mathrm{~mA}$ |  |  | $\begin{aligned} & 0.4 \\ & 0.4 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 0.4 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Output noise voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{KHz}$ |  |  | 600 |  |  | 600 | $\mu \mathrm{V}$ |
|  | Ripple rejection | $\mathrm{f}=120 \mathrm{~Hz}$ lout $=100 \mathrm{~mA}$, over temp.* | $\begin{array}{l\|l\|} \hline-38 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq-28 \mathrm{~V} \\ 50 & \\ \hline \end{array}$ |  |  |  |  |  | dB |
|  | Dropout voltage | Iout $=5 \mathrm{~mA}$ |  | 1.1 |  |  | 1.1 |  | V |
|  | Peak output current |  |  | 650 |  |  | 650 |  | mA |
|  | Average temperature coefficient of output voltage | $\mathrm{V}_{\mathrm{IN}}=-30 \mathrm{~V}$ |  | -1.0 |  |  | -1.0 |  | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Isc |  |  |  | 140 |  |  | 140 |  | mA |

*NOTE
$-55^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$ for 79 M 00
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ for 79 MOOC

## TYPICAL PERFORMANCE CHARACTERISTICS



PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE


RIPPLE REJECTION AS A FUNCTION OF FREQUENCY


OUTPUT VOLTAGE
AS A FUNCTION OF JUNCTION TEMPERATURE


OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY


RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES


TYPICAL PERFORMANCE CHARACTRISTICS (Cont'd)


## section 4 timers

5inlutirs

## FEATURES

- Turn off time less than $2 \mu \mathrm{~s}$
- Maximum operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of $\mathbf{0 . 0 0 5} \%$ per ${ }^{\circ} \mathbf{C}$
- SE555 Mil std 883A,B,C available M38510 (JAN) approved, M38510 processing available.

PIN CONFIGURATIONS


## APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | +18 | V |
| SE555 | +16 | V |
| NE555, SE555C, SA555 | 600 | mW |
| Power dissipation |  |  |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE555 | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| SA555 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE555, SE555C | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |
| Load temperature (soldering,60sec) |  |  |

## EQUIVALENT SCHEMATIC




BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=+5 \mathrm{~V}$ to +15 unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE555 |  |  | NE555/SE555C / SA555 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Supply voltage |  | 4.5 |  | 18 | 4.5 |  | 16 | V |
| Supply current (low state)1 | $\begin{aligned} & V_{C C}=5 V R_{L}=\infty \\ & V_{C C}=15 V R_{L}=\infty \end{aligned}$ |  | $\begin{gathered} \hline 3 \\ 10 \end{gathered}$ | $\begin{gathered} 5 \\ 12 \end{gathered}$ |  | $\begin{gathered} 3 \\ 10 \end{gathered}$ | $\begin{gathered} \hline 6 \\ 15 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Timing error (monostable) Initial accuracy2 Drift with temperature Drift with supply voltage | $\begin{gathered} \mathrm{R}_{\mathrm{A}}=2 \mathrm{~K} \Omega \text { to } 100 \mathrm{~K} \Omega \\ \mathrm{C}=0.1 \mu \mathrm{~F} \end{gathered}$ |  | $\begin{gathered} 0.5 \\ 30 \\ 0.05 \end{gathered}$ | $\begin{array}{r} 2.0 \\ 100 \\ 0.2 \end{array}$ |  | $\begin{aligned} & 1.0 \\ & 50 \\ & 0.1 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 0.5 \\ & \hline \end{aligned}$ | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |
| Timing error (astable) Initial accuracy² Drift with temperature Drift with supply voltage | $\begin{gathered} \mathrm{R}_{\mathrm{A}}, \mathrm{R}_{\mathrm{B}}=1 \mathrm{k} \Omega \text { to } 100 \mathrm{k} \Omega \\ \mathrm{C}=0.1 \mu \mathrm{~F} \\ \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} 1.5 \\ 90 \\ 0.15 \\ \hline \end{gathered}$ |  |  | $\begin{aligned} & 2.25 \\ & 150 \\ & 0.3 \\ & \hline \end{aligned}$ |  | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |
| Control voltage level <br> Threshold voltage | $\begin{aligned} & V_{C C}=15 V \\ & V_{C C}=5 V \\ & V_{C C}=15 V \\ & V_{C C}=5 V \end{aligned}$ | $\begin{aligned} & 9.6 \\ & 2.9 \\ & 9.4 \\ & 2.7 \end{aligned}$ | $\begin{aligned} & 10.0 \\ & 3.33 \\ & 10.0 \\ & 3.33 \end{aligned}$ | $\begin{gathered} 10.4 \\ 3.8 \\ 10.6 \\ 4.0 \end{gathered}$ | $\begin{aligned} & \hline 9.0 \\ & 2.6 \\ & 8.8 \\ & 2.4 \end{aligned}$ | $\begin{aligned} & 10.0 \\ & 3.33 \\ & 10.0 \\ & 3.33 \end{aligned}$ | $\begin{gathered} \hline 11.0 \\ 4.0 \\ 11.2 \\ 4.2 \end{gathered}$ | $\begin{aligned} & \hline V \\ & V \\ & V \\ & V \end{aligned}$ |
| Threshold current ${ }^{3}$ |  |  | 0.1 | 0.25 |  | 0.1 | 0.25 | $\mu \mathrm{A}$ |
| Trigger voltage <br> Trigger current <br> Reset voltage ${ }^{4}$ <br> Reset current <br> Reset current | $\begin{gathered} V_{C C}=15 \mathrm{~V} \\ V_{C C}=5 \mathrm{~V} \\ V_{\text {TRIG }}=0 \mathrm{~V} \\ \\ V_{\text {RESET }}=0 \mathrm{~V} \end{gathered}$ | $\begin{gathered} 4.8 \\ 1.45 \\ \\ 0.4 \end{gathered}$ | $\begin{gathered} 5.0 \\ 1.67 \\ 0.5 \\ 0.7 \\ 0.1 \\ 0.4 \end{gathered}$ | $\begin{aligned} & 5.2 \\ & 1.9 \\ & 0.9 \\ & 1.0 \\ & 0.4 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 1.1 \\ & 0.4 \end{aligned}$ | $\begin{gathered} 5.0 \\ 1.67 \\ 0.5 \\ 0.7 \\ 0.1 \\ 0.4 \end{gathered}$ | $\begin{aligned} & 5.6 \\ & 2.2 \\ & 2.0 \\ & 1.0 \\ & 0.4 \\ & 1.5 \end{aligned}$ | V <br> V <br> $\mu \mathrm{A}$ <br> V <br> mA <br> mA |
| Output voltage (low) | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V} \\ \mathrm{ISINK}=10 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{SINK}}=50 \mathrm{~mA} \\ \mathrm{I}_{\text {SINK }}=100 \mathrm{~mA} \\ \mathrm{I}_{\text {SINK }}=200 \mathrm{~mA} \\ \mathrm{VCC}_{\mathrm{CC}}=5 \mathrm{~V} \\ \mathrm{ISINK}=8 \mathrm{~mA} \\ \mathrm{I}_{\text {SINK }}=5 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 0.1 \\ 0.4 \\ 2.0 \\ 2.5 \\ \\ 0.1 \\ 0.05 \\ \hline \end{gathered}$ | $\begin{gathered} 0.15 \\ 0.5 \\ 2.2 \\ \\ 0.25 \\ 0.2 \\ \hline \end{gathered}$ |  | $\begin{gathered} 0.1 \\ 0.4 \\ 2.0 \\ 2.5 \\ \\ 0.3 \\ 0.25 \\ \hline \end{gathered}$ | $\begin{gathered} 0.25 \\ 0.75 \\ 2.5 \\ \\ 0.4 \\ 0.35 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \hline \end{aligned}$ |
| Output voltage (high) | $\begin{aligned} & \mathrm{VCC}==15 \mathrm{~V} \\ & \text { ISOURCE }=200 \mathrm{~mA} \\ & \text { ISOURCE }=100 \mathrm{~mA} \\ & V_{C C}=5 \mathrm{~V} \\ & \text { ISOURCE }=100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 13.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 13.3 \\ & \\ & 3.3 \end{aligned}$ |  | $\begin{aligned} & 12.75 \\ & 2.75 \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 13.3 \\ & 3.3 \end{aligned}$ |  | $\begin{aligned} & V \\ & V \\ & V \end{aligned}$ |
| Turn off time 5 | $\mathrm{V}_{\text {RESET }}=\mathrm{V}_{\text {CC }}$ |  | 0.5 | 2.0 |  | 0.5 |  | $\mu \mathrm{S}$ |
| Rise time of output Fall time of output Discharge leakage current |  |  | $\begin{gathered} 100 \\ 100 \\ 20 \end{gathered}$ | $\begin{aligned} & 200 \\ & 200 \\ & 100 \end{aligned}$ |  | $\begin{gathered} 100 \\ 100 \\ 20 \end{gathered}$ | $\begin{aligned} & 300 \\ & 300 \\ & 100 \end{aligned}$ | ns <br> ns <br> na |

NOTES

1. Supply current when output high typically 1 mA less.
2. Tested at $V_{C C}=5 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$.
3. This will determine the maximum value of $R_{A}+R_{B}$, for 15 V operation, the max total $R=10$ megohm, and for 5 V operation, the max total $R=3.4$ megohm.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to $0.8 \times V_{c c}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

## TYPICAL PERFORMANCE CHARACTERISTICS


lowest voltage level of trigger pulse ( $\mathrm{Xv}_{\mathrm{cc}}$ )

LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT


HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT


SUPPLY CURRENT vs SUPPLY VOLTAGE


SUPPLY VOLTAGE

LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT


DELAY TIME vs SUPPLY VOLTAGE

delay time vs TEMPERATURE


LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT


PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE


## FEATURES

- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of $\mathbf{0 . 0 0 5 \%}$ per ${ }^{\circ} \mathrm{C}$
- SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).


## APPLICATIONS

## - Precision timing

- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

PIN CONFIGURATION


## BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage |  |  |
| SE556 | +18 | V |
| NE556, SE556C, SA556 | +16 | V |
| Power dissipation | 600 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE556 | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| SA556 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE556, SE556C | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | +300 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  |  |
| (Soldering, 60 sec) |  |  |

ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=+5 \mathrm{~V}$ to +15 V unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE556 |  |  | NE556/SE556C/SA556 |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Supply voltage |  | 4.5 |  | 18 | 4.5 |  | 16 | V |
| Supply current (low state)1 | $\begin{aligned} & V_{C C}=5 V R_{L}=\infty \\ & V_{C C}=15 V R_{L}=\infty \end{aligned}$ |  | $\begin{gathered} 6 \\ 20 \end{gathered}$ | $\begin{aligned} & 10 \\ & 24 \end{aligned}$ |  | $\begin{gathered} 6 \\ 20 \end{gathered}$ | $\begin{aligned} & 12 \\ & 30 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Timing error (monostable) Initial accuracy2 Drift with temperature Drift with supply voltage | $\begin{gathered} \mathrm{R}_{\mathrm{A}}=2 \mathrm{k} \Omega \text { to } 100 \mathrm{k} \Omega \\ \mathrm{C}=0.1 \mu \mathrm{~F} \end{gathered}$ |  | $\begin{gathered} 0.5 \\ 30 \\ 0.05 \\ \hline \end{gathered}$ | $\begin{array}{r} 1.5 \\ 100 \\ 0.2 \end{array}$ |  | $\begin{gathered} 0.75 \\ 50 \\ 0.1 \\ \hline \end{gathered}$ | $\begin{array}{r} 3.0 \\ 0.5 \\ \hline \end{array}$ | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |
| Timing error (astable) Initial accuracy² Drift with temperature Drift with supply voltage | $\begin{gathered} \mathrm{R}_{\mathrm{A},} \mathrm{R}_{\mathrm{B}}=1 \mathrm{k} \Omega \text { to } 100 \mathrm{k} \Omega \\ \mathrm{C}=0.1 \mu \mathrm{~F} \\ \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} 1.5 \\ 90 \\ 0.15 \end{gathered}$ |  |  | $\begin{gathered} 2.25 \\ 150 \\ 0.3 \\ \hline \end{gathered}$ |  | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |
| Control voltage level | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 9.6 \\ & 2.9 \end{aligned}$ | $\begin{aligned} & 10.0 \\ & 3.33 \\ & \hline \end{aligned}$ | $\begin{gathered} 10.4 \\ 3.8 \end{gathered}$ | $\begin{aligned} & 9.0 \\ & 2.6 \\ & \hline \end{aligned}$ | $\begin{aligned} & 10.0 \\ & 3.33 \end{aligned}$ | $\begin{gathered} 11.0 \\ 4.0 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Threshold voltage | $\begin{aligned} & V_{C C}=15 \mathrm{~V} \\ & V_{C C}=5 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 9.4 \\ & 2.7 \end{aligned}$ | $\begin{aligned} & 10.0 \\ & 3.33 \end{aligned}$ | $\begin{gathered} 10.6 \\ 4.0 \end{gathered}$ | $\begin{aligned} & 8.8 \\ & 2.4 \end{aligned}$ | $\begin{aligned} & 10.0 \\ & 3.33 \end{aligned}$ | $\begin{gathered} 11.2 \\ 4.2 \\ \hline \end{gathered}$ | $\begin{aligned} & V \\ & V \end{aligned}$ |
| Threshold current ${ }^{3}$ |  |  | 30 | 250 |  | 30 | 250 | nA |
| Trigger voltage <br> Trigger current | $\begin{gathered} V_{C C}=15 \mathrm{~V} \\ V_{C C}=5 \mathrm{~V} \\ V_{\text {TRIG }}=0 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{gathered} 4.8 \\ 1.45 \end{gathered}$ | $\begin{gathered} 5.0 \\ 1.67 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & 5.2 \\ & 1.9 \\ & 0.9 \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 1.1 \end{aligned}$ | $\begin{gathered} 5.0 \\ 1.67 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & 5.6 \\ & 2.2 \\ & 2.0 \\ & \hline \end{aligned}$ | V <br> V <br> $\mu \mathrm{A}$ |
| Reset voltage ${ }^{5}$ Reset current Reset current | $V_{\text {RESET }}=0 \mathrm{~V}$ | 0.4 | $\begin{aligned} & \hline 0.7 \\ & 0.1 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 0.4 \\ & 1.0 \\ & \hline \end{aligned}$ | 0.4 | 0.7 <br> 0.1 <br> 0.4 | $\begin{aligned} & 1.0 \\ & 0.6 \\ & 1.5 \\ & \hline \end{aligned}$ | V <br> mA <br> mA |
| Output voltage (low) | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V} \\ \mathrm{I}_{\mathrm{SINK}}=10 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{SINK}}=50 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{SINK}}=100 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{SINK}}=200 \mathrm{~mA} \\ \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \\ \mathrm{I}_{\mathrm{SINK}}=8 \mathrm{~mA} \\ \mathrm{I}_{\text {SINK }}=5 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} 0.1 \\ 0.4 \\ 2.0 \\ 2.5 \\ \\ 0.1 \\ 0.05 \end{gathered}$ | $\begin{gathered} 0.15 \\ 0.5 \\ 2.25 \\ \\ 0.2 \\ 0.15 \end{gathered}$ |  | $\begin{aligned} & 0.1 \\ & 0.4 \\ & 2.0 \\ & 2.5 \\ & \\ & 0.25 \\ & 0.15 \end{aligned}$ | $\begin{gathered} 0.25 \\ 0.75 \\ 3.2 \\ \\ 0.3 \\ 0.25 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| Output voltage (high) | $\begin{aligned} \mathrm{V}_{\text {CC }} & =15 \mathrm{~V} \\ \text { ISOURCE } & =200 \mathrm{~mA} \\ \text { ISOURCE } & =100 \mathrm{~mA} \\ V_{C C} & =5 \mathrm{~V} \\ \text { ISOURCE } & =100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 13.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 13.3 \\ & \\ & 3.3 \end{aligned}$ |  | $\begin{aligned} & 12.75 \\ & 2.75 \\ & \hline \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 13.3 \\ & \\ & 3.3 \end{aligned}$ |  | $\begin{aligned} & V \\ & V \\ & V \end{aligned}$ |
| Rise time of output Fall time of output |  |  | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ |  | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |
| Discharge leakage current |  |  | 20 | 100 |  | 20 | 100 | nA |
| Matching characteristics ${ }^{4}$ Initial accuracy2 Drift with temperature Drift with supply voltage |  |  | $\begin{aligned} & 0.5 \\ & 10 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 0.2 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 10 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 0.5 \end{aligned}$ | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |

## NOTES

1. Supply current when output is high is typically 1.0 mA less.
2. Tested at $\mathrm{V}_{C C}=5 \mathrm{~V}$ and $\mathrm{V}_{C C}=15 \mathrm{~V}$.
3. This will determine the maximum value of $R_{A}+R_{B}$. For 15 V operation, the maximum total $R=10$ meg-ohms, and for $5 V$ operation, the max. total $R=3.4$ meg-ohms.
4. Matching charactristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.

TYPICAL PERFORMANCE CHARACTERISTICS


## FEATURES

- Turn off time less than $2 \mu \mathrm{~S}$
- Maximum operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of $0.005 \%$ per ${ }^{\circ} \mathbf{C}$


## APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

PIN CONFIGURATION


## BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING |  |
| :--- | :---: | :---: |
| Supply voltage |  | UNIT |
| SE556-1 | +18 | V |
| NE556-1, SE556-1C, SA556-1 | +16 | V |
| Power dissipation | 1.20 | W |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE556-1 | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| SA556-1 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE556-1, SE556-1C | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | +300 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  |  |
| (soldering, 60 sec) |  |  |

ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}$ to +15 V unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE556-1 |  |  | SA556-1/NE556-1/SE556-1C |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Supply voltage |  | 4.5 |  | 18 | 4.5 |  | 16 | V |
| Supply current (low state)1 | $\begin{aligned} & V_{C C}=5 V R_{L}=\infty \\ & V_{C C}=15 \mathrm{~V} R_{L}=\infty \end{aligned}$ |  | $\begin{gathered} 6 \\ 20 \end{gathered}$ | $\begin{aligned} & 10 \\ & 24 \end{aligned}$ |  | $\begin{gathered} \hline 6 \\ 20 \end{gathered}$ | $\begin{aligned} & 12 \\ & 30 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Timing error (monostable) Initial accuracy ${ }^{2}$ Drift with temperature Drift with supply voltage | $\begin{gathered} \mathrm{R}_{\mathrm{A}}=2 \mathrm{k} \Omega \text { to } 100 \mathrm{k} \Omega \\ \mathrm{C}=0.1 \mu \mathrm{~F} \end{gathered}$ |  | $\begin{gathered} 0.5 \\ 30 \\ 0.05 \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 100 \\ & 0.2 \end{aligned}$ |  | $\begin{gathered} 0.75 \\ 50 \\ 0.1 \end{gathered}$ | $\begin{aligned} & 3.0 \\ & 0.5 \end{aligned}$ | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |
| Timing error (astable) Initial accuracy² Drift with temperature Drift with supply voltage Control voltage level | $\begin{gathered} \mathrm{R}_{\mathrm{A}}, \mathrm{R}_{\mathrm{B}}=1 \mathrm{k} \Omega \text { to } 100 \mathrm{k} \Omega \\ \mathrm{C}=0.1 \mu \mathrm{~F} \\ \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{aligned} & 9.6 \\ & 2.9 \end{aligned}$ | $\begin{gathered} 1.5 \\ 90 \\ 0.15 \\ 10.0 \\ 3.33 \\ \hline \end{gathered}$ | $\begin{gathered} 10.4 \\ 3.8 \end{gathered}$ | $\begin{aligned} & 9.0 \\ & 2.6 \end{aligned}$ | $\begin{gathered} 2.25 \\ 150 \\ 0.3 \\ 10.0 \\ 3.33 \\ \hline \end{gathered}$ | $\begin{gathered} 11.0 \\ 4.0 \end{gathered}$ | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~V} \\ \hline \end{gathered}$ |
| Threshold voltage <br> Threshold current ${ }^{3}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 9.4 \\ & 2.7 \end{aligned}$ | $\begin{gathered} \hline 10.0 \\ 3.33 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 10.6 \\ 4.0 \\ 250 \\ \hline \end{gathered}$ | $\begin{aligned} & 8.8 \\ & 2.4 \end{aligned}$ | $\begin{gathered} \hline 10.0 \\ 3.33 \\ 30 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 11.2 \\ 4.2 \\ 250 \\ \hline \end{gathered}$ | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~V} \\ \mathrm{nA} \end{gathered}$ |
| Trigger voltage <br> Trigger current | $\begin{gathered} V_{C C}=15 \mathrm{~V} \\ V_{C C}=5 \mathrm{~V} \\ V_{\text {TRIG }}=0 \mathrm{~V} \end{gathered}$ | $\begin{gathered} \hline 4.8 \\ 1.45 \end{gathered}$ | $\begin{gathered} 5.0 \\ 1.67 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & 5.2 \\ & 1.9 \\ & 0.9 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 1.1 \end{aligned}$ | $\begin{gathered} \hline 5.0 \\ 1.67 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & 5.6 \\ & 2.2 \\ & 2.0 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mu \mathrm{~A} \end{gathered}$ |
| Reset voltage 5 Reset current Reset current | $\mathrm{V}_{\text {RESET }}=0 \mathrm{~V}$ | 0.4 | $\begin{aligned} & 0.7 \\ & 0.1 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 0.4 \\ & 1.0 \\ & \hline \end{aligned}$ | 0.4 | $\begin{aligned} & 0.7 \\ & 0.1 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 0.6 \\ & 1.5 \\ & \hline \end{aligned}$ | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~mA} \\ \mathrm{~mA} \\ \hline \end{gathered}$ |
| Output voltage (low) |  |  | $\begin{gathered} 0.1 \\ 0.4 \\ 0.8 \\ 2.5 \\ \\ 0.1 \\ 0.05 \\ \hline \end{gathered}$ | $\begin{gathered} 0.15 \\ 0.5 \\ 1.2 \\ \\ 0.2 \\ 0.15 \end{gathered}$ |  | $\begin{aligned} & 0.1 \\ & 0.4 \\ & 2.0 \\ & 2.5 \\ & \\ & 0.25 \\ & 0.15 \end{aligned}$ | $\begin{gathered} 0.25 \\ 0.75 \\ 2.5 \\ \\ 0.3 \\ 0.25 \end{gathered}$ | $\begin{aligned} & V \\ & v \\ & V \\ & v \\ & V \\ & v \\ & V \end{aligned}$ |
| Output voltage (high) | $\begin{aligned} V_{C C} & =15 \mathrm{~V} \\ \text { ISOURCE } & =200 \mathrm{~mA} \\ \text { ISOURCE } & =100 \mathrm{~mA} \\ V_{C C} & =5 \mathrm{~V} \\ \text { ISOURCE } & =100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 13.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 13.3 \\ & 3.3 \end{aligned}$ |  | $\begin{aligned} & 12.75 \\ & 2.75 \\ & \hline \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 13.3 \\ & 3.3 \end{aligned}$ |  | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| Turn off time ${ }^{6}$ <br> Rise time of output <br> Fall time of output | $\mathrm{V}_{\text {RESET }}=\mathrm{V}_{\text {cC }}$ |  | $\begin{aligned} & \hline 0.5 \\ & 100 \\ & 100 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 200 \\ & 200 \end{aligned}$ |  | $\begin{aligned} & \hline 0.5 \\ & 100 \\ & 100 \\ & \hline \end{aligned}$ | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{s} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| Discharge leakage current |  |  | 20 | 100 |  | 20 | 100 | nA |
| Matching characteristics ${ }^{4}$ Initial accuracy2 Drift with temperature Drift with supply voltage |  | . | $\begin{gathered} 0.5 \\ \pm 10 \\ 0.1 \end{gathered}$ | 1.0 0.2 |  | $\begin{gathered} 1.0 \\ \pm 10 \\ 0.2 \end{gathered}$ | $\begin{aligned} & 2.0 \\ & 0.5 \end{aligned}$ | $\begin{gathered} \% \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |

TYPICAL CHARACTERISTICS


NOTES

1. Supply current when output is high is typically 1.0 mA less.
2. Tested at $\mathrm{V}_{C C}=5 \mathrm{~V}$ and $\mathrm{V}_{C C}=15 \mathrm{~V}$.
3. This will determine the maximum value of $R_{A}+R_{B}$. For 15 V operation, the maximum total $R=10$ megohms, and for 5 V operation, the max. total $R=3.4$ megohms.
[^3]
## DESCRIPTION

The SA/SE/NE558 and 559 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current whereas the 559 sources current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. Astable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 and 559 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100 mA is provided in both devices.

## FEATURES

- 100 mA output current per section
- Edge triggered (no coupling capacitor)
- Output independent of trigger conditions
- Wide supply voltage range 4.5 V to 18 V
- Timer intervals from microseconds to hours
- Time period equals RC
- Military qualifications pending


## APPLICATIONS

- Sequential timing
- Time delay generation
- Precision timing
- Industrial controls
- Quad one-shot

PIN CONFIGURATION


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Supply voltage |  |  |
| SE558, SE559 | +18 | V |
| NE558, NE559 | +16 | V |
| SA558, SA559 | +16 | V |
| Power dissipation | 1.25 | W |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE558, NE559 | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| SA558, SA559 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE558, SE559 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | ${ }^{\circ} \mathrm{C}$ |  |
| Lead temperature (soldering, 60sec) |  |  |

558 EQUIVALENT CIRCUIT


## 559 EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}$ to +15 V unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE558/SE559 |  |  | NE558/NE559 SA558/SA559 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Supply voltage |  | 4.5 |  | 18 | 4.5 |  | 16 | V |
| Supply current (558) <br> (559) <br> Timing accuracy ( $\mathrm{T}=\mathrm{RC}$ ) | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=\text { Reset }=15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=\text { Reset }=15 \mathrm{~V} \\ \mathrm{R}=2 \mathrm{k} \Omega \text { to } 100 \mathrm{k} \Omega \\ \mathrm{C}=1 \mu \mathrm{~F} \end{gathered}$ |  | $\begin{gathered} 21 \\ 9 \end{gathered}$ | $\begin{aligned} & 32 \\ & 16 \end{aligned}$ |  | $\begin{aligned} & 27 \\ & 12 \end{aligned}$ | $\begin{aligned} & 36 \\ & 18 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Initial accuracy Drift with temperature Drift with supply voltage |  |  | $\begin{array}{r} 1.0 \\ 150 \\ 0.1 \\ \hline \end{array}$ | 3 |  | $\begin{gathered} 2 \\ 150 \\ 0.1 \\ \hline \end{gathered}$ |  | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ <br> \%/V |
| Trigger voltage ${ }^{1}$ Trigger current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V} \\ \text { Trigger }=0 \mathrm{~V} \end{gathered}$ | 0.8 | $\begin{gathered} 1.5 \\ 5 \end{gathered}$ | $\begin{aligned} & 2.4 \\ & 30 \end{aligned}$ | 0.8 | $\begin{gathered} 1.5 \\ 5 \end{gathered}$ | $\begin{aligned} & \hline 2.4 \\ & 100 \end{aligned}$ | $\begin{gathered} V \\ \mu \mathrm{~A} \end{gathered}$ |
| Reset voltage ${ }^{2}$ Reset current | Reset | 0.8 | $\begin{aligned} & 1.5 \\ & 50 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.4 \\ & 300 \end{aligned}$ | 0.8 | $\begin{aligned} & 1.5 \\ & 50 \\ & \hline \end{aligned}$ | 2.4 | $\begin{gathered} \mathrm{V} \\ \mu \mathrm{~A} \\ \hline \end{gathered}$ |
| Threshold voltage Threshold leakage |  |  | $\begin{gathered} 0.63 \\ 15 \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 0.63 \\ 15 \\ \hline \end{gathered}$ |  | $\begin{gathered} \mathrm{xVCC} \\ \mathrm{nA} \end{gathered}$ |
| Output voltage (558)3 | $\begin{aligned} & I_{\mathrm{L}}=10 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{L}}=100 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 0.1 \\ & 0.7 \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 1.5 \end{aligned}$ |  | $\begin{aligned} & 0.1 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \hline 0.4 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| Output voltage (559)4 | $\begin{aligned} & \mathrm{IL}=10 \mathrm{~mA} \\ & \mathrm{~L}=100 \mathrm{~mA} \end{aligned}$ | $\begin{gathered} \hline 13 \\ 12.5 \end{gathered}$ | $\begin{aligned} & \hline 13.6 \\ & 13.3 \end{aligned}$ |  | $\begin{aligned} & 12.5 \\ & 12.0 \end{aligned}$ | $\begin{aligned} & \hline 13.3 \\ & 13.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Output leakage <br> Propagation delay (558) <br> (559) |  |  | $\begin{aligned} & \hline 10 \\ & 1.0 \\ & 0.4 \end{aligned}$ |  |  | $\begin{gathered} \hline 10 \\ 1.0 \\ 0.4 \end{gathered}$ |  | $\begin{aligned} & \hline \mathrm{nA} \\ & \mu \mathrm{~S} \\ & \mu \mathrm{~S} \\ & \hline \end{aligned}$ |
| Risetime of output Falltime of output | $\begin{aligned} & I_{\mathrm{L}}=100 \mathrm{~mA} \\ & I_{\mathrm{L}}=100 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & \hline 100 \\ & 100 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to $V_{C C}$ to sink current. The output is normally low sinking current.
4. The 559 output structure is a darlington emitter follower which requires a pull down resistor to ground to source current. The output is normally low and sources current only when switched high.

## COMPARATORS

## DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the $\mu \mathrm{A} 710$. They are designed to operate over a wider range of supply voltages; from standard $\pm 15 \mathrm{~V}$ op amp supplies down to the single 5 V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50 V at currents as high as 50 mA .

Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the $\mu \mathrm{A} 710$ ( 200 ns response time vs 40 ns ) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the $\mu \mathrm{A} 710$ series.

The LH2111 series hybrids are 2 LM111 type comparators in one hermetic package. They feature the same electrical parameters as the single devices.

## FEATURES

- Operates from single 5V supply
- Maximum input bias current: 150nA (LM311-250nA)
- Maximum offset current: 20nA (LM311 50nA)
- Differential input voltage range: $\pm \mathbf{3 0 V}$
- Power consumption: 135 mW at $\pm 15 \mathrm{~V}$
- High sensitivity-200V/mV
- Military qualification pending
- LH2111 offers close thermal tracking


## PIN CONFIGURATIONS



## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Total supply voltage | 36 | V |
| Output to negative supply voltage: |  | V |
| LM111/LM211, LH2111/LH2211 | 50 | V |
| LM311, LH2311 | 40 | V |
| Ground to negative supply voltage | 30 | V |
| Differential input voltage | $\pm 30$ | V |
| Input voltage1 | $\pm 15$ | sec |
| Power dissipation2 | 500 | ${ }^{\circ} \mathrm{C}$ |
| Output short circuit duration | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| LM111, LH2111 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| LM211, LH2211 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| LM311, LH2311 | 300 |  |
| Storage temperature range |  |  |
| Lead temperature |  |  |
| (soldering, 10sec) |  |  |

DC ELECTRICAL CHARACTERISTICS
1,2,3

| PARAMETER | TEST CONDITIONS | LM111/LM211/LH2111/LH2211 |  |  | LM311/LH2311 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input offset voltage ${ }^{4}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R} \mathrm{S} \leq 50 \mathrm{k} \Omega$ |  | 0.7 | 3.0 |  | 2.0 | 7.5 | mV |
| Input offset current ${ }^{4}$ Input bias current | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & 4.0 \\ & 60 \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 10 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \hline 6.0 \\ & 100 \end{aligned}$ | $\begin{gathered} 50 \\ 250 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Voltage gain | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 200 |  |  | 200 |  | $\mathrm{V} / \mathrm{mV}$ |
| Response time ${ }^{5}$ Saturation voltage | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~V} \mathrm{IN} \leq-5 \mathrm{mV}, \text { IouT }=50 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & \hline 200 \\ & 0.75 \end{aligned}$ | 1.5 |  | $\begin{aligned} & 200 \\ & 0.75 \end{aligned}$ | . 1.5 | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~V} \end{aligned}$ |
| Strobe on current Output leakage current | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{VIN} \geq 5 \mathrm{mV}, \mathrm{~V}_{\text {OUT }}=35 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \text { ISTROBE }=3 \mathrm{~mA} \end{gathered}$ |  | $\begin{aligned} & 3.0 \\ & 0.2 \end{aligned}$ | 10 |  | $\begin{aligned} & 3.0 \\ & 0.2 \end{aligned}$ | 50 | $\mathrm{mA}$ $\mathrm{nA}$ |
| Input offset voltage ${ }^{4}$ | $\mathrm{Rs} \leq 50 \mathrm{k} \Omega$ |  |  | 4.0 |  |  | 10 | mV |
| Input offset current ${ }^{4}$ Input bias current |  |  |  | $\begin{gathered} 20 \\ 150 \end{gathered}$ |  |  | $\begin{gathered} 70 \\ 300 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| Input voltage range Saturation voltage <br> Output leakage current | $\begin{gathered} \mathrm{V}+\geq 4.5 \mathrm{~V}, \mathrm{~V}-=0 \\ \mathrm{~V}_{\mathrm{IN}} \leq-6 \mathrm{mV}, \text { ISINK } \leq 8 \mathrm{~mA} \\ \mathrm{VIN}^{2} \geq 5 \mathrm{mV}, V_{\text {OUT }}=35 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} \pm 14 \\ \\ 0.23 \\ 0.1 \end{gathered}$ | $\begin{aligned} & 0.4 \\ & 0.5 \end{aligned}$ |  | $\begin{aligned} & \pm 14 \\ & 0.23 \end{aligned}$ | 0.4 | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mu \mathrm{~A} \end{gathered}$ |
| Positive supply current Negative supply current | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & 5.1 \\ & 4.1 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 5.0 \end{aligned}$ |  | $\begin{aligned} & 5.1 \\ & 4.1 \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

NOTES

1. This rating applies for $\pm 15 \mathrm{~V}$ supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. The maximum junction temperature of the LM311, LH2311 is $110^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient, in the N package, a thermal resistance of $162^{\circ} \mathrm{C} / \mathrm{W}$, and ${ }^{\circ} \mathrm{C} / \mathrm{W}$ for the Ceramic package. The maximum junction temperature of the LM111, LH2111 is $150^{\circ} \mathrm{C}$, while that of the LM211, LH2111 is $110^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient. The thermal resistance of the Cerdip package is $110^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient.
3. These specifications apply for $V_{S}= \pm 15 \mathrm{~V}$ and $0^{\circ} \mathrm{C}<\mathrm{T}_{A}<70^{\circ} \mathrm{C}$ unless otherwise specified. With the LM211, LH2111 however, all temperature specifications are limited to $-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ and for the LM111 and LH2111 are limited to $-55^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<125^{\circ} \mathrm{C}$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to $\pm 15 \mathrm{~V}$ supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL APPLICATIONS


DETECTOR FOR MAGNETIC TRANSDUCER


TTL INTERFACE WITH HIGH LEVEL LOGIC

*Values shown are for a 0 to 30 V logic swing and a 15 V threshold.
$\dagger$ May be added to control speed and reduce susceptability to noise spikes.

## DESCRIPTION

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5 V logic supply and ground. Further, they have higher gain and lower input currents than devices like the $\mu A 710$. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA .

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to $\pm 15 \mathrm{~V}$. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the $\mu \mathrm{A} 711$.
The LM119 is specified from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, the LM219 is specified from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, and the LM319 is specified from $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$.

## FEATURES

- Two independent comparators
- Operates from a single 5 V supply
- Typically 80 ns response time at $\pm 15 \mathrm{~V}$
- Minimum fan-out of 3 (each side)
- Maximum input current of $1 \mu \mathrm{~A}$ over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate
- Mil std $\mathbf{8 8 3}$ A, B, C available

PIN CONFIGURATIONS


## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Total supply voltage | 36 | V |
| Output to negative supply voltage | 36 | V |
| Ground to negative supply voltage | 25 | V |
| Ground to positive supply voltage | 18 | V |
| Differential input voltage | $\pm 5$ | V |
| Input voltage1 | $\pm 15$ | V |
| Power dissipation2 | 500 | mW |
| Output short circuit duration | 10 | s |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| LM119 | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| LM219 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| LM319 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum rating is equal to the supply voltage.
2. The absolute maximum junction temperature is $150^{\circ} \mathrm{C}$. Device dissipation must be derated as follows
$\mathrm{N} / \mathrm{K}$ package $-150^{\circ} \mathrm{C}$ /watt above $75^{\circ} \mathrm{C}$
F package $-110^{\circ} \mathrm{C} /$ watt above $95^{\circ} \mathrm{C}$

## DC ELECTRICAL CHARACTERISTICS

LM119, $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$
LM219, $-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$
LM319, $0^{\circ} \mathrm{C} \leq T_{A} \leq 70^{\circ} \mathrm{C}$
unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | LM119/219 |  |  | LM319 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage 1,2 | $\begin{gathered} R_{S} \leq 5 K \Omega, T_{A}=25^{\circ} \mathrm{C} \\ \text { Over temp. } \end{gathered}$ |  | 0.7 | $\begin{gathered} 4.0 \\ 7 \end{gathered}$ |  | 2.0 | $\begin{aligned} & 8.0 \\ & 10 \end{aligned}$ | $\mathrm{mV}$ |
| Ios | Input offset current 1,2 | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | 30 | $\begin{gathered} 75 \\ 100 \\ \hline \end{gathered}$ |  | 80 | $\begin{aligned} & 200 \\ & 300 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IB | Input bias current 1 | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | 150 | $\begin{gathered} \hline 500 \\ 1000 \\ \hline \end{gathered}$ |  | 250 | $\begin{aligned} & \hline 1000 \\ & 1200 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| $A_{v}$ | Voltage gain | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 10 | 40 |  | 8 | 40 |  | $\mathrm{V} / \mathrm{mV}$ |
| VoL | Saturation voltage |  |  | $\begin{aligned} & 0.75 \\ & 0.23 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & \\ & 0.4 \\ & 0.6 \end{aligned}$ |  | $0.75$ $0.3$ | $1.5$ $0.4$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| IOH | Output leakage current | $\begin{gathered} \mathrm{V}-=0 \mathrm{~V}, \mathrm{~V}_{\mathbb{I N}}=5 \mathrm{mV} \\ \text { VOUT }=35 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C} \\ \text { Over temp. } \\ V-=0 \mathrm{~V}, \mathrm{VIN}^{\prime}=10 \mathrm{mV} \\ \text { VOUT }=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{gathered} 0.2 \\ 1 \end{gathered}$ | $\begin{gathered} 2 \\ 10 \end{gathered}$ |  | 0.2 | 10 | $\mu \mathrm{A}$ $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| V IN | Input voltage range | $\begin{gathered} \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V} \\ \mathrm{~V}+=5 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V} \end{gathered}$ | 1 | $\pm 13$ | 3 | 1 | $\pm 13$ | 3 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $V_{\text {ID }}$ | Differential input voltage |  |  |  | $\pm 5$ |  |  | $\pm 5$ | V |
| + ${ }_{\text {l }}^{+}$ | Positive supply current Positive supply current Negative supply current | $\begin{gathered} V^{+}=5 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ V_{S}= \pm 15 \mathrm{~V}, \mathrm{~T}_{A}=25^{\circ} \mathrm{C} \\ V_{S}= \pm 15 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 4.3 \\ & 8.0 \\ & 3.0 \end{aligned}$ | $\begin{gathered} 11.5 \\ 4.5 \end{gathered}$ |  | $\begin{aligned} & 4.3 \\ & 8.0 \\ & 3.0 \end{aligned}$ | $\begin{gathered} 12.5 \\ 5.0 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

## NOTES

1. $V_{O S}$, los and $I_{B}$ specifications apply for a supply voltage range of $V_{S}= \pm 15 \mathrm{~V}$ down to a single 5 V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1 volt of either supply with a 1 mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Response time $^{*}$ | $V_{S}= \pm 15 \mathrm{~V}, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}$ <br> $\mathrm{R}_{\mathrm{L}}=500 \Omega$ (see test figure) |  | 80 |  | ns |

*NOTE
The response time specified is for a 100 mV step with 5 mV overdrive.
TEST CIRCUIT


TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


## TYPICAL APPLICATIONS



## DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.
The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

## FEATURES

- Wide single supply voltage range 2.0 Vdc to 36 Vdc or dual supplies $\pm 1.0 \mathrm{Vdc}$ to $\pm 18 \mathrm{Vdc}$
- Very low supply current drain $(0.8 \mathrm{~mA})$ independent of supply voltage $(1.0 \mathrm{~mW} /-$ comparator at 5.0 Vdc )
- Low input biasing current 25 nA
- Low input offset currrent $\pm 5 \mathrm{nA}$ and offset voltage $\pm 3 \mathrm{mV}$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage.
- Low output 250 mV at 4 mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.


## APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| VCC supply voltage | 36 or $\pm 18$ | Vdc |
| Differential input voltage | 36 | Vdc |
| Input voltage | -0.3 to +36 | Vdc |
| Power dissipation1 | 570 | mW |
| Molded DIP | 900 | mW |
| CERDIP | Continuous |  |
| Output short circuit to ground2 | 50 | mA |
| Input current (VIN < -0.3Vdc)3 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| LM139/139A | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| LM239/239A | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| LM339/339A | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| LM2901/MC3302 | 300 | ${ }^{\circ} \mathrm{C}$ |

LM139/A/239/A/339/A/2901-F,N • MC3302-N PIN CONFIGURATION


## EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V+=5 V d c, L M 139 A / L M 139:-55^{\circ} \mathrm{C} \leq T_{A} \leq 125^{\circ} \mathrm{C}$ unless otherwise specified LM239: $-25^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq 85^{\circ} \mathrm{C}$ unless otherwise specified LM339: $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$ unless otherwise specified

| PARAMETER |  | TEST CONDITIONS | LM139 |  |  | LM239/339 |  |  | LM139A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage 5 |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. | . | $\pm 2.0$ | $\pm 5.0$ 9.0 |  | $\pm 2.0$ | $\begin{gathered} \pm 5.0 \\ 9.0 \end{gathered}$ |  | $\pm 1.0$ | $\begin{gathered} \pm 2.0 \\ 4.0 \end{gathered}$ | mV |
| VCM | Input common mode voltage range 6 | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\left\|\begin{array}{l} V+-1.5 \\ V+-2.0 \end{array}\right\|$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\left\|\begin{array}{l} \mathrm{V}+-15 \\ \mathrm{~V}+-20 \end{array}\right\|$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V}+-1.5 \\ & \mathrm{~V}+-2.0 \end{aligned}$ | V |
| VIDR | Differential input voltage ${ }^{4}$ | Keep all $\mathrm{V}_{1 \mathrm{~N}}$ s $\geq 0 \mathrm{Vdc}$ (or V -if need) |  |  | V+ |  |  | V+ |  |  | V+ | V |
| IB | Input bias current7 | $l_{i N(+)}$ or $\operatorname{liN}(-)$ with output in linear range $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | $25$ | $\begin{aligned} & 100 \\ & 300 \end{aligned}$ |  | 25 | $\begin{aligned} & 250 \\ & 400 \end{aligned}$ |  | 25 | $\begin{aligned} & 100 \\ & 300 \end{aligned}$ | nA |
| los | Input offset current | $\begin{aligned} & \ln (+)-\operatorname{IN}(-) \\ & T_{A}=25^{\circ} \mathrm{C} \end{aligned}$ <br> Over temp. |  | $\pm 3.0$ | $\begin{gathered} \pm 25 \\ \pm 100 \end{gathered}$ |  | $\pm 5.0$ | $\begin{gathered} \pm 50 \\ \pm 150 \end{gathered}$ |  | $\pm 3.0$ | $\begin{gathered} \pm 25 \\ \pm 100 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IOL | Output sink current | $\begin{gathered} \mathrm{V}_{\mathrm{IN}\left(\left(^{-}\right)\right.} \geq 1 \mathrm{Vdc}, \\ \mathrm{~V}_{\mathrm{IN}(+)}=0, \mathrm{~V}_{0} \leq 1.5 \mathrm{Vdc}, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ | 6.0 | 16 |  | 6.0 | 16 |  | 6.0 | 16 |  | mA |
| IOH | Output leakage current | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}(+)} \geq 1 \mathrm{Vdc}, \mathrm{~V}_{\operatorname{IN}(-)}=0 \\ & \mathrm{~V}_{0}=5 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{0}=30 \mathrm{Vdc}, \text { over temp. } \end{aligned}$ |  | 0.1 | 1.0 |  | 0.1 | 1.0 |  | 0.1 | 1.0 | $\begin{aligned} & \mathrm{nA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| ICC | Supply current 9 | $\mathrm{R}_{\mathrm{L}}=\infty$ on comparators, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 0.8 | 2.0 |  | 0.8 | 2.0 |  | 0.8 | 2.0 | mA |
| Av | Voltage gain | $\mathrm{R}_{\mathrm{L}} \geq 15 \mathrm{k} \Omega, \mathrm{V}+=15 \mathrm{Vdc}$ | 50 | 200 |  | 50 | 200 |  | 50 | 200 |  | $\mathrm{V} / \mathrm{mV}$ |
| VOL | Saturation voltage | $\begin{gathered} \mathrm{VIN(-)} \geq 1 \mathrm{Vdc}, \\ \mathrm{~V}_{\mathrm{IN}(+)}=0, \mathrm{ISINK} \leq 4 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \text { Over temp. } \end{gathered}$ |  | 250 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ |  | 250 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ |  | 250 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ | mV |
| TLSR | Large signal response time | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=\mathrm{TTL} \text { logic swing, } \\ \mathrm{V}_{\mathrm{REF}}=1.4 \mathrm{Vdc}, \\ \mathrm{~V}_{\mathrm{RL}}=5 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 300 |  |  | 300 |  |  | 300 |  | ns |
| TR | Response time ${ }^{8}$ | $\begin{gathered} \mathrm{V}_{\mathrm{RL}}=5 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 1.3 |  |  | 1.3 |  |  | 1.3 |  | $\mu \mathrm{S}$ |

DC ELECTRICAL CHARACTERTISICS
(Cont'd) V $+=5 \mathrm{Vdc}, \mathrm{LM} 339 \mathrm{~A}: 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$ unless otherwise specified
LM239A: $-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ unless otherwise specified LM2901/LM3302: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ unless otherwise specified

| PARAMETER |  | TEST CONDITIONS | LM239A/339A |  |  | LM2901 |  |  | MC3302 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage 5 |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | $\pm 1.0$ | $\begin{aligned} & \pm 2.0 \\ & \pm 4.0 \end{aligned}$ |  | $\begin{gathered} \pm 2.0 \\ \pm 9 \end{gathered}$ | $\begin{aligned} & \pm 7.0 \\ & \pm 15 \end{aligned}$ |  | $\pm 3.0$ | $\begin{aligned} & \pm 20 \\ & \pm 40 \end{aligned}$ | mV |
| VCM | Input common mode voltage range 6 | $T_{A}=25^{\circ} \mathrm{C}$ <br> Over temp. | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & V+-1.5 \\ & V+-2.0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | \| $\mathrm{V}+-1.5$ |  |  | $\begin{array}{\|l} \mathrm{V}+-1.5 \\ \mathrm{~V}+-2.0 \end{array}$ | V |
| VIDR | Differential input voltage ${ }^{4}$ | Keep all $\mathrm{V}_{\mathrm{IN}} \mathrm{s} \geq 0 \mathrm{Vdc}$ (or V-if need) |  |  | V+ |  |  | V+ |  |  | V+ | V |
| $I_{B}$ | Input bias current7 | $\operatorname{liN}(+)$ or $\operatorname{liN}(-)$ with output in linear range $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | 25 | $\begin{aligned} & 250 \\ & 400 \end{aligned}$ |  | $\begin{gathered} 25 \\ 200 \end{gathered}$ | $\begin{aligned} & 250 \\ & 500 \end{aligned}$ |  | 25 | $\begin{gathered} 500 \\ 1000 \end{gathered}$ | nA |
| los | Input offset current | $\begin{aligned} & \operatorname{IN}(+)-\operatorname{liN}(-) \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \text { Over temp. } \end{aligned}$ |  | $\pm 5.0$ | $\begin{gathered} \pm 50 \\ \pm 150 \end{gathered}$ |  | $\begin{gathered} \pm 5 \\ \pm 50 \end{gathered}$ | $\begin{gathered} \pm 50 \\ \pm 200 \\ \hline \end{gathered}$ |  | $\pm 5$ | $\begin{aligned} & \pm 100 \\ & \pm 300 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \hline \end{aligned}$ |
| IOL | Output sink current | $\begin{gathered} \mathrm{V}_{\operatorname{IN}(-) \geq 1 \mathrm{Vdc}} \\ \mathrm{~V}_{\mathrm{IN}(+)}=0, \mathrm{~V}_{0} \leq 1.5 \mathrm{Vdc}, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~V}_{0}=800 \mathrm{mV}, \\ \text { Over temp. } \\ \hline \end{gathered}$ | 6.0 | 16 |  | 6.0 | 16 |  | 2.0 |  |  | mA |
| IOH | Output leakage current | $\begin{gathered} V_{\operatorname{IN}(+)} \geq 1 V_{d c}, V_{\operatorname{IN}(-)}=0 \\ V_{0}=5 \mathrm{Vdc}, T_{A}=25^{\circ} \mathrm{C} \\ V_{0}=30 \mathrm{Vdc} \\ \text { Over temp. } \end{gathered}$ |  | 0.1 | 1.0 |  | 0.1 | 1.0 |  | 0.1 | 1.0 | $\begin{aligned} & \mathrm{nA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| ICC | Supply current ${ }^{9}$ | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=\infty \text { on comparators, } \\ \mathrm{V}+=5 \mathrm{Vdc} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~V}+=30 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 0.8 | 2.0 |  | $\begin{aligned} & 0.8 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.5 \end{aligned}$ |  | 0.8 | 2.0 | mA |
| AV | Voltage gain | $\mathrm{R}_{\mathrm{L}} \geq 15 \mathrm{k} \Omega, \mathrm{V}+=15 \mathrm{Vdc}$ | 50 | 200 |  | 25 | 100 |  | 2 | 100 |  | $\mathrm{V} / \mathrm{mV}$ |
| VoL | Saturation voltage | $\begin{gathered} \mathrm{VIN}(-)^{\mathrm{I}} \geq 1 \mathrm{Vdc}, \\ \mathrm{~V}_{(\mathbb{N}(+)}=0, \mathrm{IS}_{\operatorname{SNK}} \leq 4 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ <br> Over temp. $\begin{aligned} & \text { ISink }=2 \mathrm{~mA}, \mathrm{~V}+=5 \mathrm{~V} \\ & \text { to } 28 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ |  | 250 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ |  | 400 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ |  | 150 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ | mV |
| TLSR | Large signal response time | $\begin{gathered} V_{\mathbb{I N}}=\mathrm{TTL} \text { logic swing, } \\ \mathrm{V}_{\mathrm{REF}}=1.4 \mathrm{Vdc}, \\ \mathrm{~V}_{\mathrm{RL}}=5 \mathrm{Vdc}, R_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 300 |  |  | 300 |  |  | 300 |  | ns |
| TR | Response time ${ }^{8}$ | $\begin{gathered} V_{R L}=5 \mathrm{Vdc}, R_{L}=5.1 \mathrm{k} \Omega, \\ \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 1.3 |  |  | 1.3 |  |  | 1.3 |  | $\mu \mathrm{S}$ |

## NOTES

1. For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a $125^{\circ} \mathrm{C}$ maximum junction temperature and a thermal resistance of $175^{\circ} \mathrm{C} / \mathrm{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a $150^{\circ} \mathrm{C}$ maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ( $\mathrm{PD} \leq 100 \mathrm{~mW}$ ), provided the output transistors are allowed to saturate
2. Short circuits from the output to $\mathrm{V}+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of $\mathrm{V}+$.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the $\mathrm{V}+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when

LM139/A/239/A/339/A/2901-F,N • MC3302-N
the input voltage, which was negative, again returns to a value greater than -0.3 Vdc .
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 Vdc (or 0.3 Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $\mathrm{V}_{0} \cong 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}}=0 \Omega$ with $\mathrm{V}+$ from 5 Vdc to 30 Vdc ; and over the full input common-mode range ( 0 Vdc to $\mathrm{V}+-1.5 \mathrm{Vdc}$ ).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to 30 Vdc without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100 mV input step with a 5 mV overdrive. For larger overdrive signals, 300 ns can be obtained, see typical performance characteristics section.
9. The MC3302 has supply current specified with a voltage range of 5 to 28 volts

TYPICAL APPLICATIONS

## TWO-DECADE HIGH-FREQUENCY VCO



VISIBLE VOLTAGE INDICATOR


## TTL TO MOS LOGIC CONVERTER



CRYSTAL CONTROLLED OSCILLATOR


TYPICAL PERFORMANCE CHARACTERISTICS


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVESNEGATIVE TRANSITION


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVESPOSITIVE TRANSITION


## DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage: These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.
The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

## FEATURES

- Wide single supply voltage range 2.0 Vdc to 36 Vdc or dual supplies $\pm 1.0 \mathrm{Vdc}$ to $\pm 18 \mathrm{Vdc}$
- Very low supply current drain ( 0.8 mA ) independent of supply voltage $(2.0 \mathrm{~mW} /-$ comparator at 5.0 Vdc )
- Low input biasing current 25nA
- Low input offset current $\pm 5 n \mathrm{~A}$ and offset voltage $\pm 3 \mathrm{mV}$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage.
- Low output 250 mV at 4 mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.


## APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

LM193/293/393/193A/293A/393A/2903-N,T PIN CONFIGURATIONS


## EQUIVALENT CIRCUIT



LM193/293/393/193A/293A/393A/2903-N,T
DC ELECTRICAL CHARACTERISTICS $\quad \mathrm{V}+=5 \mathrm{Vdc}, \mathrm{LM} 193 / 193 \mathrm{~A}:-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ unless otherwise specified. LM293/293A: $-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ unless otherwise specified. LM393/393A: $0^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq+70^{\circ} \mathrm{C}$ unless otherwise specified. LM2903: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ unless otherwise specified. 7

| PARAMETER |  | TEST CONDITIONS | LM193A |  |  | LM293A/393A |  |  | LM2903 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage5 |  | $T_{A}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | $\pm 1.0$ | $\begin{aligned} & \pm 2.0 \\ & \pm 4.0 \end{aligned}$ |  | $\pm 1.0$ | $\begin{aligned} & \pm 2.0 \\ & \pm 4.0 \end{aligned}$ |  | $\begin{gathered} \pm 2.0 \\ \pm 9 \end{gathered}$ | $\begin{aligned} & \pm 7.0 \\ & \pm 15 \end{aligned}$ | mV |
| VCM | Input common mode voltage range6,10 | $T_{A}=25^{\circ} \mathrm{C}$ Over temp. | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\left\|\begin{array}{l} \mathrm{v}+-1.5 \\ \mathrm{v}+-2.0 \end{array}\right\|$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\left\|\begin{array}{c} \mathrm{v}+-1.5 \\ \mathrm{v}+-2.0 \end{array}\right\|$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\left.\begin{aligned} & \mathrm{v}+-1.5 \\ & \mathrm{v}+-2.0 \end{aligned} \right\rvert\,$ | V |
| VIDR | Differential input voltage ${ }^{4}$ | Keep all $\mathrm{V}_{\text {IN's }} \geq 0 \mathrm{Vdc}$ (or V-if need) |  |  | V+ |  |  | V+ |  |  | V+ | v |
| IB | Input bias current ${ }^{8}$ | $\operatorname{liN}(+)$ or $\operatorname{lin}_{(-)}^{(-)}$with output in linear range $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | 25 | $\begin{aligned} & 100 \\ & 300 \end{aligned}$ |  | 25 | $\begin{aligned} & 250 \\ & 400 \end{aligned}$ |  | $\begin{gathered} 25 \\ 200 \end{gathered}$ | $\begin{aligned} & 250 \\ & 500 \end{aligned}$ | nA |
| los | Input offset current | $\begin{aligned} & \operatorname{liN(+)}-\operatorname{liN}(-) \\ & T_{A}=25^{\circ} \mathrm{C} \end{aligned}$ <br> Over temp. |  | $\pm 3.0$ | $\begin{gathered} \pm 25 \\ \pm 100 \end{gathered}$ |  | $\pm 5.0$ | $\begin{gathered} \pm 50 \\ \pm 150 \end{gathered}$ |  | $\begin{gathered} \pm 5 \\ \pm 50 \end{gathered}$ | $\begin{gathered} \pm 50 \\ \pm 200 \end{gathered}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \end{aligned}$ |
| IoL | Output sink current | $\begin{gathered} \mathrm{V}_{\mathbb{N}(-)} \geq 1 \mathrm{Vdc}, \mathrm{~V}_{1 N_{(+)}}=0, \\ \mathrm{~V}_{0} \leq 1.5 \mathrm{Vdc}, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ | 6.0 | 16 |  | 6.0 | 16 |  | 6.0 | 16 |  | mA |
| IOH | Output leakage current | $\begin{gathered} \mathrm{V}_{\operatorname{IN}(+)} \geq 1 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{N}(-)}=0 \\ \mathrm{~V}_{0}=30 \mathrm{Vdc} \\ \text { Over temp. } \\ \mathrm{V}_{0}=5 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 0.1 | 1.0 |  | 0.1 | 1.0 |  | 0.1 | 1.0 | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{na} \end{aligned}$ |
| Icc | Supply current | $\begin{gathered} R_{L}=\infty \text { on both comparators. } \\ T_{A}=25^{\circ} \mathrm{C} \\ \mathrm{~V}+=30 \mathrm{~V}, \text { over temp. } \\ \hline \end{gathered}$ |  | $\begin{gathered} 0.8 \\ 1 \end{gathered}$ | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ |  | $\begin{gathered} 0.8 \\ 1 \end{gathered}$ | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ |  | $\begin{gathered} 0.8 \\ 1 \\ \hline \end{gathered}$ | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ | mA |
| Av | Voltage gain | $\mathrm{R}_{\mathrm{L}} \geq 15 \mathrm{k} \Omega, \mathrm{V}+=15 \mathrm{Vdc}$ | 50 | 200 |  | 50 | 200 |  | 25 | 100 |  | V/mV |
| VoL | Saturation voltage | $\begin{gathered} \mathrm{V}_{\mathrm{IN}(-)} \geq 1 \mathrm{Vdc}, \mathrm{~V}_{\operatorname{NN}(+)}=0, \\ \mathrm{I}_{\operatorname{sinK}} \leq 4 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \text { Over temp. } \end{gathered}$ |  | 250 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ |  | 250 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ |  | 400 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ | mV |
| TLSR | Large signal response time | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=\mathrm{TTL} \text { logic swing, } \\ \mathrm{V}_{\mathrm{REF}}=1.4 \mathrm{Vdc}, \\ \mathrm{~V}_{\mathrm{RL}}=5 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 300 |  |  | 300 |  |  | 300 |  | ns |
| TR | Response time ${ }^{9}$ | $\begin{gathered} \mathrm{V}_{\mathrm{RL}}=5 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \\ T_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 1.3 |  |  | 1.3 |  |  | 1.3 |  | $\mu \mathrm{S}$ |


| PARAMETER |  | TEST CONDITIONS | LM193 |  |  | LM293/393 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage ${ }^{5}$ |  | $T_{A}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | $\pm 2.0$ | $\begin{aligned} & \pm 5.0 \\ & \pm 9.0 \end{aligned}$ |  | $\pm 2.0$ | $\begin{aligned} & \pm 5.0 \\ & \pm 9.0 \end{aligned}$ | mV |
| $V_{\text {CM }}$ | Input common mode voltage range6,10 | $T_{A}=25^{\circ} \mathrm{C}$ Over temp. | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \pm-1.5 \\ & \mathrm{~V} \pm-2.0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{array}{\|} \mathrm{V} \pm-1.5 \\ \mathrm{~V} \pm-2.0 \end{array}$ | V |
| VIDR | Differential input voltage ${ }^{4}$ | Keep all $\mathrm{V}_{\text {IN's }} \geq 0 \mathrm{Vdc}$ (or V-if need) |  |  | V+ | $\because$ |  | V+ | V |
| IB | Input bias current ${ }^{8}$ | $\operatorname{lin}(+)$ or $\operatorname{lin}(-)$ with output in linear range $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Over temp. |  | 25 | $\begin{aligned} & 100 \\ & 300 \end{aligned}$ |  | 25 | $\begin{aligned} & 250 \\ & 400 \end{aligned}$ | nA |
| los | Input offset current | $\begin{gathered} \operatorname{liN}(+)-\operatorname{lin}(-) \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ <br> Over temp. |  | $\pm 3.0$ | $\begin{array}{r}  \pm 25 \\ \pm 100 \\ \hline \end{array}$ |  | $\pm 5.0$ | $\begin{gathered} \pm 50 \\ \pm 150 \\ \hline \end{gathered}$ | $\begin{aligned} & \text { nA } \\ & \text { nA } \end{aligned}$ |
| IOL | Output sink current | $\begin{gathered} \mathrm{V}_{\mathrm{IN}(-)} \geq 1 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{IN}(+)}=0, \\ \mathrm{~V}_{0} \leq 1.5 \mathrm{Vdc} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ | 6.0 | 16 |  | $6.0$ | $16$ |  | mA |
| IOH | Output leakage current | $\begin{gathered} \mathrm{V}_{\mathrm{IN}(+)} \geq 1 \mathrm{Vdc}, \mathrm{~V}_{\operatorname{IN}(-)}=0 \\ \mathrm{~V}_{0}=5 \mathrm{Vdc}, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~V}_{0}=30 \mathrm{Vdc}, \text { over temp. } \end{gathered}$ |  | 0.1 | 1.0 |  | 0.1 | $1.0$ | $\begin{aligned} & \mathrm{nA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Icc | Supply current | $\begin{gathered} R_{L}=\infty \text { on both comparators } \\ T_{A}=25^{\circ} \mathrm{C} \\ \mathrm{~V}+=30 \mathrm{~V}, \text { over temp. } \end{gathered}$ |  | 0.8 | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ |  | 0.8 | $\begin{gathered} 1 \\ 2.5 \end{gathered}$ | mA |
| Av | Voltage gain | $\mathrm{R}_{\mathrm{L}} \geq 15 \mathrm{~K} \Omega, \mathrm{~V}+=15 \mathrm{Vdc}$ | 50 | 200 |  | 50 | 200 |  | $\mathrm{V} / \mathrm{mV}$ |
| VOL | Saturation voltage | $\begin{gathered} \hline \mathrm{VIN}(-) \geq 1 \mathrm{Vdc}, \mathrm{~V}_{\operatorname{IN}(+)}=0, \\ \mathrm{I}_{\text {SINK }} \leq 4 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \text { Over temp. } \end{gathered}$ |  | 250 | $\begin{aligned} & 400 \\ & 700 \\ & \hline \end{aligned}$ | - | 250 | $\begin{aligned} & 400 \\ & 700 \end{aligned}$ | mV |
| TLSR | Large signal response time | $\begin{gathered} \mathrm{V}_{\text {IN }}=\mathrm{TTL} \text { logic swing, } \\ \mathrm{V}_{\mathrm{REF}}=1.4 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{RL}}=5 \mathrm{Vdc}, \\ \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 300 |  |  | 300 |  | ns |
| TR | Response time ${ }^{9}$ | $\begin{gathered} V_{\mathrm{RL}}=5 \mathrm{Vdc}, \\ \mathrm{RL}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 1.3 |  |  | 1.3 |  | $\mu \mathrm{S}$ |

## NOTES

1. For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a $125^{\circ} \mathrm{C}$ maximum junction temperature and a thermal resistance of $175^{\circ} \mathrm{C} / \mathrm{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a $150^{\circ} \mathrm{C}$ maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small ( $\mathrm{PD}_{\mathrm{D}} \leq 100 \mathrm{~mW}$ ), provided the output transistors are allowed to saturate.
2. Short circuits from the output to $V+$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of $\mathrm{V}+$.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the $\mathrm{V}+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 Vdc .
4. Positive excursions of input voltage may exceed the power supply level. As long as the
other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 Vdc V Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $\mathrm{V}_{0} \cong 1.4 \mathrm{Vdc}, \mathrm{Rs}_{\mathrm{s}}=0 \Omega$ with $\mathrm{V}+$ from 5 Vdc to 30 Vdc ; and over the full input common-mode range ( 0 Vdc to $\mathrm{V}+-1.5 \mathrm{Vdc}$ ).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to 30 Vdc without damage.
7. With the LM293/293A, all temperature specifications are limited to $-25^{\circ} \mathrm{C} \leq T_{A} \leq$ $+85^{\circ} \mathrm{C}$ and the LM393/393A, all temperature specifications are limited to $0^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq$ $+70^{\circ} \mathrm{C}$. The LM2903 is limited to $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$.
8. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
9. The response time specified is for a 100 mV input step with a 5 mV overdrive. For larger overdrive signals, 300 ns can be obtained, see typical performance characteristics section.
10. For input signals that exceed $V_{C C}$, only the overdriven comparator is affected. With a 5 V supply, $\mathrm{V}_{\mathbb{N}}$ should be limited to 25 V max., and a limiting resistor should be used on all inputs that might exceed the positive supply.

## FEATURES

- 12ns maximum guaranteed propagation delay
- $20 \mu \mathrm{~A}$ maximum input bias current
- TTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending


## APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver


## ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
|  | Supply voltage |  | V |
| V+ | Positive | +7 |  |
| $V$ - | Negative | -7 |  |
| $V_{\text {IDR }}$ | Differential input voltage | $\pm 6$ | V |
| $\mathrm{V}_{\text {IN }}$ | Input voltage Common mode Strobe/gate | $\begin{gathered} \pm 5 \\ +5.25 \end{gathered}$ | V |
| ${ }^{\text {PD }}$ | Power dissipation | 600 | mW |
| ${ }^{T}$ A | Operating temperature range | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| T stg | Storage temperature range Lead temperature (solder, 60 sec ) | $\begin{gathered} -65 \text { to }+150 \\ +300 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

## BLOCK DIAGRAM



EQUIVALENT SCHEMATIC


DC ELECTRICAL CHARACTERISTICS $\mathrm{V}+=+5 \mathrm{~V}, \mathrm{~V}-=-5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise specified

|  | PARAMETER | TEST CONDITIONS | LImits |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Vos | Input offset voltage At $25^{\circ} \mathrm{C}$ Over temperature range | $\mathrm{V}+=+4.75 \mathrm{~V}, \mathrm{~V}-=-4.75 \mathrm{~V}$ |  | 6 | $\begin{aligned} & 7.5 \\ & 10 \\ & \hline \end{aligned}$ | mV |
| ${ }^{\text {BIAS }}$ | Input bias current <br> At $25^{\circ} \mathrm{C}$ <br> Over temperature range | $\mathrm{V}+=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}$ |  | 7.5 | $\begin{array}{r} 20 \\ 40 \\ \hline \end{array}$ | $\mu \mathrm{A}$ |
| 'os | Input offset current <br> At $25^{\circ} \mathrm{C}$ <br> Over temperature range | $\mathrm{V}+=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}$ |  | 1.0 | $\begin{gathered} 5 \\ 12 \end{gathered}$ | $\mu \mathrm{A}$ |
| $V_{\text {CM }}$ | Common mode voltage range | $\mathrm{V}+=+4.75 \mathrm{~V}, \mathrm{~V}-=-4.75 \mathrm{~V}$ | $\pm 3$ |  |  | V |
| ${ }^{I_{I H}}$ | Input current High | $\begin{gathered} \mathrm{V}+=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V} \\ \mathrm{~V} 1 \mathrm{H}=2.7 \mathrm{~V} \\ 1 \mathrm{G} \text { or } 2 \mathrm{G} \text { strobe } \\ \text { Common strobe } \mathrm{S} \\ \hline \end{gathered}$ |  |  | $\begin{array}{r} 50 \\ 100 \\ \hline \end{array}$ | ${ }_{\mu \mathrm{A}}^{\mu \mathrm{A}}$ |
| IIL | Low | $V_{I L}=0.5 \mathrm{~V}$ <br> 1 G or 2 G strobe Common strobe S |  |  | $\begin{array}{r} -2.0 \\ -4.0 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \mathrm{v}_{\mathrm{OH}} \\ & \mathrm{v}_{\mathrm{OL}} \end{aligned}$ | Output voltage High Low | $\begin{gathered} \hline V_{I(S)}=2.0 \mathrm{~V} \\ \mathrm{~V}+=+4.75 \mathrm{~V}, \mathrm{~V}-=-4.75 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=-1 \mathrm{~mA} \\ \mathrm{~V}+=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=20 \mathrm{~mA} \end{gathered}$ | 2.7 | 3.4 | 0.5 | V |
| $\begin{aligned} & \mathrm{V}+ \\ & \mathrm{V}- \end{aligned}$ | $\begin{aligned} & \hline \text { Supply voltage } \\ & \text { Positive } \\ & \text { Negative } \\ & \hline \end{aligned}$ |  | $\begin{array}{r} 4.75 \\ -4.75 \\ \hline \end{array}$ | $\begin{array}{r} 5.0 \\ -5.0 \\ \hline \end{array}$ | $\begin{array}{r} 5.25 \\ -5.25 \\ \hline \end{array}$ | V |
| $\begin{aligned} & \text { ICC+ } \\ & \text { ICc- } \end{aligned}$ | Supply current Positive Negative | $\mathrm{V}+=5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}, \mathrm{~T}^{\prime}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 27 \\ -15 \end{gathered}$ | $\begin{array}{r} 50 \\ -28 \end{array}$ | mA |
| ${ }^{\text {I SC }}$ | Short circuit output current |  | -40 |  | -100 | $\mu \mathrm{A}$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$

| PARAMETER | FROM INPUT | $\begin{gathered} \text { TO } \\ \text { OUTPUT } \end{gathered}$ | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Input resistance Input capacitance |  |  |  | 4 3 |  | ${ }_{\mathrm{pF}}^{\mathrm{k} \Omega}$ |
| Large Signal Switching Speed |  |  |  |  |  |  |
| Propagation delay |  |  |  |  |  | ns |
| ${ }^{\text {t PLH(D) }}$ (D) Low to high ${ }^{1}$ | Amp | Output |  | 8 | 12 |  |
| ${ }^{\text {t PHL }}$ (D) $\quad$ High to low ${ }^{1}$ | Amp | Output |  | 6 | 9 |  |
| ${ }^{\text {t PLH(S) }}$ ( ${ }^{\text {P }}$ Low to high ${ }^{2}$ | Strobe | Output |  | 4.5 | 6 |  |
| ${ }^{\mathrm{t}}$ PHL(S) $\quad$ High to low ${ }^{2}$ Maximum operating frequency | Strobe | Output | 40 | 3.0 55 | 4.5 | MHz |
| Small Signal Switching Speed |  |  |  |  |  |  |
| Propagation delay |  |  |  |  |  | ns |
| PLH(D) Low to high ${ }^{3}$ | Amp | Output |  | 12 | 18 |  |
| PHL(D) High to low ${ }^{3}$ | Amp | Output |  | 10 | 15 |  |

## NOTES

1. Response time measured from 0 V point of $\pm 100 \mathrm{mV} \mathrm{p-p} 10 \mathrm{MHz}$ square wave to the 1.5 V point of the output
2. Response time measured from 1.5 V point of input to 1.5 V point of the output
3. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the 1.5 V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS


FEATURES

- 15ns maximum guaranteed propagation delay
- $20 \mu \mathrm{~A}$ maximum input bias current
- TTL compatible strobes and outputs
- Open collector output for wire-OR'd applications
- Large common mode input voltage range
- Operates from standard supply voltages


## APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver


## PIN CONFIGURATION

| F,N PACKAGE |  |
| :---: | :---: |
| inputia 1 | $14 \mathrm{v}+$ |
| input ib 2 | 13 v |
| nc 3 | 12 Input $2 A$ |
| output ir 4 | 11 input 2 B |
| strobe 1 l -5 | 10 nc |
| strobes 6 | 9 outputiv |
| ground 7 | 8 strobe 26 |

## BLOCK DIAGRAM



## EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $\mathrm{V}+=+5 \mathrm{~V}, \mathrm{~V}-=-5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise specified

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $V_{\text {OS }}$ | Input offset voltage <br> At $25^{\circ} \mathrm{C}$ <br> Over temperature range |  | $\mathrm{V}+=+4.75 \mathrm{~V}, \mathrm{~V}-=-4.75 \mathrm{~V}$ |  | 6 | $\begin{aligned} & 7.5 \\ & 10 \end{aligned}$ | mV |
| IBIAS | Input bias current <br> At $25^{\circ} \mathrm{C}$ <br> Over temperature range | $\mathrm{V}+=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}$ |  | 7.5 | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ | $\mu \mathrm{A}$ |
| ${ }^{\text {I OS }}$ | Input offset current <br> At $25^{\circ} \mathrm{C}$ <br> Over temperature range | $\mathrm{V}+=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}$ |  | 1.0 | $\begin{gathered} 5 \\ 12 \end{gathered}$ | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{CM}}$ | Common mode voltage range | $\mathrm{V}+=+4.75 \mathrm{~V}, \mathrm{~V}-=-4.75 \mathrm{~V}$ | $\pm 3$ |  |  | V |
| $1 / \mathrm{H}$ | Input current High | $\begin{gathered} \mathrm{V}+=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V} \\ \mathrm{~V}_{1 H}=2.7 \mathrm{~V} \end{gathered}$ <br> 1G or 2G strobe Common strobe S |  |  | $\begin{gathered} 50 \\ 100 \end{gathered}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| IIL | Low | $V_{I L}=0.5 \mathrm{~V}$ <br> 1G 2G strobe Common strobe S |  |  | $\begin{aligned} & -2.0 \\ & -4.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Output voltage Low | $\mathrm{V}_{+}=+5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}, \mathrm{~V}_{1}(\mathrm{~S})=2.0 \mathrm{~V}$ |  |  | 0.5 | V |
| ${ }^{1} \mathrm{OH}$ | Output current High | $\begin{aligned} \mathrm{I}_{\mathrm{LOAD}} & =20 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}+=+4.75 \\ \mathrm{~V}_{\mathrm{CC}}- & =-4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}} \end{aligned}=5.25 \mathrm{~V},$ |  |  | 250 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { V+ } \\ & \text { V- } \end{aligned}$ | Supply voltage Positive Negative |  | $\begin{gathered} 4.75 \\ -4.75 \\ \hline \end{gathered}$ | $\begin{gathered} 5.0 \\ -5.0 \end{gathered}$ | $\begin{gathered} 5.25 \\ -5.25 \\ \hline \end{gathered}$ | V |
| $\begin{aligned} & \text { ICC+ } \\ & \text { ICC- } \end{aligned}$ | Supply current Positive Negative | $\mathrm{V}+=5.25 \mathrm{~V}, \mathrm{~V}-=-5.25 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 27 \\ -15 \end{gathered}$ | $\begin{gathered} 50 \\ -28 \end{gathered}$ | mA |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, R_{L}=280 \Omega, C_{L}=15 \mathrm{pF}$

| PARAMETER | FROM INPUT | TO OUTPUT | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Input resistance Input capacitance |  |  |  | 4 3 |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \end{aligned}$ |
|  |  |  |  |  |  |  |
| ${ }^{\text {t PLH }}$ (D) Low to high ${ }^{1}$ | Amp | Output |  | 10 | 15 |  |
|  | Amp | Output |  | 8 | 12 |  |
| ${ }^{\text {PPLH(S) }}$ (S) Low to high ${ }^{2}$ | Strobe | Output |  | 6 | 10 |  |
| $\begin{array}{ll}\mathrm{t} \text { PHL(S) } & \text { High to low }{ }^{2} \\ & \text { Maximum operating frequency }\end{array}$ | Strobe | Output | 25 | 5 35 | 8 | MHz |
| Small Signal Switching Speed |  |  |  |  |  |  |
| Propagation delay |  |  |  |  |  | ns |
| $\mathrm{t}_{\text {PLH(D) }}$ L Low to high ${ }^{3}$ | Amp | Output |  | 17 | 25 |  |
| tPHL(D) High to low ${ }^{3}$ | Amp | Output |  | 11 | 17 |  |

NOTES

1. Response time measured from 0 V point of $\pm 100 \mathrm{mV} \mathrm{p-p} 10 \mathrm{MHz}$ square wave to the 1.5 V point of the output
2. Response time measured from 1.5 V point of input to 1.5 V point of the output
3. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the 1.5 V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T2L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common mode and differential voltage range
- Mil std 883A,B,C available


## APPLICATIONS

- A/D conversion
- ECL to TTL interface
- TTL to ECL interface
- Memory sensing
- Optical data coupling


## BLOCK DIAGRAM



## PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Positive supply voltage (V1+) | +15 | V |
| Negative supply voltage (V1-) | -15 | V |
| Gate supply voltage (V2 + ) | +7 | V |
| Output voltage | +15 | V |
| Differential input voltage | $\pm 5$ | V |
| Input common mode voltage | $\pm 6$ | V |
| Power dissipation | 600 | mW |
| Operating temperature range |  |  |
| NE527 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| SE527 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering, 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $\quad \mathrm{V}_{1^{+}}=10 \mathrm{~V}, \mathrm{~V}_{1^{-}}=-10 \mathrm{~V}, \mathrm{~V}_{2^{+}}=+5.0 \mathrm{~V}, \mathrm{~V}_{1 \mathrm{~N}}=0 \mathrm{~V}^{*}$

| PARAMETER | TEST CONDITIONS | SE527 |  |  | NE527 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| INPUT CHARACTERISTICS Input offset voltage @ $25^{\circ} \mathrm{C}$ Over temperature range |  |  |  | $\begin{aligned} & 4 \\ & 6 \end{aligned}$ |  |  | $\begin{gathered} 6 \\ 10 \end{gathered}$ | $\begin{aligned} & m V \\ & m V \end{aligned}$ |
| Input bias current @ $25^{\circ} \mathrm{C}$ Over temperature range | $\begin{gathered} \mathrm{V}_{1^{+}}=10 \mathrm{~V}, \mathrm{~V}_{1^{-}}=-10 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V} \end{gathered}$ |  |  | $\begin{aligned} & 2 \\ & 4 \end{aligned}$ |  |  | $\begin{aligned} & 2 \\ & 4 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| Input offset current @ $25^{\circ} \mathrm{C}$ Over temperature range | $\begin{gathered} \mathrm{V}_{1^{+}}=10 \mathrm{~V}, \mathrm{~V}_{1^{-}}=-10 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 0.5 \\ 1 \end{gathered}$ |  |  | 0.75 1 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| Input impedance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{f}=1 \mathrm{kHz}$ |  | 500 |  |  | 500 |  | k $\Omega$ |
| GATE CHARACTERISTICS <br> Output voltage <br> "1" State <br> "0" State | $\begin{gathered} \mathrm{V}_{2^{+}}=4.75 \mathrm{~V}, \text { ISOURCE }=-1 \mathrm{~mA} \\ \mathrm{~V}^{2}=4.75 \mathrm{~V}, \mathrm{I}_{\text {SINK }}=10 \mathrm{~mA} \\ \hline \end{gathered}$ | 2.5 | 3.3 | 0.5 | 2.7 | 3.3 | 0.5 | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \\ & \hline \end{aligned}$ |
| Strobe inputs <br> " 0 " Input current <br> "1" Input current @ $25^{\circ} \mathrm{C}$ <br> Over temperature range <br> " 0 " Input voltage <br> "1" Input voltage | $\begin{gathered} \mathrm{V}_{2^{+}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {STROBE }}=0.5 \mathrm{~V} \\ \mathrm{~V}_{2^{+}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {STROBE }}=2.7 \mathrm{~V} \\ \mathrm{~V}_{2^{+}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {STROBE }}=2.7 \mathrm{~V} \\ \mathrm{~V}^{+}=4.75 \mathrm{~V} \\ \mathrm{~V}_{2^{+}}=4.75 \mathrm{~V} \end{gathered}$ | 2.0 | . | $\begin{gathered} -2 \\ 50 \\ 200 \\ 0.8 \end{gathered}$ | 2.0 |  | $\begin{gathered} -2 \\ 100 \\ 200 \\ 0.8 \end{gathered}$ | $\begin{gathered} \mathrm{mA} \\ \mu \mathrm{~A} \\ \mu \mathrm{~A} \\ \mathrm{~V} \\ \mathrm{~V} \end{gathered}$ |
| Short circuit Output current | $\mathrm{V}_{2^{+}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | -18 |  | -70 | -18 |  | -70 | mA |
| ```POWER SUPPLY REQUIREMENTS Supply voltage V V1- V}\mp@subsup{2}{}{+``` |  | $\begin{gathered} 5 \\ -6 \\ 4.5 \end{gathered}$ | 5 | $\begin{gathered} 10 \\ -10 \\ 5.5 \end{gathered}$ | $\begin{gathered} 5 \\ -6 \\ 4.75 \end{gathered}$ | 5 | 10 -10 5.25 | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| Supply current $\begin{aligned} & 1_{1}{ }^{+} \\ & 1_{1} \\ & I_{2^{+}} \end{aligned}$ | $\begin{gathered} \mathrm{V}_{1^{+}}=10 \mathrm{~V}, \mathrm{~V}_{1^{-}}=-10 \mathrm{~V} \\ \mathrm{~V}_{2^{+}}=5.25 \mathrm{~V} \\ \text { Over temp. } \\ \text { Over temp. } \\ \text { Over temp. } \end{gathered}$ |  |  | 5 10 20 |  |  | 5 10 20 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

*NOTE
Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Transient response propagation delay time $\begin{aligned} & \text { tPLH } \\ & \text { tPHL } \end{aligned}$ | $\begin{gathered} V_{I N}= \pm 100 \mathrm{mV} \text { step } \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & 16 \\ & 14 \end{aligned}$ | $\begin{aligned} & 26 \\ & 24 \end{aligned}$ | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |
| Delay between output A and B |  |  | 2 | 5 | ns |
| Strobe delay time $t_{\text {on }}$ Turn-on time $t_{\text {off }}$ Turn-off time |  |  | 6 6 |  | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |

TYPICAL PERFORMANCE CHARACTERISTICS


## APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1-) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages ( $\mathrm{V} 1+$ and V 1 -) up to a maximum of $\pm 6$ volts as supply voltages are increased.

It is also important to note that Output $A$ is in phase with Input $A$ and Output $B$ is in phase with Input B.

## TYPICAL APPLICATIONS



## DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed $T^{2}$ L gates with a precision linear amplifier on a single monolithic chip.

## FEATURES

- 10ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common mode and differential voltage range


## APPLICATIONS

- A/D conversion
- ECL to TTL interface
- TTL to ECL interface
- Memory sensing
- Optical data coupling
- Mil std 883A,B,C available


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Positive supply voltage (V1+) | +15 | V |
| Negative supply voltage (V1-) | -15 | V |
| Gate supply voltage (V2+) | +7 | V |
| Output voltage | $\pm 5$ | V |
| Differential input voltage | $\pm 6$ | V |
| Input common mode voltage | 600 | mW |
| Power dissipation | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| NE529 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| SE529 |  |  |
| Storage temperature range | +300 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  |  |
| (soldering, 60 sec) |  |  |

PIN CONFIGURATION


## BLOCK DIAGRAM



## EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $\mathrm{V}_{1}+=+10 \mathrm{~V}, \mathrm{~V}_{2}+=+5.0 \mathrm{~V}, \mathrm{~V}_{1-}=-10 \mathrm{~V}, \mathrm{~V}_{1 \mathrm{~N}}=0 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE529 |  |  | NE529 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| INPUT CHARACTERISTICS <br> Input offset voltage @ $25^{\circ} \mathrm{C}$ Over temperature range |  |  |  | 4 6 |  |  | $\begin{gathered} 6 \\ 10 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Input bias current @ $25^{\circ} \mathrm{C}$ Over temperature range | $\begin{gathered} V_{1}+=10 \mathrm{~V}, V_{1-}=-10 \mathrm{~V} \\ V_{I N}=0 \mathrm{~V} \end{gathered}$ |  | 5 | $\begin{aligned} & 12 \\ & 36 \end{aligned}$ |  | 5 | $\begin{aligned} & 20 \\ & 50 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input offset current @ $25^{\circ} \mathrm{C}$ Over temperature range | $\begin{aligned} \mathrm{V}_{1}+= & 10 \mathrm{~V}, \mathrm{~V}_{1-}=-10 \mathrm{~V} \\ & \mathrm{~V}_{\mathbb{I N}}=0 \mathrm{~V} \end{aligned}$ |  | 2 | $\begin{aligned} & 3 \\ & 9 \end{aligned}$ |  | 2 | $\begin{gathered} 5 \\ 15 \\ \hline \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input impedance | $T_{A}=25^{\circ} \mathrm{C}, \mathrm{f}=1 \mathrm{kHz}$ |  | 10 |  |  | 10 |  | $k \Omega$ |
| GATE CHARACTERISTICS <br> Output voltage <br> "1" state <br> " 0 " state | $\begin{gathered} \mathrm{V}_{2}+=4.75 \mathrm{~V}, I_{\text {source }}=-1 \mathrm{~mA} \\ \mathrm{~V}_{2}+=4.75 \mathrm{~V}, I_{\text {sink }}=10 \mathrm{~mA} \end{gathered}$ | 2.5 | 3.3 | 0.5 | 2.7 | 3.3 | 0.5 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Strobe inputs <br> "0" input current <br> "1" input current @ $25^{\circ} \mathrm{C}$ <br> Over temperature range <br> " 0 " input voltage <br> "1" input voltage | $\begin{gathered} \mathrm{V}_{2}+=5.25 \mathrm{~V}, \mathrm{~V}_{\text {strobe }}=0.5 \mathrm{~V} \\ \mathrm{~V}_{2}+=5.25 \mathrm{~V}, \mathrm{~V}_{\text {strobe }}=2.7 \mathrm{~V} \\ \mathrm{~V}_{2}+=5.25 \mathrm{~V}, \mathrm{~V}_{\text {strobe }}=2.7 \mathrm{~V} \\ \mathrm{~V}_{2}+=4.75 \mathrm{~V} \\ \mathrm{~V}_{2}+=4.75 \mathrm{~V} \end{gathered}$ | 2.0 |  | $\begin{gathered} -2 \\ 50 \\ 200 \\ 0.8 \end{gathered}$ | 2.0 |  | $\begin{gathered} -2 \\ 100 \\ 200 \\ 0.8 \end{gathered}$ | $\begin{gathered} \mathrm{mA} \\ \mu \mathrm{~A} \\ \mu \mathrm{~A} \\ \mathrm{~V} \\ \mathrm{~V} \end{gathered}$ |
| Short circuit Output current | $\mathrm{V}_{2}+=5.25 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | -18 |  | -70 | -18 |  | -70 | mA |
| POWER SUPPLY REQUIREMENTS <br> Supply voltage $\begin{aligned} & V_{1+} \\ & V_{1-} \\ & V_{2}+ \end{aligned}$ |  | $\begin{array}{r} 5 \\ -6 \\ 4.5 \end{array}$ | 5 | $\begin{gathered} 10 \\ -10 \\ 5.5 \\ \hline \end{gathered}$ | $\begin{gathered} 5 \\ -6 \\ 4.75 \end{gathered}$ | 5 | $\begin{gathered} 10 \\ -10 \\ 5.25 \end{gathered}$ | $\begin{aligned} & V \\ & V \\ & V \end{aligned}$ |
| Supply current $\begin{aligned} & \mathrm{I}_{1}+ \\ & \mathrm{I}_{1}- \\ & \mathrm{I}_{2}+ \end{aligned}$ | $\begin{gathered} \mathrm{V}_{1}+=10 \mathrm{~V}, \mathrm{~V}_{1-}=-10 \mathrm{~V} \\ \mathrm{~V}_{2}+=5.25 \mathrm{~V} \\ \text { Over temp. } \\ \text { Over temp. } \\ \text { Over temp. } \end{gathered}$ |  |  | 5 10 20 |  |  | 5 10 20 | mA <br> mA <br> mA |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$

| PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Transient response | $V_{I N}= \pm 100 \mathrm{mV}$ step |  |  |  |  |
| Propagation delay time |  |  |  |  |  |
| tPLH |  |  | 12 | 22 | ns |
| tPHL |  |  | 10 | 20 | ns |
| Delay between output |  |  |  | 5 | ns |
| A and B |  |  |  |  |  |
| Strobe delay time |  |  | 6 |  | ns |
| ton turn-on time |  |  |  |  | ns |
| toff turn-off time |  |  |  |  |  |

Parameters are guaranteed over the temperature range unless otherwise specified

TYPICAL PERFORMANCE CHARACTERISTICS


## APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1-) should always be at least five volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1-) up to a maximum of $\pm 6$ volts as supply voltages are increased.

It is also important to note that Output $A$ is in phase with Input $A$ and Output $B$ is in phase with Input B.

## TYPICAL APPLICATIONS



## ECL TO TTL INTERFACE



TTL TO ECL INTERFACE


## DESCRIPTION

The $\mu \mathrm{A} 710$ is a High Speed Differential Voltage Comparator featuring low offset voltage, high sensitivity and a wide input voltage range. It is ideally suited for use as a pulse height discriminator, an analog comparator or a digital line receiver. The output structure of the $\mu A 710$ is compatible with DTL, TTL and Utilogic integrated circuits.

The $\mu \mathrm{A} 710$ is specified for operation over the MIL temperature range of $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. The $\mu \mathrm{A} 710 \mathrm{C}$ is specified for operation over the commercial/industrial temperature range of $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$.

## BLOCK DIAGRAM



## FEATURES

- Fast response-40ns
- High sensitivity-1.7V/mV
- Low offset voltage temperature coefficient- $3.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- High input voltage range- $\pm 5.0 \mathrm{~V}$
- Mil std 883A,B,C available


## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Positive supply voltage | +14.0 | V |
| Negative supply voltage | -7.0 | V |
| Peak output current | 10 | mA |
| Differential input voltage | $\pm 5.0$ | V |
| Input voltage | $\pm 7.0$ | mW |
| Internal power dissipation4 | 300 | mW |
| TO-99 | 200 | ${ }^{\circ} \mathrm{C}$ |
| TO-91 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | 0 to +75 | ${ }^{\circ} \mathrm{C}$ |
| $\mu A 710$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| رA710C | 300 |  |
| Storage temperature rage |  |  |
| Lead temperature |  |  |
| (soldering, 60sec) |  |  |

PIN CONFIGURATIONS


DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=12 \mathrm{~V}, \mathrm{~V}-=6.0 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | $\mu$ A710 |  |  | $\mu$ A710C |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input offset voltage ${ }^{3}$ | $R_{S} \leq 200 \Omega$ |  | 0.6 | 2.0 |  | 1.6 | 5.0 | mV |
| Input offset current ${ }^{3}$ Input bias current | - |  | $\begin{gathered} 0.75 \\ 13 \end{gathered}$ | $\begin{aligned} & 3.0 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & 1.8 \\ & 16 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 25 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Voltage gain |  | 1250 | 1700 |  | 1000 | 1500 |  |  |
| Output resistance Output sink current | $\Delta \mathrm{V}_{\text {IN }} \geq 5 \mathrm{mV}$, $\mathrm{V}_{\text {OUT }}=0$ | 2.0 | $\begin{array}{r} 200 \\ 2.5 \\ \hline \end{array}$ |  | 1.6 | 200 |  | $\begin{gathered} \Omega \\ \mathrm{mA} \end{gathered}$ |
| $\begin{aligned} & \text { Response time }{ }^{2} \\ & \mu \text { A710 } \\ & \mu \text { A710C } \end{aligned}$ | The following specifications apply for: $\begin{gathered} -55^{\circ} \mathrm{C} \leq \mathrm{T}_{A} \leq+125^{\circ} \mathrm{C} \\ 0^{\circ} \leq \mathrm{T}_{\mathrm{A}} \leq+75^{\circ} \mathrm{C} \end{gathered}$ |  | 40 |  |  | 40 |  | ns |
| Input offset voltage ${ }^{3}$ | RS $\leq 200 \Omega$ |  |  | 3.0 |  |  | 6.5 |  |
| Average temperature coefficient of input offset voltage | $\begin{aligned} & R_{S}=50 \Omega, T_{A}=+25^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ & R_{S}=50 \Omega, T_{A}=+25^{\circ} \mathrm{C} \text { to }-55^{\circ} \mathrm{C} \\ & \mathrm{RS}_{\mathrm{S}}=50 \Omega, \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & 3.5 \\ & 2.7 \end{aligned}$ | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ |  | 5 | 20 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input offset current3 | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{gathered} 0.25 \\ 1.8 \end{gathered}$ | $\begin{aligned} & 3.0 \\ & 7.0 \end{aligned}$ |  |  | 7.5 | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| Average temperature coefficient | $T_{A}=+25^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  | 5.0 | 25 |  |  |  | $n \mathrm{~A} /{ }^{\circ} \mathrm{C}$ |
| Input offset current | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \text { to }-55^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C} \\ T_{A}=+25^{\circ} \mathrm{C} \text { to } 0^{\circ} \mathrm{C} \end{gathered}$ |  | 15 | 75 |  | $\begin{aligned} & 15 \\ & 24 \\ & \hline \end{aligned}$ | $\begin{gathered} 50 \\ 100 \end{gathered}$ |  |
| Input bias current | $\begin{gathered} T_{A}=-55^{\circ} \mathrm{C} \\ T_{A}=0^{\circ} \mathrm{C} \end{gathered}$ |  | 27 | 45 |  | 25 | 40 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input common mode voltage range | $\mathrm{V}-=-7.0 \mathrm{~V}$ | $\pm 5.0$ |  |  | $\pm 5.0$ |  |  | V |
| Common mode rejection ratio Differential input voltage range Voltage gain | $\mathrm{RS}^{5} \leq 200 \Omega$ | $\begin{gathered} 80 \\ \pm 5.0 \\ 1000 \end{gathered}$ | 100 |  | $\begin{gathered} 70 \\ \pm 5.0 \\ 800 \end{gathered}$ | 98 |  | dB |
| Positive output level Negative output level | $\begin{aligned} & \Delta \mathrm{V}_{\mathbb{N}} \geq 5 \mathrm{mV}, 0 \leq 1 \text { OUT } \leq 5.0 \mathrm{~mA} \\ & \Delta \mathrm{~V}_{\mathbb{I N}} \geq 5 \mathrm{mV} \end{aligned}$ | $\begin{gathered} 2.5 \\ -1.0 \end{gathered}$ | $\begin{gathered} 3.2 \\ -0.5 \end{gathered}$ | $\begin{gathered} 4.0 \\ 0 \end{gathered}$ | $\begin{array}{r} 2.5 \\ -1.0 \end{array}$ | $\begin{gathered} 3.2 \\ -0.5 \end{gathered}$ | $\begin{gathered} 4.0 \\ 0 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Output sink current | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}, \Delta \mathrm{~V}_{\text {IN }} \geq 5 \mathrm{~mA}, \mathrm{~V}_{\text {OUT }}=0 \\ \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}, \Delta \mathrm{~V}_{\text {IN }} \geq 5 \mathrm{mV}, \mathrm{~V}_{\text {OUT }}=0 \\ \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C}, \Delta \mathrm{~V}_{\text {IN }} \geq 5 \mathrm{mV}, \mathrm{~V}_{\text {OUT }}=0 \end{gathered}$ | $\begin{aligned} & 0.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 1.7 \\ & 2.3 \end{aligned}$ |  | 0.5 |  |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Positive supply current Negative supply current | Vout $\leq 0$ |  | $\begin{aligned} & 5.2 \\ & 4.6 \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 7.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 5.2 \\ & 4.6 \\ & \hline \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 7.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Power consumption |  |  | 90 | 150 |  | 90 | 150 | mW |

NOTES

1. All voltages are referenced to ground.
2. The response time specified is measured with a 100 mV input step, and a 5 mV overdrive.
3. Input Offset Voltage and Input Offset Current are specified for output voltage levels of:

| $\mu \mathrm{A} 710$ | $\mu \mathrm{~A} 710 \mathrm{C}$ |
| :---: | :---: |
| 1.8 V at $-55^{\circ} \mathrm{C}$ | 1.5 V at $0^{\circ} \mathrm{C}$ |
| 1.4 V at $+25^{\circ} \mathrm{C}$ | 1.4 V at $+25^{\circ} \mathrm{C}$ |
| $1 . \mathrm{OV}$ at $+125^{\circ} \mathrm{C}$ | 1.2 V at $+75^{\circ} \mathrm{C}$ |

1.0 V at $+125^{\circ} \mathrm{C} \quad 1.2 \mathrm{~V}$ at $+75^{\circ} \mathrm{C}$
. Rating applies for temperatures up to:
$\mu \mathrm{A} 710-+125^{\circ} \mathrm{C}$
$\mu \mathrm{A} 710 \mathrm{C}-+75^{\circ} \mathrm{C}$

## DESCRIPTION

The $\mu \mathrm{A} 711$ High Speed Dual Voltage Comparator features low offset voltage, high sensitivity and a wide input voltage range. It is ideal for use as a bi-directional limit detector in automatic test equipment.
Due to fast response and strobe control capabilities the $\mu \mathrm{A} 711$ performs well as a sense amplifier in core memory systems.
The $\mu \mathrm{A} 711$ is specified over the military temperature range of $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. The $\mu \mathrm{A} 711 \mathrm{C}$ is specified over the commercial/ industrial temperature range of $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$.

## FEATURES

- Fast response-40ns
- High sensitivity- $1.5 \mathrm{~V} / \mathrm{mV}$
- Low offset voltage temperature coefficient- $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- High input voltage range $- \pm 5.0 \mathrm{~V}$
- Mil std 883A,B,C available


## LOGIC DIAGRAM



PIN CONFIGURATION


## CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Positive supply voltage | +14.0 | V |
| Negative supply voltage | -7.0 | V |
| Peak output current | 50 | mA |
| Differential input voltage | $\pm 5.0$ | V |
| Internal power dissipation4 | 300 | mW |
| Operating temperature range |  |  |
| $\mu \mathrm{A} 711$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mu \mathrm{A} 711 \mathrm{C}$ | 0 to +75 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering, 60sec) | 300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=12.0 \mathrm{~V}, \mathrm{~V}-=-6.0 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | $\mu$ A711 |  |  | $\mu \mathrm{A} 11 \mathrm{C}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input offset voltage | $\begin{gathered} \mathrm{VOUT}=+1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}} \leq 200 \Omega, \mathrm{VCM}=0 \\ \text { VOUT }=+1.4 \mathrm{~V}, \mathrm{RS}_{\mathrm{S}} \leq 200 \Omega \end{gathered}$ |  | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 5.0 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 7.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Input offset current Input bias current | $\mathrm{V}_{\text {OUT }}=+1.4 \mathrm{~V}$ |  | $\begin{aligned} & 0.5 \\ & 25 \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 10.0 \\ 75 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 0.5 \\ & 25 \\ & \hline \end{aligned}$ | $\begin{aligned} & 15.0 \\ & 100 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Voltage gain |  | 750 | 1500 |  | 700 | 1500 |  |  |
| Response time ${ }^{2}$ Strobe release time |  |  | $\begin{aligned} & 40 \\ & 12 \end{aligned}$ |  |  | $\begin{aligned} & 40 \\ & 12 \end{aligned}$ |  | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |
| Input common mode voltage range Differential input voltage range | $\mathrm{V}-=-7.0 \mathrm{~V}$ | $\begin{aligned} & \pm 5.0 \\ & \pm 5.0 \end{aligned}$ |  |  | $\begin{aligned} & \pm 5.0 \\ & \pm 5.0 \end{aligned}$ |  |  | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Output resistance |  |  | 200 |  |  | 200 |  | $\Omega$ |
| Positive output level Loaded positive output level | $\begin{gathered} V_{I N} \geq 10 \mathrm{mV} \\ V_{I N} \geq 10 \mathrm{mV}, \mathrm{I}_{\mathrm{O}}=5 \mathrm{~mA} \end{gathered}$ | 2.5 | $\begin{aligned} & 4.5 \\ & 3.5 \end{aligned}$ | 5.0 | 2.5 | $\begin{aligned} & 4.5 \\ & 3.5 \end{aligned}$ | 5.0 | V |
| Negative output level Strobed output level | $\begin{gathered} \mathrm{V}_{\text {IN }} \geq 10 \mathrm{mV} \\ \mathrm{~V}_{\text {STROBE }}<0.3 \mathrm{~V} \end{gathered}$ | $\begin{array}{r} \hline-1.0 \\ -1.0 \\ \hline \end{array}$ | -0.5 | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{array}{r} \hline-1.0 \\ -1.0 \\ \hline \end{array}$ | -0.5 | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | V |
| Output sink current | $\mathrm{V}_{\text {IN }} \geq 10 \mathrm{mV}$, $\mathrm{V}_{\text {OUT }} \geq 0$ | 0.5 | 0.8 |  | 0.5 | 0.8 |  | mA |
| Strobe current <br> Positive supply current Negative supply current | $\begin{gathered} V_{\text {STROBE }}=100 \mathrm{mV} \\ \text { VOUT } \leq 0 \end{gathered}$ |  | $\begin{aligned} & 1.2 \\ & 8.6 \\ & 3.9 \end{aligned}$ | 2.5 |  | $\begin{aligned} & \hline 1.2 \\ & 8.6 \\ & 3.9 \end{aligned}$ | 2.5 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Power consumption |  |  | 130 | 200 |  | 130 | 230 | mW |
| The following specifications apply over the temperature range of: $-55^{\circ} \mathrm{C} \leq T_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ for the $\mu \mathrm{A} 711$ <br> $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+75^{\circ} \mathrm{C}$ for the $\mu \mathrm{A} 711 \mathrm{C}$  |  |  |  |  |  |  |  |  |
| Input offset voltage ${ }^{3}$ | $\begin{aligned} & \mathrm{R}_{\mathrm{S}} \leq 200 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \\ & \mathrm{R}_{\mathrm{S}} \leq 200 \Omega \end{aligned}$ |  |  | $\begin{aligned} & 4.5 \\ & 6.0 \\ & \hline \end{aligned}$ |  |  | $\begin{gathered} \hline 6.0 \\ 10.0 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Input offset current ${ }^{3}$ Input bias current |  |  |  | $\begin{gathered} 20 \\ 150 \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 25 \\ 150 \\ \hline \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Temperature coefficient of input |  |  | 5.0 |  |  | 5.0 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Offset voltage |  |  |  |  |  |  |  |  |
| Voltage gain |  | 500 |  |  | 500 |  |  |  |

## NOTES

1. All voltages are referenced to pin 1.
2. The response time specified is for a 100 mV input step, with a 5 mV overdrive.
3. The input offset voltage and input offset current are specified for a logic threshold voltage of:
$\mu \mathrm{A} 711$
1.8 V at $-55^{\circ} \mathrm{C}$
1.4 V at $+25^{\circ} \mathrm{C}$
1.4 V at $+25^{\circ} \mathrm{C}$
1.0 V at $+125^{\circ} \mathrm{C}$

0 V at $+125^{\circ} \mathrm{C}$
1.5 V at $0^{\circ} \mathrm{C}$
1.4V at $+25^{\circ} \mathrm{C}$
1.2 V at $+75^{\circ} \mathrm{C}$
4. Rating applies for temperatures up to: $\mu \mathrm{A} 711-+125^{\circ} \mathrm{C}$
$\mu \mathrm{A} 711 \mathrm{C}-+75^{\circ} \mathrm{C}$

## section 6 memory interfnce

## DESCRIPTION

The 55325 and 75325 are monolithic integrated circuit memory drivers with logic inputs and are designed for use with magnetic memories.
The devices contain two 600-milliampere source-switch pairs and two 600milliampere sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.
The 55325 is characterized for operation over the full military temperature range of $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$; the 75325 is characterized for operation from $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.
When Rint and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575 -ohm resistor. This method provides adequate base drive for source currents up to 375 mA with a $\mathrm{VCC2}$ voltage of 15 volts or 600 mA with a $\mathrm{V}_{\mathrm{CC} 2}$ voltage of 24 volts.
When source currents greater than 375 mA are required, it is recommended that a resistor of the appropriate value be connected between $\mathrm{V}_{\mathrm{CC}}$ and node R and $\mathrm{R}_{\text {int }}$ must remain open. By using this method the source base current may usually be regulated within $\pm 5 \%$. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to $\mathrm{V}_{\mathrm{Cc}}$. This arrangement provides protection from voltage surges associated with switching inductive loads.

## FEATURES

- 600mA output capability
- Fast switching times
- Output short-circuit protection
- Dual sink and dual source outputs
- Minimum time skew between address and output current rise
- 24 volt output capability
- Source base drive externally adjustable
- TTL or DTL compatibility
- Input clamping diodes


## BLOCK DIAGRAM



## PIN CONFIGURATION



## TRUTH TABLE

| ADDRESS INPUTS |  |  |  | STROBE INPUTS |  | OUTPUTS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { SOURCE } \\ & \text { A B } \end{aligned}$ |  | SINK |  | $\underset{\text { S1 }}{\substack{\text { SOURCE }}}$ | $\begin{gathered} \text { SINK } \\ \text { S2 } \end{gathered}$ | SOURCE |  | SINK |  |
|  |  | C | D |  |  | W | X | Y | z |
| L | H | X | x | L | H | ON | OFF | OFF | OFF |
| H | L | x | X | L | H | OFF | ON | OFF | OFF |
| x | X | L | H | H | L | OFF | OFF | ON | OFF |
| x | X | H | L | H | L | OFF | OFF | OFF | ON |
| X | X | X | X | H | H | OFF | OFF | OFF | OFF |
| H | H | H | H | X | X | OFF | OFF | OFF | OFF |

NOTE
Not more than one output is to be on at any one time.
$H=$ high level, $L=$ low level, $X=$ irrelevant

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING |  | UNIT |
| :---: | :---: | :---: | :---: |
|  | 55325 | 75325 |  |
| Supply voltage $\mathrm{V}_{\mathrm{CC} 1}{ }^{1}$ | 7 | 7 | V |
| Suppy voltage $\mathrm{V}_{\mathrm{cc} 2}{ }^{2}$ | 25 | 25 | v |
| Input voltage (any address or strobe input) | 5.5 | 5.5 | V |
| Continuous total dissipation at (or below) $100^{\circ} \mathrm{C}$ case temperature ${ }^{2}$ | 1 | 1 | W |
| Operating free-air temperature range | -55 to +125 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature $1 / 16$ inch from case for 60 seconds $F$ package | 300 | 300 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature $1 / 16$ inch from case for 10 seconds $\quad \mathrm{N}$ package | 260 | 260 | ${ }^{\circ} \mathrm{C}$ |

## NOTES

1. Voltage values are with respect to network ground terminal
2. For operation above $100^{\circ} \mathrm{C}$ case temperature, refer to Dissipation Derating Curve, Figure 8. For dissipation ratings in free-air, see Figure 9.

EQUIVALENT SCHEMATIC


DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  |  | TEST CONDITIONS |  | 55325 |  |  | 75325 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  |  |  | 2 |  |  | 2 |  |  | V |
| VIL | Low-level input voltage |  |  |  |  |  | 0.8 |  |  | 0.8 | V |
| $V_{1}$ | Input clamp voltage |  | $\begin{gathered} \mathrm{VCC}_{\mathrm{C}}=4.5 \mathrm{~V}, \mathrm{VCC}=24 \mathrm{~V} \\ \mathrm{I}_{1}=-10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  |  | -1.3 | -1.7 |  | -1.3 | -1.7 | V |
| $I^{(0 f f)}$ | Source-collectors terminal off-state current |  | $\begin{aligned} & V_{C C 1}=4.5 \mathrm{~V} \\ & V_{C C 2}=24 \mathrm{~V} \end{aligned}$ | Full range ${ }^{3}$ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 3 | $\begin{aligned} & 500 \\ & 150 \end{aligned}$ |  | 3 | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | $\mu \mathrm{A}$ |
| VOH | High-level sink output voltage |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC} 1}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=24 \mathrm{~V} \\ & \mathrm{lO}_{\mathrm{O}}=0 \end{aligned}$ |  | 19 | 23 |  | 19 | 23 |  | V |
| $V_{\text {(sat) }}$ | Saturation voltage2 | Source outputs <br> Sink outputs | $\begin{aligned} & V_{C C 1}=4.5 \mathrm{~V}, \\ & V_{C C 2}=15 \mathrm{~V}, \\ & R_{L}=24 \Omega, \\ & I_{(\text {source })} \approx-600 \mathrm{~mA}^{4} \\ & V_{C C 1}=4.5 \mathrm{~V}, \\ & V_{C C 2}=15 \mathrm{~V}, \\ & R_{L}=24 \Omega, \\ & I_{\text {(sink })} \approx 600 \mathrm{~mA}^{2} \\ & \hline \end{aligned}$ | Full range ${ }^{3}$ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Full range ${ }^{3}$ $\mathrm{T}_{\Delta}=25^{\circ} \mathrm{C}$ |  | $\begin{aligned} & 0.43 \\ & 0.43 \end{aligned}$ | $\begin{aligned} & 0.9 \\ & 0.7 \\ & 0.9 \\ & 0.7 \\ & \hline \end{aligned}$ |  | $0.43$ $0.43$ | $\begin{gathered} 0.9 \\ 0.75 \\ 0.9 \\ 0.75 \end{gathered}$ | V |
| 11 | Input current at max input voltage | Address inputs Strobe inputs | $\begin{aligned} & V_{C C 1}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=24 \mathrm{~V} \\ & \mathrm{~V}_{1}=5.5 \mathrm{~V} \end{aligned}$ |  |  |  | 1 <br> 2 |  |  | 1 2 | mA |
| IIH | High-level input current | Address inputs Strobe inputs | $\begin{aligned} & V_{C c 1}=5.5 \mathrm{~V}, V_{c c}=24 \mathrm{~V} \\ & V_{1}=2.4 \mathrm{~V} \end{aligned}$ |  |  | 3 6 | $\begin{aligned} & 40 \\ & 80 \end{aligned}$ |  | 3 6 | 40 80 | $\mu \mathrm{A}$ |
| IIL | Low-level input current | Address inputs Strobe inputs | $\begin{aligned} & \mathrm{V}_{\mathrm{CC} 1}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=24 \mathrm{~V}, \\ & \mathrm{~V}_{1}=0.4 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & -1 \\ & -2 \end{aligned}$ | $\begin{aligned} & -1.6 \\ & -3.2 \end{aligned}$ |  | $\begin{aligned} & -1 \\ & -2 \end{aligned}$ | $\begin{aligned} & -1.6 \\ & -3.2 \end{aligned}$ | mA |
| ICC(off) | Supply current, all sources \& sinks off | From Vcc1 From Vcc2 | $\begin{aligned} & \cdot V_{C C 1}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=24 \mathrm{~V}, \\ & T_{A}=25^{\circ} \mathrm{C} \end{aligned}$ |  |  | $\begin{aligned} & 14 \\ & 7.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 22 \\ & 20 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 14 \\ & 7.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 22 \\ & 20 \\ & \hline \end{aligned}$ | mA |
| Icc1 | Supply current from $\mathrm{V}_{\mathrm{CC}} 1$, either sink on |  | $\begin{aligned} & V_{C C 1}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=24 \mathrm{~V}, \\ & \mathrm{I}_{(\text {sink })}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ |  |  | 55 | 70 |  | 55 | 70 | mA |
| Icc2 | Supply current from VCC2, either source on |  | $\begin{array}{r} \mathrm{VCC}_{\mathrm{CC} 1}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC} 2}=24 \mathrm{~V}, \\ \mathrm{I}_{\text {(source) }}=-50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} 4 \end{array}$ |  |  | 32 | 50 |  | 32 | 50 | mA |

NOTES

1. Over rated operating free-air temperature range, unless otherwise specified.
2. Not more than one output is to be on at any one time.
3. Full range for 55325 is $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ and for 75325 is $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$.
4. These parameters must be measured using pulse techniques, $\mathrm{t}_{\mathrm{w}}=200 \mu \mathrm{~s}$, duty cycle $\leq$
$2 \%$.
AC ELECTRICAL CHARACTERISTICS $V_{C C 1}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER* | TO (OUTPUT) | TEST FIGURE | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |
| tpLH tPHL | Source collectors | 1 | $\begin{gathered} V_{C C 2}=15 \mathrm{~V}, R_{L}=24 \Omega \\ C_{L}=25 p F \end{gathered}$ |  | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ | $\begin{aligned} & 50 \\ & 50 \end{aligned}$ | ns |
| $\begin{aligned} & \text { tTLH } \\ & \text { tTHL } \end{aligned}$ | Source outputs | 2 | $\begin{gathered} \mathrm{V}_{\mathrm{CC} 2}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega \\ \mathrm{C}_{\mathrm{L}}=25 \mathrm{pF} \end{gathered}$ |  | $\begin{gathered} 55 \\ 7 \end{gathered}$ |  | ns |
| tplh <br> tpHL | Sink outputs | 1 | $\begin{gathered} \mathrm{VCC2}=15 \mathrm{~V}, R_{\mathrm{L}}=24 \Omega \\ C_{L}=25 \mathrm{pF} \end{gathered}$ |  | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & 45 \\ & 45 \end{aligned}$ | ns |
| $\begin{aligned} & \text { tTLH } \\ & \text { tTHL } \end{aligned}$ | Sink outputs | 2 | $\begin{gathered} \mathrm{V}_{\mathrm{CC} 2}=15 \mathrm{~V}, R_{\mathrm{L}}=24 \Omega \\ C_{L}=25 \mathrm{pF} \end{gathered}$ |  | $\begin{aligned} & \hline 7 \\ & 9 \\ & \hline \end{aligned}$ | $\begin{aligned} & 15 \\ & 20 \\ & \hline \end{aligned}$ | ns |
| $t_{s}$ | Sink outputs | 1 | $\begin{gathered} \mathrm{VCC} 2=15 \mathrm{~V}, R_{\mathrm{L}}=24 \Omega, \\ C_{L}=25 \mathrm{pF} \end{gathered}$ |  | 15 | 30 | ns |

## NOTE

*tpLH $=$ propagation delay time, low-to-high-level output
tPHL $=$ propagation delay time, high-to-low-level output
tTLH $=$ transition time, low-to-high-level output
$t_{\text {THL }}=$ transition time, high-to-low-level output
$\mathrm{t}_{\mathrm{s}}=$ storage time

TYPICAL PERFORMANCE CHARACTERISTICS
TEST CIRCUIT


TEST TABLE

| PARAMETER | OUTPUT UNDER TEST | INPUT | CONNECT TO 5V |
| :---: | :---: | :---: | :---: |
| tPLH and $t_{P H L}$ | Source collectors | $A$ and $S 1$ | $B, C, D$ and $S 2$ |
|  | $B$ and $S 1$ | $A, C, D$ and $S 2$ |  |
| $t_{P L H}, t_{P H L}$ <br> $t_{T L H}$, <br> and $t_{S}$ | Sink output $Y$ | $C$ and $S 2$ | $A, B, D$ and $S 1$ |
| and | Sink output $Z$ | $D$ and $S 2$ | $A, B, C$ and $S 1$ |

VOLTAGE WAVEFORMS


FIGURE 1 SWITCHING TIMES

## TYPICAL PERFORMANCE CHARACTERISTICS



## NOTES

All resistors values are typical and in ohms.

1. The pulse generator has the following characteristics.

Zout $=50 \Omega$, duty cycle $\leq 1 \%$.
2. $C_{L}$ includes probe and jig capacitance.

TEST TABLE

| PARAMETER | OUTPUT UNDER TEST | INPUT | CONNECT TO 5V |
| :---: | :---: | :---: | :---: |
| tTLH and tTHL | Source output $W$ | $A$ and $S 1$ | $B, C, D$ and $S 2$ |
|  | Source output $X$ | $B$ and $S 1$ | $A, B, D$ and $S 2$ |

VOLTAGE WAVEFORMS


FIGURE 2 TRANSITION TIMES OF SOURCE OUTPUTS

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## FIGURE 3

SOURCE OR SINK SATURATION VOLTAGE vs FREE-AIR TEMPERATURE


FIGURE 6

HIGH-LEVEL SINK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE


FIGURE 4

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF vs FREE-AIR TEMPERATURES


FIGURE 7

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE


FIGURE 9

SOURCE OR SINK SATURATION VOLTAGE vs SOURCE CURRENT OR SINK CURRENT


FIGURE 5

CASE TEMPERATURE DISSIPATION DERATING CURVE


FIGURE 8

## DESCRIPTION

The 75S207 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75207: The improved input sensitivity of $\pm 10 \mathrm{mV}$ makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles. The 75S207 features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.
The 75 S 207 also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

## FEATURES

- Functionally equivalent and pin compatible to SN75207
- 17ns maximum guaranteed propagation delay
- $20 \mu \mathrm{~A}$ maximum input bias current
- STTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages


## APPLICATIONS

- MOS memories sense amp
- A/D conversion
- High speed line receiver


## PIN CONFIGURATION



## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Positive supply voltage (V+) | +7 | V |
| Negative supply voltage (V-) | -7 | V |
| Differential input voltage | $\pm 6$ | V |
| Common mode input voltage | $\pm 5$ | V |
| Strobe/gate input voltage | +5.5 | V |
| Power dissipation | 600 | mW |
| Operating temperature rnage | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $\mathrm{V}+=+5.00, \mathrm{~V}-=-5.00, \mathrm{~T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise specified.

\begin{tabular}{|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{PARAMETER} \& \multirow[b]{2}{*}{TEST CONDITIONS} \& \multicolumn{3}{|c|}{75S207} \& \multirow[b]{2}{*}{UNIT} \\
\hline \& \& Min \& Typ \& Max \& \\
\hline \multicolumn{6}{|l|}{AMPLIFIER INPUT} \\
\hline Input offset voltage \& \(\mathrm{V}+=4.75, \mathrm{~V}-=-4.75\) \& \& \& 10 \& mV \\
\hline Input bias current @ \(25^{\circ} \mathrm{C}\) over temp. range \& \[
\begin{aligned}
\& \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\
\& \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25
\end{aligned}
\] \& \& 7.5 \& \[
\begin{aligned}
\& 20 \\
\& 40 \\
\& \hline
\end{aligned}
\] \& \[
\begin{aligned}
\& \mu \mathrm{A} \\
\& \mu \mathrm{~A} \\
\& \hline
\end{aligned}
\] \\
\hline Input offset current @ \(25^{\circ} \mathrm{C}\) over temp. range \& \[
\begin{aligned}
\& \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\
\& \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25
\end{aligned}
\] \& \& 1.0 \& \[
\begin{gathered}
5 \\
12
\end{gathered}
\] \& \[
\begin{aligned}
\& \mu \mathrm{A} \\
\& \mu \mathrm{~A} \\
\& \hline
\end{aligned}
\] \\
\hline Input common mode voltage range Input resistance Input capacitance \& \(\mathrm{V}+=4.75, \mathrm{~V}-=-4.75\) \& \(\pm 3\) \& \[
\begin{aligned}
\& 4 \\
\& 3
\end{aligned}
\] \& 6 \& \[
\begin{gathered}
\hline \mathrm{V} \\
\mathrm{k} \Omega \\
\mathrm{pF}
\end{gathered}
\] \\
\hline Voltage gain \& \& \& 5 \& \& \(\mathrm{V} / \mathrm{mV}\) \\
\hline \multicolumn{6}{|l|}{SCHOTTKY GATE/OUTPUT} \\
\hline IIH High level input current into 1 G or 2 G strobe \& \[
\begin{gathered}
\mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\
\mathrm{~V}_{1 H}=2.7 \mathrm{~V} \\
\mathrm{~V}_{1 H}=5.5 \mathrm{~V}
\end{gathered}
\] \& \& \& \[
\begin{gathered}
50 \\
1 \\
\hline
\end{gathered}
\] \& \[
\begin{aligned}
\& \mu \mathrm{A} \\
\& \mathrm{~mA}
\end{aligned}
\] \\
\hline \(\mathrm{IIH} \quad\)\begin{tabular}{l} 
High level input current \\
into common strobe \(S\)
\end{tabular} \& \[
\begin{gathered}
\mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\
\mathrm{~V}_{\mathrm{HH}}=2.7 \mathrm{~V} \\
\mathrm{~V}_{\mathbf{H}}=5.5 \mathrm{~V}
\end{gathered}
\] \& \& \& \[
\begin{gathered}
100 \\
2
\end{gathered}
\] \& \[
\begin{aligned}
\& \mu \mathrm{A} \\
\& \mathrm{~mA}
\end{aligned}
\] \\
\hline IIL \(\quad\) Low level input current
into 1 G or 2 G \& \[
\begin{gathered}
\mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\
\mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V}
\end{gathered}
\] \& \& \& -2.0 \& mA \\
\hline IIL Low level input current \& \[
\begin{gathered}
\mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\
\mathrm{~V} \text { IL }=0.5 \mathrm{~V}
\end{gathered}
\] \& \& \& -4.0 \& mA \\
\hline VOH High level output voltage \& \[
\begin{gathered}
\hline \mathrm{V}+=4.75, \mathrm{~V}_{(\mathrm{SS})}=2.0 \mathrm{~V} \\
\mathrm{~V}-=-4.75 \\
\text { LOAD }=-1 \mathrm{~mA} \\
\hline
\end{gathered}
\] \& 2.7 \& 3.4 \& \& v \\
\hline VoL Low level output voltage \& \[
\begin{gathered}
\mathrm{V}+=4.75, \mathrm{~V}-=-4.75 \\
\mathrm{ILOAD}=20 \mathrm{~mA} \\
\mathrm{~V}(\mathrm{~S})=2.0 \mathrm{~V}
\end{gathered}
\] \& \& \& 0.5 \& V \\
\hline \multicolumn{6}{|l|}{POWER SUPPLY REQUIREMENTS} \\
\hline V+

$\mathrm{V}-$ \& \& \[
$$
\begin{array}{r}
4.75 \\
-4.75 \\
\hline
\end{array}
$$

\] \& \[

$$
\begin{array}{r}
5.00 \\
-5.00 \\
\hline
\end{array}
$$

\] \& \[

$$
\begin{array}{r}
5.25 \\
-5.25 \\
\hline
\end{array}
$$

\] \& \[

$$
\begin{aligned}
& \mathrm{V} \\
& \mathrm{v} \\
& \hline
\end{aligned}
$$
\] <br>

\hline Icc+

Icc- \& $$
\begin{gathered}
\mathrm{V}+=5.25 \mathrm{~V} \\
\mathrm{~V}-=-5.25 \mathrm{~V} \\
\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}
\end{gathered}
$$ \& \& \[

$$
\begin{gathered}
20 \\
-11
\end{gathered}
$$

\] \& \[

$$
\begin{gathered}
30 \\
-15
\end{gathered}
$$

\] \& \[

$$
\begin{aligned}
& \mathrm{mA} \\
& \mathrm{~mA}
\end{aligned}
$$
\] <br>

\hline los $\begin{aligned} & \text { Short circuit } \\ & \text { output current }\end{aligned}$ \& $$
\begin{aligned}
& \mathrm{V}+=5.25 \\
& \mathrm{~V}-=-5.25 \\
& \hline
\end{aligned}
$$ \& -40 \& \& -100 \& mA <br>

\hline \multicolumn{6}{|l|}{LARGE SIGNAL SWITCHING SPEED} <br>

\hline $T_{p} L H(D)$ Low to high propagation delay from amp inputs to output 1 \& $$
\begin{gathered}
R_{L}=280 \Omega C_{L}=15 p F \\
T_{A}=25^{\circ} \mathrm{C}
\end{gathered}
$$ \& \& 12 \& 17 \& ns <br>

\hline $\mathrm{T}_{\mathrm{p}} \mathrm{HL}(\mathrm{D})$ High to low propagation delay from amp inputs to output 1 \& $$
\begin{gathered}
\mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}
\end{gathered}
$$ \& \& 9 \& 13 \& ns <br>

\hline $\mathrm{T}_{\mathrm{p} L H}(\mathrm{~S})$ Low to high propagation delay from strobes input to output2 \& $$
\begin{gathered}
\mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}
\end{gathered}
$$ \& \& 4.5 \& 6 \& ns <br>

\hline $\mathrm{T}_{\mathrm{p}} \mathrm{HL}(\mathrm{S})$ High to low propagation delay strobe input to output ${ }^{2}$ \& $$
\begin{gathered}
R_{L}=280 \Omega C_{L}=15 \mathrm{pF} \\
T_{A}=25^{\circ} \mathrm{C}
\end{gathered}
$$ \& \& 3.0 \& 4.5 \& ns <br>

\hline Maximum operating frequency \& $$
\begin{gathered}
\mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\
\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}
\end{gathered}
$$ \& 40 \& 55 \& \& MHz <br>

\hline
\end{tabular}

## NOTES

1. Response time measured from 0 V point of $\pm 100 \mathrm{mV}$ P-P 10 MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5 V point of input to 1.5 V point of the output.
3. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the 1.5 V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


RESPONSE TIME FOR various input overdrives


## DESCRIPTION

The 75S208 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75208. The improved input sensitivity of $\pm 10 \mathrm{mV}$ makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles.
The 75S208 features less than 17 ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

## FEATURES

- Functionally equivalent and pin compatible to 75208
- 17ns maximum guaranteed propagation delay
- $20 \mu \mathrm{~A}$ maximum input bias current
- STTL compatible strobes and outputs
- Open collector outputs
- Large common mode input voltage range
- Operates from standard supply voltages


## APPLICATIONS

- MOS memories sense amp
- A/D conversion
- High speed line receiver

PIN CONFIGURATION


EQUIVALENT SCHEMATIC


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Positive supply voltage (V+) | +7 | V |
| Negative supply voltage (V-) | -7 | V |
| Differential input voltage | $\pm 6$ | V |
| Common mode input voltage | $\pm 5$ | V |
| Strobe/gate input voltage | +5.5 | V |
| Power dissipation | 600 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $\mathrm{V}+=+5.00, \mathrm{~V}-=-5.00, \mathrm{~T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | 755208 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| AMPLIFIER INPUT Input offset voltage | $\mathrm{V}+=4.75, \mathrm{~V}-=-4.75$ |  |  | 10 | mV |
| Input bias current @ $25^{\circ} \mathrm{C}$ over temp. range | $\begin{aligned} & \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25 \end{aligned}$ |  | 7.5 | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input offset current @ $25^{\circ} \mathrm{C}$ over temp. range | $\begin{aligned} & \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25 \end{aligned}$ |  | 1.0 | $\begin{gathered} 5 \\ 12 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input common mode voltage range Input resistance Input capacitance | $\mathrm{V}+=4.75, \mathrm{~V}-=-4.75$ | $\pm 3$ | $\begin{aligned} & 4 \\ & 3 \end{aligned}$ | 6 | $\begin{gathered} \mathrm{V} \\ \mathrm{k} \Omega \\ \mathrm{pF} \end{gathered}$ |
| Voltage gain |  |  | 5 |  | $\mathrm{V} / \mathrm{mV}$ |
| SCHOTTKY GATE/OUTPUT CHARACTERISTICS |  |  |  |  |  |
| $I_{I H}$ High level input current <br> into $1 G$ or $2 G$ strobe | $\begin{gathered} \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V}_{I H}=2.7 \mathrm{~V} \\ \mathrm{~V}_{I H}=5.5 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 50 \\ 1 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| $I_{I H}$ High level input current <br> into common strobe $S$ | $\begin{gathered} \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V}_{I H}=2.7 \mathrm{~V} \\ \mathrm{~V}_{I H}=5.5 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 100 \\ 2 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| IIL Low level input current into 1 G or 2 G | $\begin{gathered} \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V}_{\text {IL }}=0.5 \mathrm{~V} \end{gathered}$ |  |  | -2.0 | mA |
| IIL Low level input current into common strobe $S$ | $\begin{gathered} \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V} \end{gathered}$ |  |  | -4.0 | mA |
| VOL Low level output voltage | $\begin{gathered} \mathrm{V}+=4.75, \mathrm{~V}_{\mathrm{I}(\mathrm{~S})}=2.0 \mathrm{~V} \\ \mathrm{~V}-=-4.75 \\ \mathrm{ILOAD}=20 \mathrm{~mA} \end{gathered}$ |  |  | 0.5 | V |
| $\mathrm{IOH} \quad$ High level output voltage | $\begin{aligned} \mathrm{V}_{\mathrm{CC}}+ & =5.25 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}} & =-5.25 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{OH}} & =5.25 \mathrm{~V} \end{aligned}$ |  |  | 250 | $\mu \mathrm{A}$ |
| POWER SUPPLY REQUIREMENTS |  |  |  |  |  |
|   <br> $\mathrm{V}+$ Supply voltage <br> $\mathrm{V}-$  |  | $\begin{array}{r} 4.75 \\ -4.75 \\ \hline \end{array}$ | $\begin{gathered} 5.00 \\ -5.00 \end{gathered}$ | $\begin{array}{r} 5.25 \\ -5.25 \\ \hline \end{array}$ | $\begin{aligned} & V \\ & V \end{aligned}$ |
| Icc+ Supply current Icc- | $\begin{gathered} \mathrm{V}+=5.25 \mathrm{~V} \\ \mathrm{~V}-=-5.25 \mathrm{~V} \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{gathered} 20 \\ -11 \end{gathered}$ | $\begin{gathered} 30 \\ -15 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| LARGE SIGNAL SWITCHING SPEED |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{p}} \mathrm{LH}(\mathrm{D})$ Low to high propagation delay from amp inputs to output1 | $\begin{aligned} R_{L}= & 280 \Omega C_{L}=15 \mathrm{pF} \\ & T_{A}=25^{\circ} \mathrm{C} \end{aligned}$ |  | 12 | 17 | ns |
| TpHL(D) High to low propagation delay from amp inputs to output 1 | $\begin{aligned} \mathrm{R}_{\mathrm{L}}= & 280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ |  | 9 | 13 | ns |
| $\mathrm{T}_{\mathrm{p}} \mathrm{LH}(\mathrm{S})$ Low to high propagation delay from strobes input to output2 | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 p F \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 6 | 10 | ns |
| $\mathrm{T}_{\mathrm{p}} \mathrm{HL}(\mathrm{S})$ High to low propagation delay strobe input to output2 | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 5 | 8 | ns |
| Maximum operating frequency | $\begin{aligned} & R_{L}= 280 \Omega C_{L}=15 p F \\ & T_{A}=25^{\circ} \mathrm{C} \end{aligned}$ | 25 | 35 |  | MHz |

## NOTES

1. Response time measured from 0 V point of $\pm 100 \mathrm{MHz}$ square wave to the 1.5 point of the output.
2. Response time measured from 1.5 V point of input to 1.5 V point of the output.
3. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the 1.5 V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

RESPONSE TIME vs TEMPERATURE


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


## DESCRIPTION

The 7520 series of dual channel sense amplifiers are designed for use with high speed core memory systems. These sense amplifiers detect low level bipolar differential signals from the memory and provide the interface circuitry between the memory element and the logic system. The device outputs are compatible with TTL and DTL logic.

The 7520 circuit may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The 7522 circuit has a high fan-out, singleended, open-collector output. In addition, it may be used to expand the input capability to a 7520 device, or to perform the wiredAND function.

The 7524 circuit provides for independent dual-channel sensing with separate outputs. The 75234 is similar to the 7524 , but has an inverted output function. The 75232 is an open-collector version of the 75234 . The 7528 circuit is identical in function to the 7524 , but has the output of each preamplifier stage brought out to test points.

## FEATURES

- High speed-25ns propagation delay
- Adjustable input threshold levels
- $\pm 4 \mathrm{mV}$ threshold uncertainty
- Wide choice of output functions
- High dc noise margin


## PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| Vcc+ | Supply voltage | 7 | V |
| $V_{\text {cc- }}$ | Supply voltage | -7 | V |
| $V$ ID | Differential input voltage | $\pm 5$ | V |
| VIN | Input voltage | 5.5 | V |
| Vout | Off-state voltage applied to open-collector outputs | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {stg }}$ | Storage temperature range | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| PD | Power dissipation | 500 | mW |

BLOCK DIAGRAMS


EQUIVALENT SCHEMATICS


EQUIVALENT SCHEMATICS (Cont'd)



EQUIVALENT SCHEMATICS (Cont'd)


DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=0$ to $70^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}+}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=-5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\mathrm{V}_{\text {T }}$ | Differential input threshold voltage |  | $\begin{aligned} & V_{\text {ref }}=15 \mathrm{mV} \\ & V_{\text {ref }}=40 \mathrm{mV} \end{aligned}$ | $\begin{aligned} & 11 \\ & 36 \end{aligned}$ | $\begin{aligned} & 15 \\ & 40 \end{aligned}$ | $\begin{aligned} & 19 \\ & 44 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| VICF | Common-mode input firing voltage | $\begin{gathered} V_{\text {ref }}=40 \mathrm{mV}, V_{(S)}=V_{I H} \\ t_{r} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{w}}=50 \mathrm{~ns} \end{gathered}$ |  | $\pm 2.5$ |  | V |
| IB | Differential input bias current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}+}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=-5.25 \mathrm{~V} \\ \mathrm{~V}_{\text {ID }}=0 \end{gathered}$ |  | 30 | 75 | $\mu \mathrm{A}$ |
| los | Differential input offset current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}+}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}-}=-5.25 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{ID}}=0 \end{gathered}$ |  | 0.5 |  | $\mu \mathrm{A}$ |
| $\begin{aligned} & \hline \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{L}} \end{aligned}$ | High level input voltage Low level input voltage |  | 2 |  | 0.8 | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| VOH <br> VoL | High level output voltage <br> Low level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}+}= 4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}-}=-4.75 \mathrm{~V} \\ & \mathrm{IOH}=-400 \mu \mathrm{~A}, \mathrm{NOT} \\ & \mathrm{~V}_{\mathrm{CC}}+=4523275 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}-}=-4.75 \mathrm{~V} \\ & \mathrm{IOL}^{2}=16 \mathrm{~mA} \end{aligned}$ | 2.4 | $\begin{gathered} \hline 4 \\ 0.25 \end{gathered}$ | 0.4 | V |
| $\begin{aligned} & \mathrm{IOH} \\ & \mathrm{IH} \end{aligned}$ | High level output current <br> High level input current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}+}=4.75 \mathrm{~V}, \mathrm{VCC}_{\mathrm{CC}}=-4.75 \mathrm{~V} \\ \mathrm{VOH}_{\mathrm{OH}}=5.25 \mathrm{~V}, 75232 \mathrm{ONLY} \\ \mathrm{~V}_{\mathrm{CC}+}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}-}=-5.25 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IH}}=2.4 \mathrm{~V} \end{gathered}$ |  |  | $\begin{aligned} & 250 \\ & 40 \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| IIL | Low level input current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}+}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}-}=-5.25 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IL}}=0.4 \mathrm{~V} \end{gathered}$ |  | -1.0 | -1.6 | mA |
| los los | Short-circuit output current <br> Short-circuit output current | $\mathrm{V}_{\mathrm{CC}+}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}-}=-5.25 \mathrm{~V}$ <br> NOT Q output (pin 13) on 7520 <br> $\mathrm{V}_{\mathrm{CC}}+=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=-5.25 \mathrm{~V}$ <br> Q output (pin 13) ONLY on 7520 | $\begin{gathered} \hline-2.1 \\ -3 \end{gathered}$ |  | $\begin{gathered} \hline-3.5 \\ -5 \end{gathered}$ | mA <br> mA |
| $\begin{aligned} & \text { Icc }+ \\ & \text { Icc- } \end{aligned}$ | Supply current from VCC+ Supply current from Vcc- | $\mathrm{V}_{\mathrm{CC}+}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {CC- }}=-5.25 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{gathered} 27 \\ -15 \end{gathered}$ | $\begin{gathered} 40 \\ -20 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TO | FROM | TEST CONDITIONS | 7520 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max |  |
| $t_{p d}(1)$ | DQ |  | Q output | A1/A2 or B1/B2 | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 25 | 40 | ns |
| $t_{p d}(0)$ | DQ | Q output | A1/A2 or B1/B2 | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 20 |  | ns |
| $t_{p d}(1)$ | D $\bar{Q}$ | $\overline{\mathrm{Q}}$ output | A1/A2 or B1/B2 | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 30 |  | ns |
| $t_{\text {pd( }}(0)$ | D $\bar{Q}$ | $\overline{\mathrm{Q}}$ output | A1/A2 or B1/B2 | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 35 | 55 | ns |
| $t_{p d}(1)$ | SQ | Q output | Strobe A or B | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 15 | 30 | ns |
| $t_{p d}(0)$ | SQ | Q output | Strobe A or B | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 20 |  | ns |
| $t_{p d}(1)$ | S $\bar{Q}$ | $\overline{\mathrm{Q}}$ output | Strobe A or B | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 30 |  | ns |
| $t_{p d}(0)$ | S $\bar{Q}$ | $\bar{Q}$ output | Strobe A or B | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 35 | 55 | ns |
| $t_{p d}(1)$ | $\mathrm{G}_{Q Q}$ | Q output | Gate Q | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{L}=288 \Omega$ |  | 15 | 25 | ns |
| $t \mathrm{pd}(0)$ | $\mathrm{GQQ}_{Q}$ | Q output | Gate Q | $\mathrm{C}_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 10 |  | ns |
| $t_{p d}(1)$ | $\mathrm{G}_{\mathrm{Q}} \overline{\mathrm{Q}}$ | $\bar{Q}$ output | Gate Q | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 15 |  | ns |
| $t_{\text {pd }}(0)$ | $\mathrm{G}_{\mathrm{Q}} \overline{\mathrm{Q}}$ | $\overline{\mathrm{Q}}$ output | Gate Q | $\mathrm{C}_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 20 | 30 | ns |
| $t_{p d}(1)$ | $\mathrm{G}_{\overline{\mathrm{Q}}}^{\underline{\mathrm{Q}}}$ | $\overline{\mathrm{Q}}$ output | Gate $\bar{Q}$ | $\mathrm{C}_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 15 |  | ns |
| $t_{\text {pd }}(0)$ | $\mathrm{G} \overline{\mathrm{Q}} \overline{\mathrm{Q}}$ | $\bar{Q}$ output | Gate $\bar{Q}$ | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 10 | 20 | ns |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TO | FROM | TEST CONDITIONS | 7522 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max |  |
| $\mathrm{tpd}_{\text {(1) }}$ | D |  | Y output | A1/A2 or B1/B2 | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 20 |  | ns |
| $t_{\text {pd( }}$ ( $)$ | D | Y output | A1/A2 or B1/B2 | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 30 | 45 | ns |
| $t_{\text {pd(1) }}$ | S | Y output | Strobe A or B | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 20 |  | ns |
| $t_{\text {pd }}(0)$ | S | Y output | Strobe A or B | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 20 | 40 | ns |
| $\mathrm{tpd}_{\text {(1) }}$ | G | Y output | Gate Y | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 10 |  | ns |
| $t_{\text {pd }}(0)$ | G | Y output | Gate Y | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 15 | 25 | ns |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TO | FROM | TEST CONDITIONS | 7524/7528 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max |  |
| $t_{\text {pd(1) }}$ | D |  | Output A or B | A1/A2 or B1/B2 | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 25 | 40 | ns |
| $t_{\text {pd( }}(0)$ | D | Output A or B | A1/A2 or B1/B2 | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 20 |  | ns |
| $\mathrm{tpd}_{\text {(1) }}$ | S | Output A or B | Strobe A or B | $C_{L}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 15 | 30 | ns |
| $t \mathrm{pd}(0)$ | S | Output A or B | Strobe A or B | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 20 |  | ns |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TO | FROM | TEST CONDITIONS | 75232/75234 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max |  |
| $\mathrm{t}_{\mathrm{pd}(1)}$ | D |  | Output A or B | A1/A2 or B1/B2 | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 25 |  | ns |
| $t_{\text {pd( }}$ ( $)$ | D | Output A or B | A1/A2 or B1/B2 | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 25 | 40 | ns |
| $t_{\text {pd(1) }}$ | S | Output A or B | Strobe A or B | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=288 \Omega$ |  | 25 |  | ns |
| $t_{\text {pd( }}$ ( $)$ | S | Output A or B | Strobe A or B | $C_{L}=15 p F, R_{L}=288 \Omega$ |  | 15 | 30 | ns |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| torD | Differential-input overload recovery time |  | $\begin{aligned} V_{I D} & =2 V \\ t_{r}=t_{f} & =20 n s \end{aligned}$ |  | 20 |  | ns |
| torC | Common-mode input overload recovery time | $\begin{gathered} V_{I C}= \pm 2 V \\ t_{r}=t_{f}=20 n s \end{gathered}$ |  | 20 |  | ns |
| $t_{\text {cyc }}$ (min) | Minimum cycle time |  |  | 200 |  | ns |

## TEST LOAD CIRCUITS—7520



NOTES

1. Pulse generators have the following characteristics:
$Z_{\text {OUT }}=50 \Omega, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=15\left( \pm 5 \mathrm{hss}, \mathrm{t}_{\mathrm{p} 1}=100 \mathrm{~ns}\right.$,
$\mathrm{t}_{\mathrm{p} 2}=300 \mathrm{~ns}$, and $P R R=1 \mathrm{MHz}$.
2. $\mathrm{C}_{1}$ includes probe and jig capacitance.


## VOLTAGE WAVEFORMS-7520



TEST LOAD CIRCUIT-7522


NOTES

1. Pulse generators have the following characteristics:

Zout $=50 \Omega, \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=15( \pm 5) \mathrm{ns}, \mathrm{t}_{\mathrm{p} 1}=100 \mathrm{~ns}$,
$\mathrm{t}_{\mathrm{p} 2}=300 \mathrm{~ns}$, and $\mathrm{PRR}=1 \mathrm{MHz}$.
2. Strobe input pulse is applied to Strobe $A$ when inputs $A_{1}-A_{2}$ are being tested and to Strobe $B$ when inputs $B_{1}-B_{2}$ are being tested.
3. $\mathrm{C}_{1}$ includes probe and jig capacitance.

VOLTAGE WAVEFORM-7522


TEST LOAD CIRCUIT—7524/7528


VOLTAGE WAVEFORM—7524/7528

## DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS



## TEST LOAD CIRCUIT-75232/75234



NOTES

1. The pulse generators have the following characteristics
$Z_{\text {OUT }}=50 \Omega, \mathrm{t}_{\mathrm{r}}=15 \pm 5 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}}=15 \pm 5 \mathrm{~ns}, \mathrm{t}_{\mathrm{w}} 1=100 \mathrm{~ns}$,
$\mathrm{t}_{\mathrm{w} 2}=300 \mathrm{~ns}$, and $P R R=1 \mathrm{MHz}$.
2. The strobe input pulse is applied to Strobe 1 S when inputs 1A1-1A2 are being tested and to Strobe 2 S when inputs 2A1-2A2 are being tested.
3. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.

VOLTAGE WAVEFORM-75232/75234


TYPICAL PERFORMANCE CHARACTERISTICS


THRESHOLD VOLTAGE vs REFERENCE VOLTAGE


COMMON MODE FIRING VOLTAGE vs FREE-AIR TEMPERATURE


LOGICAL 1 OUTPUT VOLTAGE vs LOAD CURRENT


THRESHOLD VOLTAGE vs SUPPLY VOLTAGE


DIFFERENTIAL-INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE


LOGICAL 0 OUTPUT VOLTAGE vs SINK CURRENT


NORMALIZED THRESHOLD VOLTAGE vs PULSE REPETITION RATE


DIFFERENTIAL-INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE


TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The 75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400 mA (source/sink) switch pairs with decoding capability from four address lines. Two address inputs ( $B$ and $C$ ) are used for mode selection, ie., source or sink. The other two address inputs (A and D) are used for switch-pair selection (output pair $\mathrm{Y} / \mathrm{Z}$ or W/X).
The sink circuit is composed of an inverting switch with a TTL input. The source circuit is an emitter-follower driven from a TTL input.

ABSOLUTE MAXIMUM RATINGS

FEATURES

- 400 mA output capability
- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- Fast switching times
- Output short-circuit protection

Over operating case temperature range unless otherwise specified.

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage VCC ${ }^{1}$ | 17 | V |
| Input voltage ${ }^{2}$ | 5.5 | $\vee$ |
| Operating case temperature range | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| Continuous total power | 800 | mW |
| dissipation at (or |  |  |
| below) $70^{\circ} \mathrm{C}$ case temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range |  |  |

PIN CONFIGURATIONS


GND 1 and GND 2 are to be used in parallel

NOTES

1. Voltage values are with respect to network ground terminal
2. Input signals must be zero or positive with respect to network ground terminal.

DC ELECTRICAL CHARACTERISTICS $T_{A}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}, \mathrm{V}_{C C}=14 \mathrm{~V}$ unless otherwise specified.*

|  | PARAMETER | TEST. FIGURE | TEST CONDITIONS |  | IMITS |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ* | Max |  |
| $\begin{aligned} & V_{I H} \\ & V_{I L} \end{aligned}$ | High-level input voltage Low-level input voltage | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ |  | 3.5 |  | 0.8 | $\begin{aligned} & V \\ & V \end{aligned}$ |
| $\begin{aligned} & I_{H} \\ & I_{\mid H} \end{aligned}$ | High-level input current, address inputs High-level input current, timing inputs | $1$ <br> 1 | $\begin{aligned} & V_{1}=5 V \\ & V_{1}=5 V \end{aligned}$ |  |  | $\begin{aligned} & 200 \\ & 100 \end{aligned}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| ILL IIL | Low-level input current, address inputs Low-level input current, timing inputs | 1 1 | $\begin{aligned} & V_{1}=0 V \\ & V_{1}=0 V \end{aligned}$ |  |  | $\begin{gathered} -6 \\ -12 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & V_{(S A T)} \\ & V_{(S A T)} \end{aligned}$ | Sink saturation voltage Source saturation voltage | $\begin{aligned} & 2 \\ & 2 \end{aligned}$ | $\begin{gathered} \text { ISINK } \cong 420 \mathrm{~mA}, R_{\mathrm{L}}=53 \Omega \\ \text { ISOURCE } \cong 420 \mathrm{~mA}, R_{\mathrm{L}}=47.5 \Omega \end{gathered}$ |  | $\begin{aligned} & 0.75 \\ & 0.75 \end{aligned}$ | $\begin{aligned} & 0.85 \\ & 0.85 \end{aligned}$ | $\begin{aligned} & v \\ & v \end{aligned}$ |
| loff | Output off-state current | 1 | $\mathrm{V}_{1}=0 \mathrm{~V}$ |  | 125 | 200 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \mathrm{ICC} \\ & \mathrm{ICC} \\ & \mathrm{ICC} \end{aligned}$ | Supply current, all sources and sinks off <br> Supply current, either sink selected Supply current, either source selected | $3$ $\begin{aligned} & 4 \\ & 4 \end{aligned}$ | $\mathrm{V}_{1}=0 \mathrm{~V}$ |  | $\begin{aligned} & 12.5 \\ & 30 \\ & 25 \end{aligned}$ | $\begin{aligned} & 15 \\ & 42 \\ & 35 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

- NOTE

All typical values are at $T_{A}=25^{\circ} \mathrm{C}$.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, ~ V C C=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST FIGURE | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  | Typ | Max |  |
| $\begin{aligned} & \text { tPLH } \\ & \text { tPHL } \end{aligned}$ | Propagation delay time <br> Low-to-high-level source output <br> Propagation delay time <br> High-to-low-level source output |  | $\begin{aligned} & 5 \\ & 5 \end{aligned}$ | $\begin{gathered} R_{L 1}=53 \Omega \\ R_{L 2}=500 \Omega \\ C_{L}=20 p F \end{gathered}$ |  |  | $\begin{aligned} & 90 \\ & 50 \end{aligned}$ | ns ns |
| tpli <br> tpHL <br> $t_{s}$ | Propagation delay time Low-to-high-level sink output Propagation delay time High-to-low-level sink output Sink storage time | 6 6 | $\begin{aligned} R_{L} & =53 \Omega \Omega \\ C_{L} & =20 \mathrm{pF} \end{aligned}$ |  |  | 110 40 70 | ns ns ns |

## EQUIVALENT SCHEMATIC



## PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* $\quad \mathrm{V}_{\mathrm{IL}}, \mathrm{V}_{\text {IH }}, \mathrm{I}_{\mathrm{IL}}, \mathrm{I}_{\mathrm{IH}}$, AND $\mathrm{I}_{\text {OFF }} \quad$ TEST TABLE FOR $\mathrm{I}_{\mathrm{IL}}$


| APPLY 3.5V | GROUND | TEST <br> IIL |
| :---: | :---: | :---: |
|  |  |  |
| B,C,E,F, and G | A and D | A |
| B,C,E,F, and G | A and D | D |
| A,D,E,F, and G | B and C | B |
| A,D,E,F, and G | B and C | C |
| A,B,C,C,F, and G | E | E |
| A,B,C,D,E, and G | F | F |
| A,B,C,D,E, and F | G | G |

NOTES

1. Check $V_{I H}$ and $V_{I L}$ per Function Table.
2. Measure IIL per Test Table.
3. When measuring $I_{I H}$, all other inputs are at ground. Each input is tested separately

Figure 1


NOTE
This parameter must be using pulse techniques,
$\mathrm{t}_{\mathrm{w}}=500 \mathrm{~ns}$, duty cycle $\leq 1 \%$.
*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

ICC (ALL OUTPUTS OFF)

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 2
Figure 3

PARAMETER MEASUREMENT INFORMATION (Cont'd)


1. Ground $A$ and $B$, apply 3.5 V to C and D , and measure ICC (output W is on).
2. Ground $B$ and $D$, apply 3.5 V to $A$ and $C$, and measure Icc (output $Z$ is on).
3. Ground $A$ and $C$, apply 3.5 V to $B$ and $D$, and measure Icc (output $X$ is on).
4. Ground $C$ and $D$, apply 3.5 V to $A$ and $B$, and measure Icc (output $Y$ is on).
*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
Figure 4

## SWITCHING CHARACTERISTICS

## SOURCE-OUTPUT SWITCHING TIMES

TEST CIRCUIT


VOLTAGE WAVEFORM


## NOTES

1. The input waveform is supplied by a generator with the following characteristics: $t_{r}=t_{f}$ $=10 \mathrm{~ns}$, duty cycle $\leq 1 \%$, and $Z_{\text {OUT }} \approx 50 \Omega$.
2. When measuring delay times at output $X$, apply $+5 V$ to input $D$, and ground $A$. When measuring delay times at output $Y$, apply $+5 V$ to input $A$, and ground $D$.
3. $C_{L}$ includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5 W .

Figure 5

SWITCHING CHARACTERISTICS (Cont'd)


## sECTION 7 interface

## DESCRIPTION

The DS3611 series of dual peripheral drivers was designed for applications where higher breakdown voltage is required than that provided by the 75451 series.

The pin out for the 3611 series is identical to those of the 75451 through 75454 . The 3611 series feature high voltage outputs ( 80 V breakdown in the "off" state) as well as high current $(300 \mathrm{~mA}$ /driver in the on state).

## FEATURES

-     - High voltage PNP inputs
- PMOS/CMOS TTL or DTL compatible inputs
-     - Low input currents
- High voltage outputs 80 V (off)
- High current- $300 \mathrm{~mA} /$ driver (on)
- Input clamping diodes
- Choice of logic function
- DS3611/12/13/14, DS1611/12/13/14
- Military qualifications pending


## NOTE

- Special Signetics features


## APPLICATIONS

- Power drivers
- Relay drivers
- Lamp drivers
- Mos drivers
- Memory drivers


## PIN CONFIGURATIONS



DUAL NAND DRIVER DS3612



Pin 4 is in electrical contact with the case.

## DS3614T



Pin 4 is in electrical contact with the case.

## BLOCK DIAGRAMS



## EQUIVALENT SCHEMATICS



NOTE
One circuit only shown

## ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| VCC | Supply voltage continuous momentary (1 second) | 7 15 | $\begin{aligned} & V \\ & V \end{aligned}$ |
| VIN | Input voltage | 30 | V |
| Vout | Output voltage (off state) | 80 | V |
| lout | Output current (continuous) | 300 | mA |
| $P_{\text {D }}$ | Power dissipation* | 750 | mW |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
|  | Lead temperature (soldering, 10 sec ) | 300 | ${ }^{\circ} \mathrm{C}$ |

NOTE
*The maximum, junction temperature is $150^{\circ} \mathrm{C}$. Derate at $162^{\circ} \mathrm{C} /$ Watt above $25^{\circ} \mathrm{C}$.
DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=5 \mathrm{~V}, 0^{\circ} \mathrm{C}<\mathrm{T}_{A}<70^{\circ} \mathrm{C}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | DS3611 SERIES |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \\ & \mathrm{~V}_{\mathrm{I}} \end{aligned}$ | Logical " 1 " input voltage Logical "0" input voltage Input clamp voltage | $\begin{gathered} V_{C C}=4.75 \mathrm{~V} \\ V_{C C}=4.75 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{I}_{1}=-12 \mathrm{~mA} \end{gathered}$ | 2.0 | -1.2 | $\begin{gathered} 0.8 \\ -1.5 \\ \hline \end{gathered}$ | $\begin{aligned} & v \\ & v \\ & v \end{aligned}$ |
| IIH <br> IL | Logical " 1 " input current <br> Logical " 0 " input current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=2.4 \mathrm{~V} \\ \mathrm{~V}_{\text {IN }}=5.5 \mathrm{~V} \\ \mathrm{~V}_{\text {IN }}=30 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0.4 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} <1 \\ 1 \\ -50 \\ \hline \end{gathered}$ | $\begin{gathered} 10 \\ 10 \\ 100 \\ -100 \\ \hline \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| VoL | Output low voltage | $\begin{aligned} & \mathrm{V}_{\text {IN }}= 0.8 \mathrm{~V}(\mathrm{DS} 3611 / 3613) \\ & \mathrm{VIN}_{\mathrm{I}}=2.0 \mathrm{~V}(\mathrm{DS} 3612 / 3614) \\ & \mathrm{VCC}= 4.75 \mathrm{~V}, 10 \mathrm{loL}=100 \mathrm{~mA} \\ & 10 \mathrm{~L}=300 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 0.20 \\ & 0.45 \end{aligned}$ | $\begin{aligned} & 0.40 \\ & 0.70 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| VOH | Output breakdown voltage | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=2.0 \mathrm{~V}(\mathrm{DS} 3611 / 3613) \\ \mathrm{V}_{\mathrm{IN}}=0.8 \mathrm{~V}(\mathrm{DS} 3612 / 3614) \\ \mathrm{IOH}^{2}=100 \mu \mathrm{~A} \end{gathered}$ | 80 |  |  | V |
| IOH | Output leakage current | $\begin{gathered} V_{\text {IN }}=2.0 \mathrm{~V}(\mathrm{DS} 3611 / 3613) \\ \mathrm{VIN}^{2}=0.8 \mathrm{~V}(\mathrm{DS} 3612 / 3614) \\ \mathrm{VOUT}^{2}=80 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \\ \mathrm{VCC}_{\text {C }}=\text { open } \end{gathered}$ |  |  | $\begin{aligned} & 100 \\ & 100 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Icch | Supply current with outputs high | $\begin{gathered} V_{C C}=5.25 \mathrm{~V}: \\ \text { DS3611-VIN }=5 \mathrm{~V} \\ \text { DS3612-VIN }=0 \mathrm{~V} \\ \text { DS3613-VIN }=5 \mathrm{~V} \\ \text { DS } 3614-V_{I N}=0 V \\ \hline \end{gathered}$ |  | $\begin{gathered} 5 \\ 8 \\ 8 \\ 8 \\ \hline \end{gathered}$ | $\begin{aligned} & 11 \\ & 14 \\ & 14 \\ & 17 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| ICCL | Supply current with outputs low | $\begin{gathered} V_{C C}=5.25 \mathrm{~V}: \\ \text { DS3611-VIN }=0 \mathrm{~V} \\ \text { DS3612-VIN }=5 \mathrm{~V} \\ \text { DS } 3613-V_{\mathbb{~}}=0 \mathrm{~V} \\ \text { DS } 3614-V_{I N}=5 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & 44 \\ & 47 \\ & 44 \\ & 49 \end{aligned}$ | $\begin{aligned} & 69 \\ & 71 \\ & 73 \\ & 79 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS $V_{C C}=5 V, T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | DS3611 SERIES |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| TPLH | Propagation delay time, low-to-high output |  | $10 \simeq 200 \mathrm{~mA}$ |  |  |  |  |
|  |  | $C_{L}=15 \mathrm{pf}$ |  |  |  |  |
|  |  | $R_{L}=50 \Omega$ |  |  |  |  |
|  |  | DS3611 |  | 130 |  | ns |
|  |  | DS3612 |  | 110 |  | ns |
|  |  | DS3613 |  | 125 |  | ns |
|  |  | DS3614 |  | 220 |  | ns |
| TPHL | Propagation delay time, high-to-low output | DS3611 |  | 125 |  | ns |
|  |  | DS3612 |  | 110 |  | ns |
|  |  | DS3613 |  | 125 |  | ns |
|  |  | DS3614 |  | 150 |  | ns |

TYPICAL CIRCUIT


TIMING WAVEFORMS


## DESCRIPTION

The DS7820, specified from $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$, and the DS8820, specified from $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for $\pm 10$-percent supply voltage variations and over the entire input voltage range.

## FEATURES

- Operation from a single +5 V logic supply
- Input voltage range of $\pm 15 \mathrm{~V}$
- Independent channel strobing
- High input resistance
- Fanout of two with DTL or TTL
- Output can be wire OR'ed
- DS7820 Mil std 883A,B,C available


## PIN CONFIGURATION



## CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | 8.0 | V |
| Input voltage | $\pm 20$ | V |
| Differential input voltage | $\pm 20$ | V |
| Strobe voltage | 8.0 | V |
| Output sink current | 25 | mA |
| Power dissipation | 600 | mW |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| DS7820 | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| DS8820 | 300 | ${ }^{\circ} \mathrm{C}$ |

NOTE
"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

DC ELECTRICAL CHARACTERISTICS Specifications apply for $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{cc}} \leq 5.5$,
$-15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 15 \mathrm{~V}$ and $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ for the DS7820 or $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}$ for the DS8820 unless otherwise specified. Typical values given are for $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ unless stated differently. $1,2,3$

| PARAMETER |  | TEST CONDITIONS | DS7820 |  |  | DS8820 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & V_{\text {TH }} \\ & V_{\text {TH }} \end{aligned}$ | Input threshold Input threshold |  | $\begin{gathered} V_{\text {IN }}=0 V \\ -15 V \leq V_{\text {IN }} \leq 15 V \end{gathered}$ | $\begin{aligned} & \hline-0.5 \\ & -1.0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 1.0 \end{aligned}$ | $\begin{array}{r} -0.5 \\ -1.0 \\ \hline \end{array}$ | 0 | $\begin{aligned} & 0.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{VOH} \\ & \mathrm{VOL} \end{aligned}$ | High output level Low output level | $\begin{aligned} & \text { Iout } \leq-0.2 \mathrm{~mA} \\ & \text { I }_{\text {SINK }} \leq 3.5 \mathrm{~mA} \end{aligned}$ | $\begin{gathered} 2.5 \\ 0 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 5.5 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 2.5 \\ 0 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \hline 5.5 \\ & 0.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| $\begin{aligned} & \hline \text { RIN }- \\ & \text { RIN }+ \\ & \text { RT }^{2} \\ & \hline \end{aligned}$ | Inverting input resistance Noninverting input resistance Line termination resistance |  | $\begin{aligned} & 3.6 \\ & 1.8 \\ & 120 \\ & \hline \end{aligned}$ | $\begin{array}{r} \hline 5.0 \\ 2.5 \\ 170 \\ \hline \end{array}$ | 250 | $\begin{aligned} & \hline 3.6 \\ & 1.8 \\ & 120 \\ & \hline \end{aligned}$ | $\begin{array}{r} 5.0 \\ 2.5 \\ 170 \\ \hline \end{array}$ | 250 | $\begin{gathered} \mathrm{k} \Omega \\ \mathrm{k} \Omega \\ \Omega \\ \hline \end{gathered}$ |
| $\begin{aligned} & \text { IST } \\ & \text { IST } \end{aligned}$ | Strobe current Strobe current | $\begin{aligned} & V_{\text {Strobe }}=0.4 \mathrm{~V} \\ & V_{\text {Strobe }}=5.5 \mathrm{~V} \\ & \hline \end{aligned}$ |  | 1.0 | $\begin{aligned} & 1.4 \\ & -5 \end{aligned}$ |  | 1.0 | $\begin{aligned} & 1.4 \\ & -5 \end{aligned}$ | $\mathrm{mA}_{\mu \mathrm{A}}$ |
| $\begin{aligned} & \hline \text { Icc } \\ & \text { Icc } \\ & \text { Icc } \end{aligned}$ | Supply current ${ }^{3}$ Supply current ${ }^{3}$ Supply current ${ }^{3}$ | $\begin{aligned} V_{I N} & =15 \mathrm{~V} \\ V_{\text {IN }} & =0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}} & =-15 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 3.2 \\ & 5.8 \\ & 8.3 \end{aligned}$ | $\begin{gathered} \hline 6.0 \\ 10.2 \\ 15.0 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \hline 3.2 \\ & 5.8 \\ & 8.3 \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 6.0 \\ 10.2 \\ 15.0 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \hline \operatorname{lin}+ \\ & \operatorname{lin}+ \\ & \operatorname{lin}+ \end{aligned}$ | Noninverting input current Noninverting input current Noninverting input current | $\begin{aligned} & V_{\text {IN }}=15 \mathrm{~V} \\ & V_{\text {IN }}=0 \mathrm{~V} \\ & V_{I N}=-15 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & -1.6 \\ & -9.8 \end{aligned}$ | $\begin{array}{r} 3.0 \\ -1.0 \\ -7.0 \\ \hline \end{array}$ | 7.0 | $\begin{aligned} & -1.6 \\ & -9.8 \end{aligned}$ | $\begin{gathered} 5.0 \\ -1.0 \\ -7.0 \\ \hline \end{gathered}$ | 7.0 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \operatorname{lin}- \\ & \operatorname{lin}- \\ & \operatorname{lin}- \end{aligned}$ | Inverting input current Inverting input current Inverting input current | $\begin{aligned} V_{I N} & =15 \mathrm{~V} \\ V_{I N} & =0 \mathrm{~V} \\ V_{I N} & =-15 \mathrm{~V} \end{aligned}$ | -4.2 | $\begin{gathered} \hline 3.0 \\ 0 \\ -3.0 \end{gathered}$ | $\begin{gathered} 4.2 \\ -0.5 \end{gathered}$ | -4.2 | $\begin{gathered} 3.0 \\ 0 \\ -3.0 \end{gathered}$ | $\begin{gathered} \hline 4.2 \\ -0.5 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

NOTES

1. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
2. Only one output at a time should be shorted.
3. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | DS7820 |  |  | DS8820 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{T}_{\mathrm{R}}$ Response time | $\mathrm{C}_{\text {delay }}=0$ |  | 40 |  |  | 40 |  | ns |
| $\mathrm{T}_{\mathrm{R}}$ Response time | $C_{\text {delay }}=100 \mathrm{pF}$ |  | 150 |  |  | 150 |  | ns |

## DS7820-DS8820 TYPICAL APPLICATION



[^4]
## DESCRIPTION

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic " 1 " for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range $\left(-55^{\circ} \mathrm{C}\right.$ to $125^{\circ} \mathrm{C}$ and $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ respectively), over the entire input voltage range, for $\pm 10 \%$ supply voltage variations.

## FEATURES

- Operation from a single +5 V logic supply
- Input voltage range of $\pm 15 \mathrm{~V}$
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible


## PIN CONFIGURATION



## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | 8.0 | V |
| Input voltage | $\pm 20$ | V |
| Differential input voltage | $\pm 20$ | V |
| Strobe voltage | 8.0 | V |
| Output sink current | 50 | mA |
| Power dissipation | 600 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| DS7820A | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| DS8820A | 300 |  |

*NOTE
"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. $1,2,3,4$

| PARAMETER |  | TEST CONDITIONS |  | DS7820A/DS8820A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $V_{\text {TH }}$ | Differential threshold voltage |  |  | $\begin{aligned} & \text { lout }=-400 \mu \mathrm{~A} \\ & \text { VOUT } \geq 2.5 \mathrm{~V} \\ & \text { lout }=+16 \mathrm{~mA} \\ & \text { VOUT } \leq 0.4 \mathrm{~V} \end{aligned}$ | $\begin{aligned} -3 V & \leq V_{C M} \leq+3 V \\ -15 V & \leq V_{C M} \leq+15 V \\ -3 V & \leq V_{C M} \leq+3 V \\ -15 V & \leq V_{C M} \leq+15 V \end{aligned}$ |  | $\begin{gathered} 0.06 \\ 0.06 \\ -0.08 \\ -0.08 \end{gathered}$ | $\begin{gathered} 0.5 \\ 1.0 \\ -0.5 \\ -1.0 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{RI}^{-}$ | Inverting input resistance | $-15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq+15 \mathrm{~V}$ |  | 3.6 | 5 |  | $k \Omega$ |
| $\mathrm{Rl}^{+}$ | Non-inverting input resistance | $-15 \mathrm{~V} \leq \mathrm{V}_{\text {CM }} \leq+15 \mathrm{~V}$ |  | 1.8 | 2.5 |  | $k \Omega$ |
| $\mathrm{R}_{\mathrm{T}}$ | Line termination resistance |  |  | 120 | 170 | 250 | $\Omega$ |
| $1^{-}$ | Inverting input current | $\begin{aligned} & V_{C M}=15 \mathrm{~V} \\ & V_{C M}=0 \mathrm{~V} \\ & V_{C M}=-15 \mathrm{~V} \end{aligned}$ |  |  | $\begin{gathered} \hline 3.0 \\ 0 \\ -3.0 \\ \hline \end{gathered}$ | $\begin{gathered} 4.2 \\ -0.5 \\ -4.2 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $11^{+}$ | Non-inverting input current | $\begin{aligned} & V_{C M}=15 \mathrm{~V} \\ & V_{C M}=0 \mathrm{~V} \\ & V_{C M}=-15 \mathrm{~V} \end{aligned}$ |  |  | $\begin{gathered} 5.0 \\ -1.0 \\ -7.0 \end{gathered}$ | $\begin{array}{r} 7.0 \\ -1.6 \\ -9.8 \end{array}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Icc | Power supply current | $\begin{aligned} & \text { VDIFF }=-1 \mathrm{~V} \text {, } \\ & \text { louT }=\text { Logical " } 0 \text { " } \\ & \text { VDIFF }=-0.5 \mathrm{~V} \text {, } \end{aligned}$ | $\begin{gathered} V_{C M}=15 \mathrm{~V} \\ V_{C M}=-15 \mathrm{~V} \\ V_{C M}=0 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & 3.9 \\ & 9.2 \\ & 6.5 \end{aligned}$ | $\begin{gathered} \hline 6.0 \\ 14.0 \\ 10.2 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| VOH <br> VOL | Logical "1" output voltage Logical "0" output voltage | $\begin{aligned} & \text { IOUT }=-400 \mu A, V_{\text {DIFF }}=1 V \\ & \text { IOUT }=+16 m A, V_{\text {DIFF }}=-1 V \end{aligned}$ |  | $\begin{gathered} 2.5 \\ 0 \end{gathered}$ | $\begin{gathered} 4.0 \\ 0.22 \end{gathered}$ | $\begin{aligned} & 5.5 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \mathrm{V}_{\mathrm{SH}} \\ & \mathrm{~V}_{\mathrm{SL}} \end{aligned}$ | Logical " 1 " strobe input voltage Logical " 0 " strobe input voltage | $\begin{aligned} & \text { IOUT }=+16 \mathrm{~mA}, \text { V OUT } \leq 0.4 \mathrm{~V}, \mathrm{~V}_{\text {DIFF }}=-3 \mathrm{~V} \\ & \text { IOUT }=-400 \mu \mathrm{~A}, \mathrm{~V}_{\text {OUT }} \geq 2.5 \mathrm{~V}, \mathrm{~V}_{\text {DIFF }}=-3 \mathrm{~V} \end{aligned}$ |  | 2.1 |  | 0.9 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \text { ISH } \\ & \text { ISL } \end{aligned}$ | Logical "1" strobe input current Logical " 0 " strobe input current | $\begin{aligned} & V_{\text {STROBE }}=5.5 \mathrm{~V}, \mathrm{~V}_{\text {DIFF }}=3 \mathrm{~V} \\ & V_{\text {STROBE }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {DIFF }}=-3 \mathrm{~V} \end{aligned}$ |  |  | $\begin{array}{r} 0.01 \\ -1.0 \end{array}$ | $\begin{gathered} 5.0 \\ -1.4 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| Isc | Output short circuit current | $\mathrm{IOUT}=0 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=5.5 \mathrm{~V}, \mathrm{~V}_{\text {STROBE }}=0 \mathrm{~V}$ |  | -2.8 | -4.5 | -6.7 | mA |

NOTES

1. These specifications apply for $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 5.5 \mathrm{~V},-15 \mathrm{~V} \leq \mathrm{V}_{C M} \leq 15 \mathrm{~V}$ and $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq$ $+125^{\circ} \mathrm{C}$ for the DS7820A or $0^{\circ} \mathrm{C} \leq T_{A} \leq+70^{\circ} \mathrm{C}$ for the DS8820A unless otherwise specified. Typical values given are for $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ unless stated differently,
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
3. Only one output at a time should be shorted.
4. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | DS7820A/DS8820A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| tPDO | Propagation delay, differential input to "0" output |  |  |  | 30 | 45 | ns |
| tpD1 | Propagation delay, differential input to "1" output |  |  | 27 | 40 | ns |
| tpDo | Propagation delay, strobe input to "0" output |  |  | 16 | 25 | ns |
| tPD1 | Propagation delay, strobe input to "1" output |  |  | 18 | 30 | ns |

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## AC TEST CIRCUIT


*Includes Jig and Probe

VOLTAGE WAVEFORM

$A=$ Differential input to " 0 " output
$B=$ Differential input to " 1 " output
$C=$ Strobe input to " 0 " output
$D=$ Strobe input to " 1 " output

## TYPICAL APPLICATIONS



## DESCRIPTION

The DS7830/DS8830 is a dual differential line driver that also performs the dual fourinput NAND or dual four-input AND function.
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of $50 \Omega$ to $500 \Omega$. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

## FEATURES

- Single 5 volt power supply
- High speed
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- Short circuit protection
- DS7830 Mil std 883A,B,C available

PIN CONFIGURATION


EQUIVALENT SCHEMATIC


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| VCC | 7.0 | V |
| Input voltage | 5.5 | V |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| DS7830 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| DS8830 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C} V_{C C}=5 \mathrm{~V}$ unless otherwise specified. 1,2

| PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Logical " 1 " input voltage Logical " 0 " input voltage |  | 2.0 |  | 0.8 | $\bar{v}$ |
| Logical "1" output voltage Logical "1" output voltage Logical " 0 " output voltage Logical " 0 " output voltage Logical " 1 " input current | $\begin{array}{ll} \hline V_{\text {IN }}=0.8 \mathrm{~V} & \text { IOUT }=-0.8 \mathrm{~mA} \\ V_{\text {I }}=0.8 \mathrm{~V} & \text { IOUT }=-40 \mathrm{~mA} \\ V_{I N}=2.0 \mathrm{~V} & \text { IOUT }=+32 \mathrm{~mA} \\ V_{\text {IN }}=2.0 \mathrm{~V} & \text { IOUT }=+40 \mathrm{~mA} \\ V_{\text {IN }}=+2.4 \mathrm{~V} & \end{array}$ | $\begin{aligned} & 2.4 \\ & 18 \end{aligned}$ | $\begin{gathered} 2.9 \\ 0.2 \\ 0.22 \end{gathered}$ | $\begin{aligned} & 0.4 \\ & 0.5 \\ & 120 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Logical " 1 " input current Logical " 0 " input current | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}=0.4 \mathrm{~V} \end{aligned}$ |  |  | $\begin{gathered} 2 \\ 4.8 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Output short circuit current ${ }^{2}$ Supply current | $\begin{aligned} & \hline \mathrm{VCC}=5.0 \mathrm{~V} \\ & \mathrm{VCC}=5.0 \mathrm{~V} \quad \mathrm{~V}_{\mathrm{IN}}=5.0 \mathrm{~V} \\ & \text { (Each driver) } \\ & \hline \end{aligned}$ | -40 | $\begin{gathered} -100 \\ 11 \end{gathered}$ | $\begin{gathered} -120 \\ 18 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ & \text { See Figure } 1 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 8 \\ 11 \\ 8 \\ 5 \end{gathered}$ | $\begin{gathered} 12 \\ 18 \\ 12 \\ 8 \end{gathered}$ | ns ns ns ns |
| Differential delay $\mathrm{t}_{1}$ Differential delay $\mathrm{t}_{2}$ | Load, $100 \Omega$ and 5000 pF See Figure 2 |  | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | $\begin{aligned} & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |

## notes

1. Specifications apply for DS7830-55 ${ }^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V} \pm 10 \%, \mathrm{DS} 88300^{\circ} \mathrm{C}$
$\leq T_{A} \leq 70^{\circ} \mathrm{C}, \mathrm{V}_{C C}=+5 \mathrm{~V} \pm 5 \%$ unless otherwise specified.
2. Applies for $T_{A}=+125^{\circ} \mathrm{C}$, only one output at a time to be shorted.

## AC TEST CIRCUIT



SWITCHING TIME WAVEFORMS



## TYPICAL APPLICATION


$\dagger$ Exact value depends on line length
$\ddagger \mathrm{V}_{\mathrm{CC}}$ is 4.5 V to 5.5 V for the DS7820 and DS7830
*Optional to control response time

## DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS232C and CCITT Recommendation V.24.

## FEATURES

- Current limited output: $\pm 10 \mathrm{~mA}$ Typ
- Power-off source impedance: $300 \Omega$ Min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible


## PIN CONFIGURATION



CIRCUIT SCHEMATIC


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage V+ | +15 | V |
| V- | -15 | V |
| Input voltage (VIN) | $-15 \leq \mathrm{V}_{\text {IN }} \leq 7.0$ | V |
| Output voltage | $\pm 15$ | V |
| Power dissipation: | 1000 | mW |
| F package | 800 | mW |
| N package | 0 to +75 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $\mathrm{V}+=+9.0 \mathrm{~V} \pm 1 \%, \mathrm{~V}-=-9.0 \mathrm{~V} \pm 1 \%, \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$
unless otherwise specified.
All typicals are for $\mathrm{V}+=9.0 \mathrm{~V}, \mathrm{~V}-=-9.0 \mathrm{~V}$, and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.*

| PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Logic " 0 " input current Logic "1" input current | $\begin{aligned} & V_{\text {IN }}=0 V \\ & V_{\text {IN }}=+5.0 \mathrm{~V} \end{aligned}$ |  | $\begin{array}{r} -1.0 \\ .005 \end{array}$ | $\begin{aligned} & -1.6 \\ & 10.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| High level output voltage |  $\mathrm{V}+=9.0 \mathrm{~V}$ <br> $\mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega$ $\mathrm{V}-=-9.0 \mathrm{~V}$ <br> $\mathrm{~V}_{\mathrm{IN}}=0.8 \mathrm{~V}$ $\mathrm{~V}+=13.2 \mathrm{~V}$ <br>  $\mathrm{~V}-=-13.2 \mathrm{~V}$ | $\begin{aligned} & 6.0 \\ & 9.0 \end{aligned}$ | $\begin{gathered} 7.0 \\ 10.5 \end{gathered}$ |  | $\begin{aligned} & V \\ & V \end{aligned}$ |
| Low level output voltage | $\begin{array}{ll}  & \mathrm{V}+=9.0 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega & \mathrm{~V}-=-9.0 \mathrm{~V} \\ \mathrm{VIN}=1.9 \mathrm{~V} & \mathrm{~V}+=13.2 \mathrm{~V} \\ & \mathrm{~V}-=-13.2 \mathrm{~V} \end{array}$ | $\begin{aligned} & -6.0 \\ & -9.0 \end{aligned}$ | $\begin{gathered} -6.8 \\ -10.5 \end{gathered}$ |  | $\begin{aligned} & V \\ & v \end{aligned}$ |
| High level output Short-circuit current Low level output Short-circuit current Output resistance | $\begin{aligned} & \hline \text { VOUT }=0 \mathrm{~V} \\ & \text { VIN }=0.8 \mathrm{~V} \\ & \text { VOUT }=0 \mathrm{~V} \\ & \text { VIN }=1.9 \mathrm{~V} \\ & \mathrm{~V}+=\mathrm{V}-=0 \mathrm{~V} \\ & \text { VOUT }= \pm 2 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{array}{r} -6.0 \\ 6.0 \\ 300 \end{array}$ | $\begin{array}{r} -10.0 \\ 10.0 \end{array}$ | $\begin{array}{r} -12.0 \\ 12.0 \end{array}$ | $\begin{gathered} \mathrm{mA} \\ \mathrm{~mA} \\ \Omega \end{gathered}$ |
| Positive supply current (output open) | $\begin{array}{ll} \mathrm{V} \text { IN }=1.9 \mathrm{~V} & \mathrm{~V}+=12 \mathrm{~V}, \mathrm{~V}-=-12 \mathrm{~V} \\ & \mathrm{~V}+=15 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V} \end{array}$ |  | $\begin{aligned} & 15.0 \\ & 19.0 \\ & 25.0 \end{aligned}$ | $\begin{aligned} & 20.0 \\ & 25.0 \\ & 34.0 \\ & \hline \end{aligned}$ | mA <br> mA <br> mA |
|  |  $\mathrm{V}+=9.0 \mathrm{~V}, \mathrm{~V}-=-9.0 \mathrm{~V}$ <br> $\mathrm{~V} \mathbb{N}$ $=0.8 \mathrm{~V} \quad \mathrm{~V}+=12 \mathrm{~V}, \mathrm{~V}-=-12 \mathrm{~V}, \mathrm{~V}^{2} \mathrm{~V}$ |  | $\begin{aligned} & 4.5 \\ & 5.5 \\ & 8.0 \end{aligned}$ | $\begin{gathered} 6.0 \\ 7.0 \\ 12.0 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Negative supply current (output open) |  |  | $\begin{aligned} & \hline-13.0 \\ & -18.0 \\ & -25.0 \end{aligned}$ | $\begin{aligned} & -17.0 \\ & -23.0 \\ & -34.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | $\begin{array}{ll}  & \mathrm{V}+=9.0 \mathrm{~V}, \mathrm{~V}-=-9.0 \mathrm{~V} \\ \mathrm{~V} \mathrm{IN}=0.8 \mathrm{~V} & \mathrm{~V}+=12 \mathrm{~V}, \mathrm{~V}-=-12 \mathrm{~V} \\ & \mathrm{~V}+=15 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V} \end{array}$ |  | $\begin{gathered} -1 \\ -1 \\ -.01 \end{gathered}$ | $\begin{aligned} & -15 \\ & -15 \\ & -2.5 \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ mA |
| Power dissipation <br> Propagation delay to " 1 " ( $t_{p d 1}$ ) <br> Propagation delay to " 0 " ( $t_{p d 0}$ ) <br> Rise time ( $\mathrm{t}_{\mathrm{r}}$ ) <br> Fall time ( $\mathrm{t}_{\mathrm{f}}$ ) | $\begin{aligned} & \mathrm{V}+=9.0 \mathrm{~V}, \mathrm{~V}-=-9.0 \mathrm{~V} \\ & \mathrm{~V}+=12 \mathrm{~V}, \mathrm{~V}-=-12 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ |  | 252 444 275 70 75 40 | 333 576 350 175 100 75 | mW <br> mW <br> ns <br> ns <br> ns <br> ns |

NOTE
*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

TYPICAL PERFORMANCE CHARACTERISTICS


AC LOAD CIRCUIT


NOTE
${ }^{*} \mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.

## SWITCHING WAVEFORMS




## APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$
\mathrm{C}=\operatorname{Isc}(\Delta \mathrm{T} / \Delta \mathrm{V})
$$

where $C$ is the required capacitor, ISC is the short circuit current value, and $\Delta \mathrm{V} / \Delta \mathrm{T}$ is the slew rate.

RS232C specifies that the output slew rate must not exceed 30 V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

TYPICAL APPLICATIONS
DTL/TTL-TO-MOS TRANSLATOR


DTL/TTL-TO-RTL TRANSLATOR


## DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

## FEATURES

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand $\pm 30 \mathrm{~V}$

PIN CONFIGURATION


## EQUIVALENT SCHEMATIC



MC1489: $R_{F}=10 k$
MC1489A: $\mathrm{RF}_{\mathrm{F}}=2 \mathrm{k}$

AC TEST CIRCUIT


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Power supply voltage | 10 | V |
| Input voltage range | $\pm 30$ | V |
| Output load current | 20 | mA |
| Power dissipation: |  | W |
| F package | 800 | mW |
| N package | 0 to +75 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## VOLTAGE WAVEFORMS

DC ELECTRICAL CHARACTERISTICS
$V_{C C}=5.0 \mathrm{~V} \pm 1 \%, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+75^{\circ} \mathrm{C}$ unless otherwise specified. 1,2

| PARAMETER | TEST CONDITIONS | MC1489 |  |  | MC1489A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input high threshold voltage Input low threshold voltage | $\begin{gathered} T_{A}=25^{\circ} \mathrm{C}, V_{\text {OUT }} \leq 0.45 \mathrm{~V}, \\ \text { IOUT }=10 \mathrm{~mA} \end{gathered}$ | 1.0 |  | 1.5 | 1.75 |  | 2.25 | v <br> V <br> mA |
|  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{~V}_{\text {OUT }} \leq 2.5 \mathrm{~V}, \\ \text { IOUT }=-0.5 \mathrm{~mA} \end{gathered}$ | 0.75 |  | 1.25 | 0.75 |  | 1.25 |  |
|  | $\begin{aligned} & V_{\text {IN }}=+25 \mathrm{~V} \\ & V_{\text {IN }}=-25 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & +3.6 \\ & -3.6 \end{aligned}$ | $\begin{aligned} & +5.6 \\ & -5.6 \end{aligned}$ | $\begin{aligned} & +8.3 \\ & -8.3 \end{aligned}$ | $\begin{aligned} & +3.6 \\ & -3.6 \end{aligned}$ | $\begin{aligned} & +5.6 \\ & -5.6 \end{aligned}$ | $\begin{aligned} & +8.3 \\ & -8.3 \end{aligned}$ |  |
| Input current | $\begin{aligned} & V_{\text {IN }}=+3 V \\ & V_{\text {IN }}=-3 V \end{aligned}$ | $\begin{array}{r} +0.43 \\ -0.43 \\ \hline \end{array}$ | $\begin{array}{r} +0.53 \\ -0.53 \\ \hline \end{array}$ |  | $\begin{array}{r} +0.43 \\ -0.43 \\ \hline \end{array}$ | $\begin{array}{r} +0.53 \\ -0.53 \\ \hline \end{array}$ |  | mA |
| Output high voltage Output low voltage | $\begin{aligned} \mathrm{V}_{\text {IN }} & =0.75 \mathrm{~V}, \text { Iout }=-0.5 \mathrm{~mA} \\ \text { Input } & =\text { Open, } \text { Iout }=-0.5 \mathrm{~mA} \\ \mathrm{~V}_{\text {IN }} & =3.0 \mathrm{~V}, \text { Iout }=10 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 2.6 \\ & 2.6 \end{aligned}$ | $\begin{gathered} \hline 3.8 \\ 3.8 \\ 0.33 \end{gathered}$ | $\begin{gathered} \hline 5.0 \\ 5.0 \\ 0.45 \\ \hline \end{gathered}$ | $\begin{aligned} & 2.6 \\ & 2.6 \end{aligned}$ | $\begin{gathered} \hline 3.8 \\ 3.8 \\ 0.33 \\ \hline \end{gathered}$ | $\begin{gathered} 5.0 \\ 5.0 \\ 0.45 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Output short circuit current Supply current | $\begin{aligned} & \mathrm{V}_{\text {IN }}=0.75 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}=5.0 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 3.0 \\ & 20 \end{aligned}$ | 26 |  | $\begin{aligned} & 3.0 \\ & 20 \\ & \hline \end{aligned}$ | 26 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Power dissipation | $\mathrm{V}_{\text {IN }}=5.0 \mathrm{~V}$ |  | 100 | 130 |  | 100 | 130 | mW |

## NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is
defined as current into the referenced pin.
2. These specifications apply for response control pin =open.

AC ELECTRICAL CHARACTERISTICS $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \pm 1 \%, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified. 1,2

| PARAMETER | TEST CONDITIONS | MC1489 |  |  | MC1489A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input to output "high" | $\mathrm{R}_{\mathrm{L}}=3.9 \mathrm{k} \Omega$ ( AC test circuit) |  | 25 | 85 |  | 25 | 85 | ns |
| Propagation delay ( $\mathrm{t}_{\mathrm{pd} 1}$ ) <br> Input to output "low" <br> Propagation delay (tpdo) | $\mathrm{RL}=390 \Omega$ ( AC test circuit) |  |  |  |  | 20 | 50 | ns |
| Output rise time Output fall time | $\mathrm{R}_{\mathrm{L}}=3.9 \mathrm{k} \Omega$ (AC test circuit) $\mathrm{R}_{\mathrm{L}}=390 \Omega$ (AC test circuit) <br> $\mathrm{R}_{\mathrm{L}}=390 \Omega$ (AC test circuit) |  | $\begin{gathered} 110 \\ 9 \end{gathered}$ | $\begin{aligned} & 175 \\ & 20 \end{aligned}$ |  | $\begin{gathered} 110 \\ 9 \end{gathered}$ | $\begin{aligned} & 175 \\ & 20 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |

notes

1. Voltage values shown are with respect to network ground terminal. Positive current is
defined as current into the referenced pin.
2. These specifications apply for response control pin $=$ open.

TYPICAL APPLICATIONS


## DESCRIPTION

The UDN 5711 series of dual peripheral drivers have high voltage ( 80 V ) and high current ( 300 mA ) NPN output transistors. In addition an overshoot clamp diode is provided for each output collector for use when switching inductive loads.
A choice of AND, NAND, OR and NOR logic functions comprise the four device types in the series.
In use care must be taken to insure that the absolute maximum junction temperature rating is not exceeded due to excessive power dissipation; particularly when switching capacitive or inductive loads at high frequencies.

## FEATURES

- Four logic functions
- DTL/TTL/PMOS/CMOS compatible inputs
- Low input current loading
- 80V output breakdown


## APPLICATIONS

- Relay drivers
- Lamp drivers
- LED drivers
- High current triac trigger


## PIN CONFIGURATIONS


$\qquad$
DUAL NAND DRIVER UDN 5712


DUAL OR DRIVER UDN 5713


DUAL NOR DRIVER UDN 5714


## BLOCK DIAGRAMS




## EQUIVALENT CIRCUIT



## EQUIVALENT CIRCUIT (Cont'd)



ABSOLUTE MAXIMUM RATINGS at $25^{\circ} \mathrm{C}$ unless otherwise stated.

| PARAMETER |  | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| Vcc | Supply voltage |  |  |
|  | Continuous | 7 | V |
|  | Momentary (1 second) | 15 | V |
| VIN | Input voltage | 30 | V |
| Vout | Output voltage (off state) | 80 | V |
| IOUT | Output current | 600 | mA |
| Vs | Suppression diode reverse voltage | 80 | V |
| Is | Suppression diode forward current | 600 | mA |
| PD | Power dissipation* | 750 | mW |
| TA | Operating temperature range | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| Tstg | Storage temperature range | $-65 \text { to } 150$ | ${ }^{\circ} \mathrm{C}$ |
|  | Lead soldering temperature (10 seconds) | $300$ | ${ }^{\circ} \mathrm{C}$ |

note
${ }^{*}$ The maximum junction is $150^{\circ} \mathrm{C}$. Derate at $162^{\circ} \mathrm{C}$ /watt above $25^{\circ} \mathrm{C}$.

DC ELECTRICAL CHARACTERISTICS $0^{\circ} \mathrm{C} \leq T_{A} \leq 85^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage range |  |  | 4.75 | 5.00 | 5.25 | V |
| $\begin{aligned} & V_{I H} \\ & V_{I L} \end{aligned}$ | Logical "1" input voltage Logical "0" input voltage | $\begin{aligned} & V_{C C}=4.75 \mathrm{~V} \\ & V_{c c}=4.75 \mathrm{~V} \end{aligned}$ | 2.0 |  | 0.8 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{1}$ | Input clamp voltage | $\mathrm{V}_{\text {CC }}=4.75 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{1}=-12 \mathrm{~mA}$ |  | -1.2 | -1.5 | V |
| $\begin{aligned} & \mathrm{IH} \\ & \mathrm{IH} \end{aligned}$ | ```Logical "1" input current except stobe Logical "1" input current at strobe``` | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=30 \mathrm{~V} \\ \mathrm{~V}_{\text {strobe }}=0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {strobe }}=30 \mathrm{~V} \\ \mathrm{~V}_{\text {N }}=0 \mathrm{~V} \end{gathered}$ |  |  | 10 20 | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| IL IIL | Logical " 0 " input current except strobe Logical " 0 " input current at strobe | $\begin{gathered} \mathrm{V}_{C C}=5.25 \mathrm{~V}, \mathrm{~V}_{1 \mathrm{~N}}=0.4 \mathrm{~V} \\ \mathrm{~V}_{\text {strobe }}=30 \mathrm{~V} \\ \mathrm{~V}_{C C}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {strobe }}=0.4 \mathrm{~V} \\ \mathrm{~V}_{\text {IN }}=30 \mathrm{~V} \end{gathered}$ |  | $\begin{array}{r} -50 \\ -100 \\ \hline \end{array}$ | $\begin{aligned} & -100 \\ & -200 \end{aligned}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| Iout | Output current | UDN $5711 / 5713-\mathrm{V}_{\mathrm{IN}}=0.8 \mathrm{~V}$ UDN 5712/5714- $\mathrm{V}_{\mathrm{IN}}=2.0 \mathrm{~V}$ |  |  | 300 | mA |
| IOH | Output leakage current | $\begin{gathered} \hline \mathrm{V}_{\text {IN }}=2.0 \mathrm{~V}(\text { UDN } 5711 / 5713) \\ \mathrm{V}_{\text {IN }}=0.8 \mathrm{~V}(\text { UDN } 5712 / 5714) \\ \mathrm{V}_{\mathrm{OH}}=80 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=\text { open } \end{gathered}$ |  |  | $\begin{aligned} & 100 \\ & 100 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| VoL | Output low voltage | $\begin{gathered} \hline \mathrm{V}_{\text {IN }}=0.8 \mathrm{~V}(\mathrm{UDN} 5711 / 5713) \\ \mathrm{V}_{\mathrm{IN}}=2.0 \mathrm{~V}(\mathrm{UDN} 5712 / 5714) \\ \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{IOL}=150 \mathrm{~mA} \\ \mathrm{loL}=300 \mathrm{~mA} \end{gathered}$ |  | $\begin{aligned} & 0.35 \\ & 0.50 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.50 \\ & 0.70 \end{aligned}$ | $\begin{aligned} & \text { v } \\ & \text { v } \end{aligned}$ |
| ILD | Diode leakage current | $\begin{aligned} V_{I N} & =0 V(U D N 5711 / 5713) \\ V_{I N} & =5 \mathrm{~V}(U D N 5712 / 5714) \\ V_{C C} & =5 \mathrm{~V}, V_{L D}=80 \mathrm{~V}, \mathrm{~T}_{A}=25^{\circ} \mathrm{C} \end{aligned}$ |  |  | 200 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {FD }}$ | Diode forward voltage | $\mathrm{I}_{\text {FD }}=300 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.5 | 1.75 | V |
| Icch | Supply current with outputs high | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \text { UDN } 5711 \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{~V} \\ \text { UDN } 5712 \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V} \\ \text { UDN } 5713 \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{~V} \\ \text { UDN } 5714 \mathrm{~V}_{\text {IN }}=0 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} 8 \\ 12 \\ 8 \\ 12 \end{gathered}$ | $\begin{aligned} & 12 \\ & 15 \\ & 13 \\ & 15 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| ICCL | Supply current with outputs low | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \text { UDN } 5711 \mathrm{~V}_{\text {IN }}=0 \mathrm{~V} \\ \text { UDN } 5712 \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{~V} \\ \text { UDN } 5713 \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V} \\ \text { UDN } 5714 \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & 35 \\ & 40 \\ & 36 \\ & 40 \end{aligned}$ | $\begin{aligned} & 49 \\ & 53 \\ & 50 \\ & 50 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| TPLH | Propagation delay time, low-to-high output |  | $\begin{gathered} V_{S}=70 \mathrm{~V}, R_{\mathrm{L}}=465 \Omega \\ C_{L}=15 \mathrm{pF} \end{gathered}$ |  |  | 500 | ns |
| TPHL | Propagation delay time, high-to-low output | $\begin{gathered} \mathrm{V}_{\mathrm{S}}=70 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=465 \Omega \\ \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \end{gathered}$ |  |  | 750 | ns |

## 

## TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS


## DESCRIPTION

The 75S107 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75107A. If features less than 17 ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.
The 75S107 maintains $\pm 3 \mathrm{~V}$ common mode voltage range, 7.5 mV input offset voltage and $5 \mu \mathrm{~A}$ offset current. It also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

FEATURES

- Functionally equivalent and pin compatible to SN75107A
- 17 ns maximum guaranteed propagation delay
- $20 \mu \mathrm{~A}$ maximum input bias current
- STTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages


## APPLICATIONS

- MOS memory sense amp
- A/D conversion
- High speed line receiver

PIN CONFIGURATION


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Positive supply voltage (V+) | +7 | V |
| Negative supply voltage (V-) | -7 | V |
| Differential input voltage | $\pm 6$ | V |
| Common mode input voltage | $\pm 5$ | V |
| Strobe/gate input voltage | +5.5 | V |
| Power dissipation | 600 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

EQUIVALENT SCHEMATIC


ELECTRICAL CHARACTERISTICS $\mathrm{T}_{\mathrm{A}}=0$ to $+70^{\circ} \mathrm{C}, \mathrm{V}+=+5.00, \mathrm{~V}-=-5.00$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 75S107 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| AMPLIFIE | INPUT Input offset voltage |  | $\mathrm{V}+=4.75, \mathrm{~V}-=-4.75$ |  |  | 25 | mV |
|  | Input bias current @ $25^{\circ} \mathrm{C}$ over temp. range | $\begin{aligned} & \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25 \end{aligned}$ |  | 7.5 | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
|  | Input offset current @ $25^{\circ} \mathrm{C}$ over temp. range | $\begin{aligned} & \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25 \end{aligned}$ | - | 1.0 | $\begin{gathered} 5 \\ 12 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
|  | Input common mode voltage range Input resistance Input capacitance | $\mathrm{V}+=4.75, \mathrm{~V}-=-4.75$ | $\pm 3$ | $\begin{aligned} & 4 \\ & 3 \end{aligned}$ | 6 | $\begin{gathered} \mathrm{V} \\ \mathrm{k} \Omega \\ \mathrm{pF} \end{gathered}$ |
|  | Voltage gain |  |  | 5 |  | $\mathrm{V} / \mathrm{mV}$ |
| $\begin{aligned} & \text { SCHOTTI } \\ & I_{I_{H}} \end{aligned}$ | GATE/OUTPUT CHARACTERISTICS <br> High level input current into 1 G or 2G strobe | $\begin{gathered} \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V}_{I H}=2.7 \mathrm{~V} \\ \mathrm{~V}_{I H}=5.5 \mathrm{~V} \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 50 \\ 1 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| $\mathrm{l} / \mathrm{H}$ | High level input current into common strobe S | $\begin{gathered} \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V}_{\mathrm{IH}}=2.7 \mathrm{~V} \\ \mathrm{~V}_{I H}=5.5 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 100 \\ 2 \\ \hline \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| IIL IIL | Low level input current into 1G or 2G <br> Low level input current into common strobe $S$ | $\begin{gathered} \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V} \text { IL }=0.5 \mathrm{~V} \\ \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25 \\ \mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V} \end{gathered}$ |  |  | $\begin{aligned} & -2.0 \\ & -4.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| VOH | High level output voltage | $\begin{gathered} \hline \mathrm{V}+=4.75 \mathrm{~V}, \mathrm{~V}_{(\mathrm{S})}=2.0 \mathrm{~V} \\ \mathrm{~V}-=-4.75 \mathrm{~V} \\ \mathrm{I}_{\text {LOAD }}=-1 \mathrm{~mA} \\ \hline \end{gathered}$ | 2.7 | 3.4 |  | V |
| VoL | Low level output voltage | $\begin{aligned} V+ & =4.75 \\ V- & =-4.75 \\ I_{\text {LOAD }} & =20 \mathrm{~mA} \\ V_{1(S)} & =2.0 \mathrm{~V} \end{aligned}$ |  |  | 0.5 | V |
| POWER SUPPLY REQUIREMENTS Supply voltage |  |  | $\begin{array}{r} 4.75 \\ -4.75 \\ \hline \end{array}$ | $\begin{array}{r} 5.00 \\ -5.00 \\ \hline \end{array}$ | $\begin{array}{r} 5.25 \\ -5.25 \\ \hline \end{array}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \text { Icc+ } \\ & \text { Icc- } \end{aligned}$ | Supply current | $\begin{gathered} \mathrm{V}+=5.25 \mathrm{~V} \\ \mathrm{~V}-=-5.25 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{gathered} 20 \\ -11 \end{gathered}$ | $\begin{gathered} 30 \\ -15 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| los | Short circuit output current | $\begin{aligned} & \mathrm{V}+=+5.25 \\ & \mathrm{~V}-=-5.25 \end{aligned}$ | -40 |  | -100 | mA |
| LARGE S TpLH (D) | NAL SWITCHING SPEED <br> Low to high propagation delay from amp inputs to output 1 | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 p F \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 12 | 17 | ns |
| TpHL (D) | High to low propagation delay from amps inputs to output1 | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 \mathrm{pF} \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 9 | 13 | ns |
| TpLH (S) | Low to high propagation delay from strobes input to output2 | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 4.5 | 6 | ns |
| TpHL (S) | High to low propagation delay strobe input to output2 | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 3.0 | 4.5 | ns |
| Maximum operating frequency |  | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ | 40 | 55 |  | MHz |

NOTES

1. Response time measured from 0 V point of $\pm 100 \mathrm{mVP}$-p 10 MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5 V point to input to 1.5 V point of output.
3. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the 1.5 V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The 75S108 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75108N. It features less than 17 ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75 S 108 maintains $\pm 3 \mathrm{~V}$ common mode voltage range, 7.5 mV input offset voltage and $5 \mu$ A offset current. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

## FEATURES

- Functionally equivalent and pin compatible to SN75108A
- 17ns maximum guaranteed propagation delay
- $20 \mu \mathrm{~A}$ maximum input bias current
- TTL compatible strobes and outputs
- Open collector outputs
- Large common mode input voltage range
- Operates from standard supply voltages


## APPLICATIONS

- High speed line receiver
- MOS memory sense amp
- A/D conversion

PIN CONFIGURATION


EQUIVALENT SCHEMATIC


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Positive supply voltage (V+) | +7 | V |
| Negative supply voltage (V-) | -7 | V |
| Differential input voltage | $\pm 6$ | V |
| Common mode input voltage | $\pm 5$ | V |
| Strobe gate input voltage | +5.5 | V |
| Power dissipation | 600 | mW |
| Operating temperature range | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering 60 sec ) | +300 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $T_{A}=0$ to $70^{\circ} \mathrm{C}, \mathrm{V}+=+5.00, \mathrm{~V}-=-5.00$ unless otherwise specified:

| PARAMETER | TEST CONDITIONS | $75 S 108$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| AMPLIFIER INPUT Input offset voltage | $\mathrm{V}+=4.75, \mathrm{~V}-=-4.75$ |  |  | 25 | mV |
| Input bias current @ $25^{\circ} \mathrm{C}$ over temp range | $\begin{aligned} & \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25 \end{aligned}$ |  | 7.5 | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input offset current @ $25^{\circ} \mathrm{C}$ over temp range | $\begin{aligned} & \mathrm{V}+=5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}+=5.25, \mathrm{~V}-=-5.25 \end{aligned}$ |  | 1.0 | $\begin{gathered} 5 \\ 12 \end{gathered}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| Input common mode voltage range Input resistance Input capacitance | $\mathrm{V}+=4.75, \mathrm{~V}-=-4.75$ | $\pm 3$ | $\begin{aligned} & 4 \\ & 3 \end{aligned}$ | $\begin{gathered} \pm 3 \\ 6 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{k} \Omega \\ \mathrm{pF} \end{gathered}$ |
| Voltage gain |  |  | 5 |  | $\mathrm{V} / \mathrm{mV}$ |
| SCHOTTKY GATE/OUTPUT CHARACTERISTICS IIH High level input current into 1G or 2G strobe | $\begin{gathered} V+=5.25, V-=-5.25 \\ V_{I H}=2.7 \mathrm{~V} \\ V_{I H}=5.5 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 50 \\ 1 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| l\|H High level input current into common strobe $S$ | $\begin{gathered} V+=5.25, V-=-5.25 \\ V_{I H}=2.7 \mathrm{~V} \\ V_{I H}=5.5 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 100 \\ 2 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| IL Low level input current into $1 G$ or 2 G <br> IIL Low level input current into common strobe S | $\begin{aligned} & \mathrm{V}+= 5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V} \\ & \mathrm{~V}+= 5.25, \mathrm{~V}-=-5.25 \\ & \mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & -2.0 \\ & -4.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| VOL Low level output voltage | $\begin{gathered} V+=4.75, V_{1}(S)=2.0 \mathrm{~V} \\ V-=-4.75 \\ I_{\text {LOAD }}=20 \mathrm{~mA} \end{gathered}$ |  |  | 0.5 | V |
| loh High level output current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}+=5.25 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=-5.25 \mathrm{~V} \\ \mathrm{VOH}_{\mathrm{OH}}=5.25 \mathrm{~V} \end{gathered}$ |  |  | 250 | $\mu \mathrm{A}$ |
| POWER SUPPLY REQUIREMENTS <br> Supply voltage <br> V+ <br> V- |  | $\begin{array}{r} 4.75 \\ -4.75 \\ \hline \end{array}$ | $\begin{array}{r} 5.00 \\ -5.00 \\ \hline \end{array}$ | $\begin{array}{r} 5.25 \\ -5.25 \\ \hline \end{array}$ | $\begin{aligned} & V \\ & V \end{aligned}$ |
| Supply current | $\begin{gathered} \mathrm{V}+=5.25 \mathrm{~V} \\ \mathrm{~V}-=-5.25 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  |  |  |  |
| $\begin{aligned} & \text { Icct } \\ & \text { Icc- } \end{aligned}$ |  |  | $\begin{array}{r} 20 \\ -11 \\ \hline \end{array}$ | $\begin{array}{r} 30 \\ -15 \\ \hline \end{array}$ | $\begin{array}{r} \mathrm{mA} \\ \mathrm{~mA} \\ \hline \end{array}$ |
| LARGE SIGNAL SWITCHING SPEED TpLH (D) Low to high propagation delay from amp inputs to output1 | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 p F \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 12 | 17 | ns |
| $T_{p} H L$ (D) High to low propagation delay from amp inputs to output1 | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 p F \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 9 | 13 | ns |
| $\mathrm{T}_{\mathrm{p}} \mathrm{LH}(\mathrm{S})$ Low to high propagation delay from strobes input to output ${ }^{2}$ | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 \mathrm{pF} \\ T_{A} 25^{\circ} \mathrm{C} \end{gathered}$ |  | 6 | 10 | ns |
| $\mathrm{T}_{\mathrm{p}} \mathrm{HL}$ (S) High to low propagation delay strobe input to output2 | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 \mathrm{pF} \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ |  | 5 | 8 | ns |
| Maximum operating frequency | $\begin{gathered} R_{L}=280 \Omega C_{L}=15 p F \\ T_{A}=25^{\circ} \mathrm{C} \end{gathered}$ | 25 | 35 |  | MHz |

## NOTES:

1. Response time measured from $O V$ point of $\pm 100 \mathrm{mVp}-\mathrm{P} 10 \mathrm{MHz}$ square wave to the 1.5 point of the output.
2. Response time measured from 1.5 V point of input to 1.5 V point of output.
3. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the 1.5 V point of the output.

## TYPICAL PERFORMANCE CHARACTERISTICS



OUTPUT VOLTAGE vs AMBIENT TEMPERATURE


RESPONSE TIME vs TEMPERATURE


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE


INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES


INPUT BIAS CURRENT vs
AMBIENT TEMPERATURE


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES


## DESCRIPTION

Series 55450B/75450B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. The $55450 \mathrm{~B} / 75450 \mathrm{~B}$ family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the $55450 \mathrm{~B} / 75450 \mathrm{~B}$ family is equal to that of the 75450 family and a test to ensure freedom from latch-up has been added. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55450B drivers are characterized for operation over the full military temperature range of $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$; Series 75450 B drivers are characterized for operation from $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.
The 55450B and 75450 B are unique generalpurpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage $n-p-n$ transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The $55451 \mathrm{~B} / 75451 \mathrm{~B}, 55452 \mathrm{~B} / 75452 \mathrm{~B}$, $55453 \mathrm{~B} / 75453 \mathrm{~B}$, and $55454 \mathrm{~B} / 75454 \mathrm{~B}$ are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the $\mathrm{n}-\mathrm{p}-\mathrm{n}$ output transistors.

FEATURES

- 300mA output current capability
- High voltage outputs
- No output latch up at 20 V
- High speed switching
- Circuit flexibility for varied applications
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages

TRUTH TABLE (55/75450B and 55/75451B)

| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}$ |
| :---: | :---: | :---: |
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| $H$ | $H$ | H (off state) |

TRUTH TABLE (55/75452B)

| A | B | $\mathbf{Y}$ |
| :--- | :--- | :---: |
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

TRUTH TABLE (55/75453B)

| A | B | Y |
| :---: | :---: | :---: |
| $L$ | $L$ | L (on state) |
| L | $H$ | $H$ (off state) |
| $H$ | $L$ | $H$ (off state) |
| $H$ | $H$ | $H$ (off state) |

TRUTH TABLE (55/75454B)

| A | $\mathbf{B}$ | $\mathbf{Y}$ |
| :---: | :---: | :---: |
| L | L | H (off state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | L (on state) |

## PIN CONFIGURATIONS



Pin 4 is in electrical contact with the case
ORDER PART NO.
55/75451B
55/75452B
55/75453B 55/75454B


EQUIVALENT SCHEMATICS



## EQUIVALENT SCHEMATICS



## 

ABSOLUTE MAXIMUM RATINGS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | 55450B | 75450B | 55454B 55453B 55452B 55451B | 75454B <br> 75453B <br> 75452B <br> 75451B | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage, $\mathrm{V}_{\mathrm{CC}}{ }^{1}$ | 7 | 7 | 7 | 7 | V |
| Input voltage | 5.5 | 5.5 | 5.5 | 5.5 | V |
| Interemitter voltage2 | 5.5 | 5.5 | 5.5 | 5.5 | v |
| Vcc-to-substrate voltage | 35 | 35 |  |  | V |
| Collector-to-substrate voltage | 35 | 35 |  |  | V |
| Collector-base voltage | 35 | 35 |  |  | V |
| Collector-emitter voltage 3 | 30 | 30 |  |  | V |
| Emitter-base voltage | 5 | 5 |  |  | V |
| Output voltage ${ }^{4}$ |  |  | 30 | 30 | V |
| Collector current5 | 300 | 300 |  |  | mA |
| Output current5 |  |  | 300 | 300 | mA |
| Continuous total dissipation at (or below) $25^{\circ} \mathrm{C}$ free-air temperature ${ }^{6}$ | 800 | 800 | 800 | 800 | mW |
| Operating free-air temperature range | -55 to 125 | 0 to 70 | -55 to 125 | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to 150 | -65 to 150 | -65 to 150 | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature $1 / 16$ inch from case for 60 seconds $F$ or T package | 300 | 300 | 300 | 300 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature $1 / 16$ inch from case for 10 seconds N package | 260 | 260 | 260 | 260 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transitor.
3. This value applies when the base-emitter resistance ( $R_{B E}$ ) is equal to or less than $500 \Omega$.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously; however power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above $25^{\circ} \mathrm{C}$ free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the $T$ package requires a heat sink that provides a thermal resistance from case to free-air, $\mathrm{R}_{\theta C A}$, of not more than $95^{\circ} \mathrm{C} / \mathrm{W}$.

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 55450B |  |  | 75450B |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $V_{\text {(BR) }}$ CBO | Collector-base breakdown voltage |  | $I_{C}=100 \mu A, I_{E}=0$ | 35 |  |  | 35 |  |  | V |
| $V_{\text {(BR)CER }}$ | Collector-emitter breakdown voltage | $\mathrm{IC}=100 \mu \mathrm{~A}, \mathrm{R}_{\mathrm{BE}}=500 \Omega$ | 30 |  |  | 30 |  |  | V |
| $V_{\text {(BR) EBO }}$ | Emitter-base breakdown voltage | $I_{E}=100 \mu A, I_{C}=0$ | 5 |  |  | 5 |  |  | V |
| hfe <br> hfe <br> hfe <br> hfe <br> hfe <br> hfe | Static forward current transfer ratio <br> Static forward current transfer ratio <br> Static forward current transfer ratio <br> Static forward current transfer ratio <br> Static forward current transfer ratio <br> Static forward current transfer ratio | $\begin{aligned} & \mathrm{V}_{\mathrm{CE}}=3 \mathrm{~V}, \mathrm{IC}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CE}}=3 \mathrm{~V}, \mathrm{IC}=300 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CE}}=3 \mathrm{~V}, \mathrm{IC}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CE}}=3 \mathrm{~V}, \mathrm{IC}=300 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CE}}=3 \mathrm{~V}, \mathrm{I} \mathrm{I}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CE}}=3 \mathrm{~V}, \mathrm{IC}=300 \mathrm{~mA} \end{aligned}$ | 25 <br> 30 <br> 10 <br> 15 |  |  | 25 <br> 30 <br> 20 <br> 25 |  |  |  |
| $V_{B E}$ <br> VBE | Base-emitter voltage Base-emitter voltage | $\begin{aligned} & I_{B}=10 \mathrm{~mA}, I_{C}=100 \mathrm{~mA} \\ & I_{B}=30 \mathrm{~mA}, I_{C}=300 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 0.85 \\ & 1.05 \end{aligned}$ | $\begin{aligned} & 1.2 \\ & 1.4 \end{aligned}$ |  | $\begin{aligned} & 0.85 \\ & 1.05 \end{aligned}$ | $\begin{gathered} 1 \\ 1.2 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{CE}}(\mathrm{SAT})$ <br> $V_{C E}(S A T)$ | Collector-emitter saturation voltage Collector-emitter saturation voltage | $\begin{aligned} & I_{B}=10 \mathrm{~mA}, I_{C}=100 \mathrm{~mA} \\ & I_{B}=30 \mathrm{~mA}, I_{C}=300 \mathrm{~mA} \end{aligned}$ |  | 0.25 0.5 | 0.5 0.8 |  | 0.25 0.5 | 0.4 0.7 | V V |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  |  | TEST CONDITIONS | 55450B |  |  | 75450B |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| $V_{I H}$ $V_{I L}$ | High-level input voltage Low-level input voltage |  |  | 2 |  | 0.8 | 2 |  | 0.8 | $\begin{aligned} & V \\ & V \end{aligned}$ |
| $\begin{aligned} & V_{1} \\ & V_{1} \end{aligned}$ | Input clamp voltage Input clamp voltage |  | $\begin{aligned} & V_{C C}=4.5 \mathrm{~V} \quad I_{1}=-12 \mathrm{~mA} \\ & V_{C C}=4.75 \mathrm{~V} \quad I_{1}=-12 \mathrm{~mA} \end{aligned}$ |  |  | 1.5 |  |  | 1.5 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \mathrm{VOH} \\ & \mathrm{VOH}_{\mathrm{OH}} \end{aligned}$ | High-level output voltage <br> High-level output voltage |  | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ \mathrm{IOH}_{\mathrm{OH}}=-400 \mu \mathrm{~A} \\ \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V} \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ \mathrm{IOH}_{\mathrm{OH}}=-400 \mu \mathrm{~A} \end{gathered}$ | 2.4 | 3.3 |  |  | 2.4 | 3.3 | $\mathrm{V}$ <br> V |
| VOL <br> VOL | Low-level output voltage <br> Low-level output voltage |  | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\ \mathrm{lOL}=16 \mathrm{~mA} \\ \mathrm{VCC}=4.75 \mathrm{~V} \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\ \mathrm{lOL}=16 \mathrm{~mA} \end{gathered}$ |  | 0.22 | 0.5 |  | 0.22 | 0.4 | V <br> V |
| 11 | Input current at maximum input voltage Input current at maximum input voltage | InputA <br> InputG <br> InputA <br> InputG | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \mathrm{~V}_{1}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \mathrm{~V}_{1}=5.5 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & 1 \\ & 2 \end{aligned}$ |  |  | 1 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| IH IH | High level input current High level input current | InputA InputG InputA InputG | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \mathrm{~V}_{1}=2.4 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \mathrm{~V}_{1}=2.4 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & 40 \\ & 80 \end{aligned}$ | . |  | $\begin{aligned} & 40 \\ & 80 \end{aligned}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| IIL <br> IIL | Low-level input current Low-level input current | InputA InputG InputA InputG | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V} V_{1}=0.4 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V} V_{1}=0.4 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & -1.6 \\ & -3.2 \end{aligned}$ |  |  | $\begin{aligned} & -1.6 \\ & -3.2 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \text { los } \\ & \text { los } \end{aligned}$ | Short-circuit output current ${ }^{2}$ Short-circuit output current ${ }^{2}$ |  | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V} \end{aligned}$ | -18 |  | -55 | -18 |  | -55 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \mathrm{ICCH} \\ & \mathrm{ICCH} \end{aligned}$ | Supply current, outputs high Supply current, outputs high |  | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V} V_{1}=0 \\ & V_{C C}=5.25 V V_{1}=0 \end{aligned}$ |  | 2 | 4 |  | 2 | 4 | mA mA |
| ICCL <br> ICCL | Supply current, outputs low Supply current, outputs low |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \mathrm{~V}_{1}=5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \mathrm{~V}_{\mathrm{I}}=5 \mathrm{~V} \end{aligned}$ |  | 6 | 11 |  | 6 | 11 | mA mA |

NOTES

1. Electrical characteristics over recommended operating free-air temperature range
(unless otherwise specified).
2. Not more than one output should be shorted at a time

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ unless otherwise specified.

\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|r|}{\multirow{2}{*}{PARAMETER}} \& \multirow{2}{*}{TEST CONDITIONS} \& \multicolumn{3}{|c|}{55451} \& \multicolumn{3}{|c|}{75451} \& \multirow{2}{*}{UNIT} \\
\hline \& \& \& Min \& Typ \& Max \& Min \& Typ \& Max \& \\
\hline \[
\begin{aligned}
\& \mathrm{V}_{\mathrm{IH}} \\
\& \mathrm{~V}_{\mathrm{IL}}
\end{aligned}
\] \& High-level input voltage Low-level input voltage \& \& 2 \& \& 0.8 \& 2 \& \& 0.8 \& V \\
\hline \[
\begin{aligned}
\& v_{1} \\
\& v_{1}
\end{aligned}
\] \& Input clamp voltage Input clamp voltage \& \[
\begin{aligned}
\& \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} \mathrm{I}_{1} \\
\&=-12 \mathrm{~mA} \\
\& \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V} \\
\& \hline
\end{aligned}
\] \& \& \& -1.5 \& \& \& 1.5 \& V \\
\hline \[
\begin{aligned}
\& \mathrm{IOH} \\
\& \mathrm{IOH}
\end{aligned}
\] \& High-level output current High-level output current \& \[
\begin{aligned}
\& \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=30 \mathrm{~V} \\
\& \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=30 \mathrm{~V}
\end{aligned}
\] \& \& \& 300 \& \& \& 100 \& \[
\begin{aligned}
\& \mu \mathrm{A} \\
\& \mu \mathrm{~A}
\end{aligned}
\] \\
\hline \begin{tabular}{l}
VoL \\
Vol
\end{tabular} \& \begin{tabular}{l}
Low-level output voltage \\
Low-level output voltage
\end{tabular} \&  \& \& \[
\begin{gathered}
\hline 0.25 \\
0.5
\end{gathered}
\] \& \[
\begin{aligned}
\& \hline 0.5 \\
\& 0.8
\end{aligned}
\] \& \& \[
\begin{gathered}
0.25 \\
0.5
\end{gathered}
\] \& \[
\begin{aligned}
\& 0.4 \\
\& 0.7
\end{aligned}
\] \& V

V <br>

\hline 11 \& Input current at maximum input voltage Input current at maximum input voltage \& $$
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=5.5 \mathrm{~V} \\
& \mathrm{~V}_{C C}=5.25 \mathrm{~V}, \mathrm{~V}_{1}=5.5 \mathrm{~V}
\end{aligned}
$$ \& \& \& 1 \& \& \& 1 \& \[

$$
\begin{aligned}
& \mathrm{mA} \\
& \mathrm{~mA}
\end{aligned}
$$
\] <br>

\hline $$
\begin{aligned}
& \mathrm{I}_{\mathrm{H}} \\
& \mathrm{I}_{\mathrm{H}}
\end{aligned}
$$ \& High level input current High level input current \& \[

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=2.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \mathrm{~V}_{1}=2.4 \mathrm{~V}
\end{aligned}
$$

\] \& \& \& 40 \& \& \& 40 \& \[

$$
\begin{aligned}
& \mathrm{mA} \\
& \mu \mathrm{~A}
\end{aligned}
$$
\] <br>

\hline $$
\begin{aligned}
& \text { IL } \\
& I_{1 L}
\end{aligned}
$$ \& Low level input current Low-level input current \& \[

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \mathrm{~V}_{1}=0.4 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \mathrm{~V}_{1}=0.4 \mathrm{~V}
\end{aligned}
$$

\] \& \& -1 \& -1.6 \& \& -1 \& -1.6 \& \[

$$
\begin{aligned}
& \mathrm{mA} \\
& \mathrm{~mA}
\end{aligned}
$$
\] <br>

\hline ICCH ICCH \& Supply current, outputs high Supply current, outputs high \& $$
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \mathrm{~V}_{1}=5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V} \mathrm{~V}_{1}=5 \mathrm{~V}
\end{aligned}
$$ \& \& 7 \& 11 \& \& 7 \& 11 \& \[

$$
\begin{aligned}
& \mathrm{mA} \\
& \mathrm{~mA}
\end{aligned}
$$
\] <br>

\hline ICCL ICCL \& Supply current, outputs low Supply current, outputs low \& $$
\begin{aligned}
& V_{C C}=5.5 \mathrm{~V} V_{1}=0 \\
& V_{C C}=5.25 \mathrm{~V} \mathrm{~V}_{1}=0
\end{aligned}
$$ \& \& 52 \& 65 \& \& 52 \& 65 \& \[

$$
\begin{aligned}
& \mathrm{mA} \\
& \mathrm{~mA}
\end{aligned}
$$
\] <br>

\hline
\end{tabular}

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | 55452 |  |  | 75452 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | High-level input voltage Low-level input voltage |  | 2 |  | 0.8 | 2 |  | 0.8 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \hline V_{1} \\ & V_{1} \end{aligned}$ | Input clamp voltage Input clamp voltage | $\begin{aligned} & \mathrm{VCC}_{\mathrm{CC}}=4.5 \mathrm{~V} \\|_{1}=-12 \mathrm{~mA} \\ & \mathrm{VCC}=4.75 \mathrm{~V} \quad I_{1}=-12 \mathrm{~mA} \end{aligned}$ |  |  | -1.5 |  |  | -1.5 | V |
| $\begin{aligned} & \mathrm{IOH} \\ & \mathrm{IOH} \end{aligned}$ | High-level output current High-level output current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{VOH}_{\mathrm{OH}}=30 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=30 \mathrm{~V} \end{aligned}$ |  |  | 300 |  |  | 100 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Vol <br> Vol | Low-level output voltage Low-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, 1 \mathrm{IOL}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{1 \mathrm{H}}=2 \mathrm{~V}, 1 \mathrm{IOL}=300 \mathrm{~mA} \\ & \mathrm{VCC}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{1 H}=2 \mathrm{~V}, \mathrm{IOL}=100 \mathrm{~mA} \\ & \mathrm{VCC}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{1 \mathrm{H}}=2 \mathrm{~V}, 1 \mathrm{IOL}=300 \mathrm{~mA} \\ & \hline \end{aligned}$ |  | $\begin{gathered} \hline 0.25 \\ 0.5 \end{gathered}$ | $\begin{aligned} & 0.5 \\ & 0.8 \end{aligned}$ |  | $\begin{gathered} 0.25 \\ 0.5 \\ \hline \end{gathered}$ | $\begin{aligned} & 0.4 \\ & 0.7 \\ & \hline \end{aligned}$ | V V |
| 11 | Input current at maximum input voltage Input current at maximum input voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{1}=5.5 \mathrm{~V} \end{aligned}$ |  |  | 1 |  |  | 1 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{I}_{\mathrm{H}} \\ & \mathrm{I}_{\mathrm{H}} \end{aligned}$ | High-level input current High-level input current | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=2.4 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{1}=2.4 \mathrm{~V} \end{gathered}$ |  |  | 40 |  |  | 40 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| $\begin{aligned} & I_{I L} \\ & I_{I L} \end{aligned}$ | Low-level input current Low-level input current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=0.4 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{1}=0.4 \mathrm{~V} \end{aligned}$ |  | -1 | -1.6 |  | -1 | -1.6 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \mathrm{I} \mathrm{CCH} \\ & \mathrm{ICCH} \\ & \hline \end{aligned}$ | Supply current, outputs high Supply current, outputs high | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V}, V_{1}=0 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V}, V_{1}=0 \mathrm{~V} \end{aligned}$ |  | 11 | 14 |  | 11 | 14 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| ICCL IcCL | Supply current, outputs low Supply current, outputs low | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=5 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V}, \mathrm{~V}_{1}=5 \mathrm{~V} \end{aligned}$ |  | 56 | 71 |  | 56 | 71 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | 55453 |  |  | 75453 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & V_{I H} \\ & V_{I L} \end{aligned}$ | High-level input voltage Low-level input voltage |  | 2 |  | 0.8 | 2 |  | 0.8 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & V_{1} \\ & V_{1} \end{aligned}$ | Input clamp voltage Input clamp voltage | $\begin{aligned} & \mathrm{V}_{C C}=4.5 \mathrm{~V} I_{I}=-12 \mathrm{~mA} \\ & V_{C C}=4.75 \mathrm{~V} I_{I}=-12 \mathrm{~mA} \end{aligned}$ |  |  | -1.5 |  |  | -1.5 | V |
| $\begin{aligned} & \mathrm{IOH} \\ & \mathrm{IOH} \end{aligned}$ | High-level output current High-level output current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{1 H}=2 \mathrm{~V}, \mathrm{VOH}_{\mathrm{OH}}=30 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=30 \mathrm{~V} \end{aligned}$ |  |  | 300 |  |  | 100 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Vol <br> VOL | Low-level output voltage <br> Low-level output voltage | $\begin{gathered} \mathrm{VCC}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ 1 \mathrm{OL}=100 \mathrm{~mA} \\ \mathrm{VCC}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ 10 \mathrm{~V}=300 \mathrm{~mA} \\ \mathrm{VCC}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ 10 \mathrm{CL}=100 \mathrm{~mA} \\ \mathrm{VCC}=4.75 \mathrm{~V}, \mathrm{~V} / \mathrm{IL}=0.8 \mathrm{~V} \\ 1 \mathrm{OL}=300 \mathrm{~mA} \end{gathered}$ |  | $\begin{aligned} & 0.25 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & \hline 0.5 \\ & 0.8 \end{aligned}$ |  | $\begin{aligned} & 0.25 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.7 \end{aligned}$ | V |
| 11 | Input current at maximum input voltage Input current at maximum input voltage | $\begin{aligned} & \mathrm{V}_{C C}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{I}}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{I}}=5.5 \mathrm{~V} \end{aligned}$ |  |  | 1 |  |  | 1 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \mathrm{I}_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{IH}} \end{aligned}$ | High-level input current High-level input current | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V}, V_{1}=2.4 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V}, V_{1}=2.4 \mathrm{~V} \end{aligned}$ |  |  | 40 |  |  | 40 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| $\begin{aligned} & \text { IIL } \\ & \text { IIL } \end{aligned}$ | Low-level input current Low-level input current | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V}, V_{1}=0.4 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V}, V_{1}=0.4 \mathrm{~V} \end{aligned}$ |  | -1 | -1.6 |  | -1 | -1.6 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \mathrm{I} \mathrm{CCH} \\ & \mathrm{ICCH} \end{aligned}$ | Supply current, outputs high Supply current, outputs high | $\begin{aligned} & V_{C C}=5.5 V, V_{1}=5 V \\ & V_{C C}=5.25 V, V_{1}=5 V \end{aligned}$ |  | 8 | 11 |  | 8 | 11 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| ICCL ICCL | Supply current, outputs low Supply current, outputs low | $\begin{aligned} & V_{C C}=5.5 V, V_{1}=0 \\ & V_{C C}=5.25 V, V_{1}=0 \end{aligned}$ |  | 54 | 68 |  | 54 | 68 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 55454 |  |  | 75454 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | High-level input voltage Low-level input voltage |  |  | 2 |  | 0.8 | 2 |  | 0.8 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & V_{1} \\ & V_{1} \end{aligned}$ | Input clamp voltage Input clamp voltage | $\begin{aligned} & \mathrm{V}_{C C}=4.5 \mathrm{~V} \\|_{1}=-12 \mathrm{~mA} \\ & \mathrm{VCC}=4.75 \mathrm{~V} \\|_{1}=-12 \mathrm{~mA} \end{aligned}$ |  |  | -1.5 |  |  | -1.5 | V |
| $\begin{aligned} & \mathrm{IOH} \\ & \mathrm{IOH} \end{aligned}$ | High-level output current High-level output current | $\begin{array}{\|l\|} \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=30 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=30 \mathrm{~V} \end{array}$ |  |  | 300 |  |  | 100 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \mathrm{VOL} \\ & \mathrm{VOL} \end{aligned}$ | Low-level output voltage <br> Low-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \mathrm{IOL}_{\mathrm{OL}}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \mathrm{IOL}_{\mathrm{OL}}=300 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \mathrm{IOL}_{\mathrm{OL}}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V}, \mathrm{IOL}_{\mathrm{OL}}=300 \mathrm{~mA} \end{aligned}$ |  | $\begin{gathered} 0.25 \\ 0.5 \end{gathered}$ | $\begin{aligned} & 0.5 \\ & 0.8 \end{aligned}$ |  | $\begin{gathered} 0.25 \\ 0.5 \end{gathered}$ | $\begin{aligned} & 0.4 \\ & 0.7 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| 11 | Input current at maximum input voltage Input current at maximum input voltage | $\begin{aligned} & \mathrm{V}_{C C}=5.5 \mathrm{~V}, \mathrm{~V}_{1}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{C C}=5.25 \mathrm{~V}, \mathrm{~V}_{1}=5.5 \mathrm{~V} \end{aligned}$ |  |  | 1 |  |  | 1 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \mathrm{I}_{\mathrm{H}} \\ & \mathrm{I}_{\mathrm{H}} \end{aligned}$ | High-level input current High-level input current | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V}, V_{1}=2.4 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V}, V_{1}=2.4 \mathrm{~V} \end{aligned}$ |  |  | 40 |  |  | 40 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & I_{I L} \\ & I_{I L} \end{aligned}$ | Low-level input current Low-level input current | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V}, V_{1}=0.4 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V}, V_{1}=0.4 \mathrm{~V} \end{aligned}$ |  | -1 | -1.6 |  | -1 | -1.6 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \mathrm{ICCH} \\ & \mathrm{ICCH} \end{aligned}$ | Supply current, outputs high Supply current, outputs high | $\begin{aligned} & V_{C C}=5.5 \mathrm{~V}, V_{1}=0 \mathrm{~V} \\ & V_{C C}=5.25 \mathrm{~V}, V_{1}=0 \mathrm{~V} \end{aligned}$ |  | 13 | 17 |  | 13 | 17 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| ICCL ICCL | Supply current, outputs low Supply current, outputs Iow | $\begin{gathered} V_{C C}=5.5 \mathrm{~V}, V_{1}=5 \mathrm{~V} \\ V_{C C}=5.25 \mathrm{~V}, V_{1}=5 \mathrm{~V} \end{gathered}$ |  | 61 | 79 |  | 61 | 79 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=5 \mathrm{~V}$ unless otherwise specified.


AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 55451/75451 |  |  | 55452/75452 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| tpLH | Propagation delay time, low-to-high level output |  | $10 \approx 200 \mathrm{~mA}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=50 \Omega$ |  | 18 | 25 |  | 26 | 35 | ns |
| tphL | Propagation delay time, high-to-low level output | $10 \approx 200 \mathrm{~mA}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=50 \Omega$ |  | 18 | 25 |  | 24 | 35 | ns |
| ttith | Transition time, low-to-high level output | $1 \mathrm{O} \approx 200 \mathrm{~mA}, \mathrm{CL}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=50 \Omega$ |  |  |  |  | 5 | 8 | ns |
| tthl | Transition time, High-to-low level output | $10 \approx 200 \mathrm{~mA}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=50 \Omega$ |  | 7 | 12 |  | 7 | 12 | ns |
| VOH | High-level output voltage after switching | $\mathrm{V}_{\mathrm{s}}=20 \mathrm{~V}, 1 \mathrm{O} \approx 300 \mathrm{~mA}$ | Vs-6.5 |  |  | $V_{s}$-6.5 |  |  | mV |

NOTE
Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

AC ELECTRICAL CHARACTERISTICS (Cont'd) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | 55453/75453 |  |  | 55454/75454 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { tPLH } \\ & \text { tPHL } \end{aligned}$ | Propagation delay time, low-to-high level output Propagation delay time, high-to-low level output |  | $\begin{aligned} & 10 \approx 200 \mathrm{~mA}, C_{L}=15 \mathrm{pF}, R_{L}=50 \Omega \\ & 10 \approx 200 \mathrm{~mA}, C_{L}=15 \mathrm{pF}, R_{L}=50 \Omega \end{aligned}$ |  | $\begin{aligned} & 18 \\ & 16 \end{aligned}$ | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ |  | 27 24 | $\begin{aligned} & 35 \\ & 35 \end{aligned}$ | ns ns |
| tTLH <br> tTHL | Transition time, low-to-high level output Transition time, High-to-low level output | $\begin{aligned} & 10 \approx 200 \mathrm{~mA}, C_{L}=15 \mathrm{pF}, R_{L}=50 \Omega \\ & 10 \approx 200 \mathrm{~mA}, C_{L}=15 \mathrm{pF}, R_{L}=50 \Omega \end{aligned}$ |  | $5$ <br> 7 | 8 $12$ |  | $5$ $7$ | 8 12 | ns ns |
| VOH | High-level output voltage after switching | $\mathrm{V}_{\mathrm{S}}=20 \mathrm{~V}, \mathrm{I}_{0} \approx 300 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{S}}-6.5$ |  |  | $V_{\text {S }}-6.5$ |  |  | mV |

NOTE
Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

## LATCH-UP TEST OF COMPLETE DRIVERS



NOTES

1. The pulse generator has the following characteristics: $P R R=12.5 \mathrm{kHz}, \mathrm{Z}_{\text {OUT }}=50 \Omega$
2. When testing 55450 B or 75450 B , connect output Y to transistor base with a $500-\Omega$ resistor from there to ground, and ground to substrate terminal.
3. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.

## LATCH-UP TEST OF COMPLETE DRIVERS (Cont'd)



NOTES

1. The pulse generator has the following characteristics: $\mathrm{PRR}=12.5 \mathrm{kHz}, Z_{\text {OUT }}=50 \Omega$.
2. When testing 55450B or 75450 B , connect output $Y$ to transistor base with a $500-\Omega$ resistor from there to ground, and ground to substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

## SWITCHING TIMES OF COMPLETE DRIVERS



NOTES

1. The pulse generator has the following characteristics: $\mathrm{PRR}=1 \mathrm{MHz}, \mathrm{Z}_{\text {OUT }} \approx 50 \Omega$.
2. When testing 55451B or 75451 B , connect output $Y$ to translator base and ground the substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

## LATCH-UP TEST OF COMPLETE DRIVERS



NOTES

1. The pulse generator has the following characteristics: $P R R=12.5 \mathrm{kHz}$, Z OUT $=50 \Omega$.
2. When testing 55451 B or 75451 B , connect output $Y$ to transistor base with a $500-\Omega$ resistor from there to ground, and ground the substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

## SWITCHING TIMES OF COMPLETE DRIVERS



## SWITCHING TIMES OF COMPLETE DRIVERS (Cont'd)



NOTES

1. The pulse generator has the following characteristics: $P R R=1 \mathrm{MHz}, Z_{\text {OUT }} \approx 50 \Omega$.
2. When testing 55452B or 75452 B , connect output $Y$ to transistor base and ground the substrate terminal.
3. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.

## LATCH-UP TEST OF COMPLETE DRIVERS



## NOTES

1. The pulse generator has the following characteristics: $\mathrm{PRR}=12.5 \mathrm{kHz}, \mathrm{ZOUT}=50 \Omega$.
2. When testing 55452B or 75452 B , connect output Y to transistor base with a $500-\Omega$ resistor from there to ground, and ground the substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

## SWITCHING TIMES OF COMPLETE DRIVERS



NOTES

1. The pulse generator has the following characteristics: $P R R=1 \mathrm{MHz}, Z_{\text {OUT }} \approx 50 \Omega$.
2. When testing 55453B or 75453B, connect output $Y$ to transistor base and ground the substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

## LATCH-UP TEST OF COMPLETE DRIVERS



LATCH-UP TEST OF COMPLETE DRIVERS (Cont'd)


NOTES

1. The pulse generator has the following characteristics: $P R R=12.5 \mathrm{kHz}, \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$.
2. When testing 55453 B or 75453 B , connect output $Y$ to transistor base with a $500-\Omega$
resistor from there to ground, and ground the substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

SWITCHING TIMES OF COMPLETE DRIVERS


NOTES

1. The pulse generator has the following characteristics: $\mathrm{PRR}=1 \mathrm{MHz}, \mathrm{Z}$ OUT $\approx 50 \Omega$.
2. When testing 55454B or 75454B, connect output $Y$ to transistor base and ground the
substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

## LATCH-UP TEST OF COMPLETE DRIVERS



## NOTES

1. The pulse generator has the following characteristics: $\mathrm{PRR}=12.5 \mathrm{kHz}, \mathrm{ZOUT}=50 \Omega$.
2. When testing 55454 B or 75454 B , connect output $Y$ to transistor base with a $500-\Omega$ resistor from there to ground, and ground the substrate terminal.
3. $C_{L}$ includes probe and jig capacitance.

TYPICAL PERFORMANCE CHARACTERISTICS


1. These parameters must be measured using pulse techniques, $\mathrm{tw}=300 \mu \mathrm{~s}$, duty cycle $\leq$
2. This rating for the T Package requires a heat sink that provides a thermal resistance from case to free-air, ROCA, of not more than $95^{\circ} \mathrm{C} / \mathrm{W}$.

## sECTION 8 TRANSISTOR ARRAYS

## DESCRIPTION

The 510/511 are dual high frequency differential amplifiers with associated constant current sources and biasing elements contained within a silicon monolithic substrate. The large number of accessable internal points allows large flexibility of applications from dc to in excess of 100 mhz . Circuit layouts may be either common-common base, cascode or common collectorcommon base configurations.

## FEATURES

- Low input offset voltage $\pm \mathbf{2 m V}$
- Low input offset current $\pm 3 \mu \mathrm{~A}$
- AGC capability
- High forward transadmittance
- Low feed back capacitance
- Single power supply
- SE510, SE511 Mil std 883A,B,C available


## PIN CONFIGURATIONS




## EQUIVALENT SCHEMATICS



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Applied voltage (V+) | 20 | V |
| Differential input voltage | $\pm 5$ | V |
| Current (all pins) | $\pm 15$ | mA |
| Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE510N, SE511N | 0 to +75 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE510 |  |  | NE510 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage |  | Over temp. 2 |  | $\begin{aligned} & 0.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 3.5 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 0.5 \\ 1 \end{gathered}$ | $\begin{gathered} 3.0 \\ 4 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| los | Input offset current | Over temp. 2 |  | $\begin{aligned} & 2.0 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 7.5 \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 6 \\ & 9 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| IB | Input bias current | Over temp. 2 |  | $\begin{gathered} 8 \\ \hline 16 \end{gathered}$ | $\begin{aligned} & 20 \\ & 40 \end{aligned}$ |  | $\begin{gathered} 8 \\ 10 \end{gathered}$ | $\begin{aligned} & 25 \\ & 40 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| $\Delta \mathrm{l}$ c | Differential collector current per pair | $\begin{gathered} V_{\mathbb{N}}=0, I p=2 m A \\ \text { Over temp.2, } V_{I N}=0, I P=2 m A \end{gathered}$ |  | $\begin{aligned} & 45 \\ & 50 \end{aligned}$ | $\begin{aligned} & 62.5 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & 45 \\ & 50 \end{aligned}$ | $\begin{gathered} 75 \\ 100 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
|  | Differential source current | Over temp. 2 |  | $\begin{aligned} & 30 \\ & 35 \end{aligned}$ | $\begin{aligned} & \hline 62.5 \\ & 100 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 35 \\ & \hline \end{aligned}$ | $\begin{gathered} 75 \\ 100 \\ \hline \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Icc | Total current |  |  | 11 | 15 |  | 11 | 15 | mA |
| CMRR | Common mode rejection ratio |  | 60 | 80 |  | 60 | 80 |  | dB |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE511 |  |  | NE511 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Vos | Input offset voltage |  | Over temp. 2 |  | $\begin{aligned} & 0.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 3.5 \end{aligned}$ |  | $\begin{gathered} 0.5 \\ 1 \end{gathered}$ | $\begin{gathered} 3.0 \\ 4 \end{gathered}$ | $\begin{aligned} & m V \\ & m V \end{aligned}$ |
| Ios | Input offset current | Over temp. 2 |  | $\begin{gathered} 2 \\ 2.5 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 7.5 \end{aligned}$ |  | $\begin{gathered} 2 \\ 2.5 \end{gathered}$ | $\begin{aligned} & 6 \\ & 9 \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| IB | Input bias current | Over temp. 2 |  | $\begin{gathered} 8 \\ 16 \\ \hline \end{gathered}$ | $\begin{aligned} & 20 \\ & 40 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 8 \\ 10 \\ \hline \end{gathered}$ | $\begin{aligned} & 25 \\ & 40 \\ & \hline \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| $\Delta \mathrm{l}$ c | Differential collector current per pair | $\begin{gathered} V_{I N}=0, I P=2 m A \\ \text { Over temp.2, } V_{I N}=0, I P=2 m A \end{gathered}$ |  | $\begin{aligned} & 45 \\ & 50 \\ & \hline \end{aligned}$ | $\begin{gathered} 62.5 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 45 \\ & 50 \\ & \hline \end{aligned}$ | $\begin{gathered} 75 \\ 100 \\ \hline \end{gathered}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
|  | Differential source current | Over temp. 2 |  | $\begin{aligned} & 30 \\ & 35 \end{aligned}$ | $\begin{gathered} 62.5 \\ 100 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 30 \\ & 35 \\ & \hline \end{aligned}$ | $\begin{gathered} 75 \\ 100 \\ \hline \end{gathered}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| ICC | Total current |  |  | 11 | 15 |  | 11 | 15 | mA |
| CMRR | Common mode rejection ratio |  | 60 | 80 |  | 60 | 80 |  | dB |
| $\mathrm{G}_{22}$ | Output conductance |  |  | 0.01 |  |  | 0.01 |  | mmhos |
| $\begin{aligned} & \mathrm{C}_{\mathrm{OB}} \\ & \mathrm{C}_{\mathrm{IB}} \end{aligned}$ | Output capacitance Input capacitance |  |  | 2.5 10 |  |  | 2.5 10 |  | $\begin{aligned} & \mathrm{pF} \\ & \mathrm{pF} \end{aligned}$ |

NOTES

1. Standard test circuit of Figure 1.
2. Operating temperature range: SE510/511-55 ${ }^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ NE510/511 $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$

## DUAL DIFFERENTIIL AMPIFIER

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | EMITTER COUPLED |  |  | CASCODE |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\left[\begin{array}{l} \operatorname{Re}_{E}\left(Y_{11}\right) \\ \operatorname{RE}_{E}\left(Y_{22}\right) \end{array}\right.$ | Input conductance ${ }^{2,3}$ <br> Output conductance2,3 |  |  |  | $\begin{gathered} 0.7 \\ 0.01 \\ \hline \end{gathered}$ |  |  | $\begin{gathered} 3.0 \\ 0.01 \\ \hline \end{gathered}$ |  | mmhos mmhos |
| $\mathrm{C}_{1 \mathrm{~B}}$ <br> Сов | Input capacitance ${ }^{2,3}$ <br> Output capacitance2,3 <br> Reverse transfer capacitance2,3 |  |  | $\begin{gathered} 4.5 \\ 2.5 \\ 0.05 \end{gathered}$ |  |  | $\begin{gathered} 10 \\ 2.5 \\ 0.05 \end{gathered}$ |  | pF pF pF |
|  | Forward transconductance ${ }^{2,3}$ |  |  | 25 |  |  | 90 |  | mmhos |

NOTES

1. Applicable from $D C$ to 10 MHz
2. Emitter coupled configuration figure 2
3. Cascode configuration figure 3

TYPICAL PERFORMANCE CHARACTERISTICS


NOTE All characteristics for $25^{\circ} \mathrm{C}$ unless otherwise specified

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


NOTE All characteristics for $25^{\circ} \mathrm{C}$ unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## STANDARD TEST CIRCUIT (510)



Figure 1a

## STANDARD TEST CIRCUIT (511)



Figure 1b

## TEST LOAD CIRCUITS 510, 511



N $55501 / 55027550375504$

## DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600 mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type NE5501 is a general-purpose array which may be used with DTL, TTL PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type NE5502 was specifically designed for use with 14 to 25V PMOS devices. Each input has a Zener diode and resistor in series in order to limit the input current to a safe value.

The Type NE5503 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V .

The Type NE5504 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V . The required input current is below that of the Type NE5503 while the required input voltage is less than that required by the Type NE5502.
In all cases, the individual Darlington pair collector current rating is 500 mA . However outputs may be paralleled for higher load current capability. All devices are supplied in a 16 -pin dual in-line plastic " $N$ " package.

## FEATURES

- Output $\mathrm{V}_{\text {CEO }}>100 \mathrm{~V}$
- Peak inrush current 600 mA
- Protected internally against inductive loads
- Open collector topology
- Compatible with most logic technologies


## BLOCK DIAGRAM



PIN CONFIGURATION


## EQUIVALENT SCHEMATICS



ABSOLUTE MAXIMUM RATINGS ${ }^{1,2}$

| PARAMETER | RATING | UNIT |  |
| :--- | :--- | :---: | :---: |
| V $_{\text {CE }}$ | Output breakdown voltage | 100 | V |
| VIN | Input voltage (except 5501) | 30 | V |
| VEBO | Emitter base voltage | 6 | V |
| IC | Continuous collector current | 500 | mA |
| $\mathrm{I}_{\mathrm{B}}$ | Continuous base current | 25 | mA |
| $\mathrm{PD}_{\mathrm{D}}$ | Power dissipation | 1.3 | W |
| $\mathrm{~T}_{\mathrm{A}}$ | Ambient temperature | 0 to +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {Sg }}$ | Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTES

1. $T_{A}=25^{\circ} \mathrm{C}$
2. Thermal resistivity, $\theta \mathrm{j} \mathrm{A},=95^{\circ} \mathrm{C} /$ Watt.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. $1,2,3$

| PARAMETER |  | TEST CONDITIONS | NE5501 |  |  | NE5502 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| ICEX | Output leakage current |  | $\begin{gathered} \mathrm{V}_{\mathrm{CE}}= \\ 100 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C} \\ \text { Test Fig. } 1 \mathrm{~A} \\ \mathrm{~V}_{\mathrm{CE}}=100 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C}, \\ \mathrm{~V}_{\mathrm{IN}}=6 \mathrm{~V}, \text { Test Fig. } 1 \mathrm{~B} \end{gathered}$ |  | $\begin{gathered} 0.1 \\ - \end{gathered}$ | 10 |  | $\begin{gathered} - \\ 0.1 \end{gathered}$ | $10$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| VCESAT | Collecter emitter saturation voltage | $\begin{aligned} & I_{C}=350 \mathrm{~mA}, I_{B}=500 \mu \mathrm{~A}, \text { Test Fig. } 2 \\ & I_{C}=200 \mathrm{~mA}, I_{B}=350 \mu A \text {, Test Fig. } 2 \\ & I_{C}=100 \mathrm{~mA}, I_{B}=250 \mu A, \text { Test Fig. } 2 \end{aligned}$ |  | $\begin{aligned} & 1.6 \\ & 1.2 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 1.6 \\ & 1.4 \end{aligned}$ |  | $\begin{aligned} & 1.6 \\ & 1.2 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 1.6 \\ & 1.4 \end{aligned}$ | $\begin{aligned} & V \\ & V \\ & V \end{aligned}$ |
| IIN | Input current (ON) | $\mathrm{V}_{\mathrm{IN}}=17 \mathrm{~V}$, Test Fig. 3 |  | - |  |  | 0.9 | 1.45 | mA |
| $\begin{aligned} & \hline \operatorname{liN} \\ & \mathrm{VIN} \end{aligned}$ | Input current (OFF) Input voltage (ON) | $\mathrm{IC}=500 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$, Test Fig. 4 $V_{C E}=2 \mathrm{~V}, I_{C}=300 \mathrm{~mA}$, Test Fig. 5 | 50 | $65$ |  | 50 | 65 | 13 | $\mu \mathrm{A}$ |
| hFE | Forward current gain | $V_{C E}=2 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=350 \mathrm{~mA}$, Test Fig. 2 | 1000 |  |  |  | - |  |  |
| $\begin{aligned} & \mathrm{I}_{\mathrm{R}} \\ & \mathrm{~V}_{\mathrm{F}} \end{aligned}$ | Clamp diode leakage Clamp diode forward voltage | $\mathrm{V}_{\mathrm{R}}=100 \mathrm{~V}$, Test Fig. 6 $I_{F}=350 \mathrm{~mA}$, Test Fig. 7 |  | 1.6 | $\begin{aligned} & 10 \\ & 2.0 \end{aligned}$ |  | 1.6 | $\begin{aligned} & 10 \\ & 2.0 \end{aligned}$ | $\mu \mathrm{A}$ |

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. $1,2,3$

| PARAMETER |  | TEST CONDITIONS | NE5503 |  |  | NE5504 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| ICEX | Output leakage current |  | $\begin{gathered} V_{C E}=100 \mathrm{~V}, T_{A}=70^{\circ} \mathrm{C}, \\ \text { Test Fig. } 1 \mathrm{~A} \\ V_{C E}=100 \mathrm{~V}, T_{A}=70^{\circ} \mathrm{C}, \\ V_{\text {IN }}=1 \mathrm{~V}, \text { Test Fig. } 1 \mathrm{~B} \end{gathered}$ |  | $\begin{gathered} 0.1 \\ - \end{gathered}$ | 10 |  | $\begin{aligned} & - \\ & 0.1 \end{aligned}$ | 10 | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| VCESAT | Collecter emitter saturation voltage | $\begin{aligned} & I_{C}=350 \mathrm{~mA}, I_{B}=500 \mu A, \text { Test Fig. } 2 \\ & I_{C}=200 \mathrm{~mA}, I_{B}=350 \mu A, \text { Test Fig. } 2 \\ & I_{C}=100 \mathrm{~mA}, I_{B}=250 \mu A, \text { Test Fig. } 2 \end{aligned}$ |  | $\begin{aligned} & 1.6 \\ & 1.2 \\ & 1.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 1.6 \\ & 1.4 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.6 \\ & 1.2 \\ & 1.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 1.6 \\ & 1.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| IIN | Input current (ON) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=3.85 \mathrm{~V} \text {, Test Fig. } 3 \\ & \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{~V} \text {, Test Fig. } 3 \\ & \mathrm{VIN}_{\mathrm{IN}}=12 \mathrm{~V} \text {, Test Fig. } 3 \end{aligned}$ |  | $1.05$ <br> - | 1.65 |  | $\begin{aligned} & \overline{0.4} \\ & 1.1 \end{aligned}$ | $\begin{gathered} 0.65 \\ 1.7 \end{gathered}$ | mA <br> mA <br> mA |
| $\begin{aligned} & \mathrm{I}_{\mathrm{IN}} \\ & \mathrm{~V}_{\mathrm{IN}} \end{aligned}$ | Input current (OFF) Input voltage (ON) | $\begin{aligned} & \mathrm{I}_{\mathrm{C}}=500 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C} \text {, Test Fig. } 4 \\ & \mathrm{~V}_{C E}=2 \mathrm{~V}, \mathrm{IC}=200 \mathrm{~mA} \text {, Test Fig. } 5 \\ & \mathrm{~V}_{\mathrm{CE}}=2 \mathrm{~V}, \mathrm{IC}=250 \mathrm{~mA} \text {, Test Fig. } 5 \\ & \mathrm{~V}_{\mathrm{CE}}=2 \mathrm{~V}, \mathrm{IC}_{\mathrm{C}}=300 \mathrm{~mA} \text {, Test Fig. } 5 \end{aligned}$ | 50 | 65 | $\begin{aligned} & 2.4 \\ & 2.7 \\ & 3.0 \\ & \hline \end{aligned}$ | 50 | $65$ <br> - $\qquad$ $-$ |  | $\begin{gathered} \mu \mathrm{A} \\ \mathrm{~V} \\ \mathrm{~V} \\ \mathrm{~V} \end{gathered}$ |
| VIN | Input voltage (ON) | $\begin{aligned} & V_{C E}=2 V \text {, } I C=125 \mathrm{~mA} \text {, Test Fig. } 5 \\ & V_{C E}=2 V, I C=200 \mathrm{~mA} \text {, Test Fig. } 5 \\ & V_{C E}=2 V, I C=275 \mathrm{~mA} \text {, Test Fig. } 5 \\ & V_{C E}=2 V, I C=350 \mathrm{~mA} \text {, Test Fig. } 5 \end{aligned}$ |  |  |  |  |  | $\begin{aligned} & \hline 5.0 \\ & 6.0 \\ & 7.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & \hline V \\ & V \\ & V \\ & V \end{aligned}$ |
| $I_{\text {R }}$ | Clamp diode leakage | $\mathrm{V}_{\mathrm{R}}=100 \mathrm{~V}$, Test Fig. 6 |  |  | 10 |  |  | 10 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{F}}$ | Clamp diode forward voltage | $I_{F}=350 \mathrm{~mA}$, Test Fig. 7 |  | 1.6 | 2.0 |  | 1.6 | 2.0 | V |

## NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The IIN(OFF) current limit guarantees against partial turn-on of the output.
3. The $V_{I N(O N)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TO | FROM | TEST CONDITIONS | NE5501 |  |  | NE5502 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max | Min | Typ | Max |  |
| CIN | Input capacitance |  |  |  |  |  | 15 | 30 |  | 15 | 30 | pF |
| TPLH | Turn on delay | Input | Output | 50\% Ein to 50\% EOUT |  | 1 | 5 |  | 1 | 5 | $\mu \mathrm{S}$ |
| TPHL | Turn off delay | Input | Output | 50\% Ein to 50\% EOUT |  | 1 | 5 |  | 1 | 5 | $\mu \mathrm{S}$ |

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TO | FROM | TEST CONDITIONS | NE5503 |  |  | NE5504 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max | Min | Typ | Max |  |
| CIN | Input capacitance |  |  |  |  |  | 15 | 30 |  | 15 | 30 | pF |
| TPLH | Turn on delay | Input | Output | 50\% EIN to 50\% EOUT |  | 1 | 5 |  | 1 | 5 | $\mu \mathrm{S}$ |
| TPHL | Turn off delay | Input | Output | 50\% EIN to 50\% EOUT |  | 1 | 5 |  | 1 | 5 | $\mu \mathrm{S}$ |

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The lin(OFF) current limit guarantees against partial turn-on of the output. 3. The $\left.\mathrm{V}_{\mathrm{IN}(O)}\right)$ voltage limit guarantees a minimum output sink current per the specified test conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE NE5502


COLLECTOR CURRENT AS A FUNCTION OF
INPUT CURRENT


INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE NE5503


ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE NE5504


TEST LOAD CIRCUITS


Figure 1A



Figure 6


Figure 7

TYPICAL APPLICATIONS



## DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600 mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type ULN-2001 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type ULN-2002 was specifically designed for use with 14 to 25V PMOS devices. Each input has a Zener diode and resistor in series in order to limit the input current to a safe value.

The Type ULN-2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V .
The Type ULN-2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V . The required input current is below that of the Type ULN2003 while the required input voltage is less than that required by the Type ULN-2002.
In all cases, the individual Darlington pair collector current rating is 500 mA . However, outputs may be paralleled for higher load current capability. All devices are supplied in a $16-\mathrm{pin}$ dual in-line plastic "BA" package.

## FEATURES

- Peak inrush current 600 mA
- Protected internally against inductive loads
- Open collector topology
- Compatible with most logic technologies

PIN CONFIGURATION


## EQUIVALENT SCHEMATICS


at $25^{\circ} \mathrm{C}$ Free-Air temperature for any one Darlington pair unless otherwise specified.
ABSOLUTE MAXIMUM RATINGS

| PARAMETER |  | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| $V_{\text {ce }}$ | Output voltage | 50 | V |
| V IN | Input voltage | 30 | V |
| VEBO | Emitter base voltage | 6 | V |
| 1 c | Continuous collector current | 500 | mA |
| IB | Continuous base current | 25 | mA |
| PD | Power dissipation | 1.3 | W |
|  | Derating factor above $25^{\circ} \mathrm{C}$ | 95 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{T}_{\text {A }}$ | Ambient temperature range (operating) | 0 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Ts | Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## *NOTE

Under normal operating conditions, these units will sustain 350 mA per output with
$V_{\text {CE(SAT) }}=1.6 \mathrm{~V}$ at $70^{\circ} \mathrm{C}$ with a pulse width of 20 ms and a duty cycle of $30 \%$.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. 1, 2,3

| PARAMETER |  | TEST CONDITIONS | Test Fig. | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  | Typ | Max |  |
| Icex | Output leakage current <br> Type ULN-2002 <br> Type ULN-2004 |  | $\begin{gathered} V_{C E}=50 \mathrm{~V}, T_{A}=70^{\circ} \mathrm{C} \\ V_{C E}=50 \mathrm{~V}, T_{A}=70^{\circ} \mathrm{C}, V_{I N}=6 \mathrm{~V} \\ V_{C E}=50 \mathrm{~V}, T_{A}=70^{\circ} \mathrm{C}, V_{I N}=1 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & 1 \mathrm{~A} \\ & 1 \mathrm{~B} \\ & 1 \mathrm{~B} \\ & \hline \end{aligned}$ | - | - | $\begin{aligned} & \hline 100 \\ & 500 \\ & 500 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{\text {CE( }}(\mathrm{SAT})$ | Collector-emitter Saturation voltage | $\begin{aligned} & I_{C}=350 \mathrm{~mA}, I_{B}=500 \mu \mathrm{~A} \\ & I_{C}=200 \mathrm{~mA}, I_{B}=350 \mu \mathrm{~A} \\ & I_{C}=100 \mathrm{~mA}, I_{B}=250 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 2 \\ & 2 \\ & 2 \end{aligned}$ | - | $\begin{array}{r} 1.25 \\ 1.1 \\ 0.9 \\ \hline \end{array}$ | $\begin{aligned} & 1.6 \\ & 1.3 \\ & 1.1 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| $\operatorname{lin}(O N)$ | Input current <br> Type ULN-2002 <br> Type ULN-2003 <br> Type ULN-2004 | $\begin{gathered} V_{I N}=17 \mathrm{~V} \\ V_{I N}=3.85 \mathrm{~V} \\ V_{I N}=5 \mathrm{~V} \\ V_{I N}=12 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & 3 \\ & 3 \\ & 3 \\ & 3 \\ & \hline \end{aligned}$ | - | $\begin{gathered} 0.85 \\ 0.93 \\ 0.35 \\ 1.0 \\ \hline \end{gathered}$ | $\begin{gathered} 1.3 \\ 1.35 \\ 0.5 \\ 1.45 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| $\operatorname{lin}$ (OFF) | Input current | $\mathrm{I}_{\mathrm{C}}=500 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ | 4 | 50 | 65 | - | $\mu \mathrm{A}$ |
| VIN(ON) | Input voltage Type ULN-2002 | $\mathrm{V}_{\mathrm{CE}}=2 \mathrm{~V}, \mathrm{IC}=300 \mathrm{~mA}$ | 5 | - | - | 13 | V |
|  | Type ULN-2003 | $\begin{aligned} & V_{C E}=2 \mathrm{~V}, I_{C}=200 \mathrm{~mA} \\ & V_{C E}=2 \mathrm{~V}, I_{C}=250 \mathrm{~mA} \\ & V_{C E}=2 \mathrm{~V}, I_{C}=300 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 5 \\ & 5 \\ & 5 \\ & \hline \end{aligned}$ | - | - | $\begin{aligned} & 2.4 \\ & 2.7 \\ & 3.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { v } \\ & \text { v } \\ & \text { v } \end{aligned}$ |
|  | Type ULN-2004 | $\begin{aligned} & \mathrm{V}_{\mathrm{CE}}=2 \mathrm{~V}, \mathrm{IC}=125 \mathrm{~mA} \\ & \mathrm{~V}_{C E}=2 \mathrm{~V}, \mathrm{IC}=200 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CE}}=2 \mathrm{~V}, \mathrm{IC}=275 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CE}}=2 \mathrm{~V}, \mathrm{IC}_{\mathrm{C}}=350 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 5 \\ & 5 \\ & 5 \\ & 5 \end{aligned}$ | - | - | $\begin{aligned} & 5.0 \\ & 6.0 \\ & 7.0 \\ & 8.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \\ & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| hfe | D-C forward current transfer ratio Type ULN-2001 | $\mathrm{V}_{C E}=2 \mathrm{~V}, \mathrm{IC}=350 \mathrm{~mA}$ | 2 | 1000 |  | - | - |
| $\mathrm{CIN}_{\text {I }}$ | Input capacitance |  | - | - | 15 | 30 | pF |
| $\mathrm{I}_{\mathrm{R}}$ | Clamp diode leakage current | $V_{R}=50 \mathrm{~V}$ | 6 | - | - | 50 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{F}$ | Clamp diode forward voltage | $1 \mathrm{~F}=350 \mathrm{~mA}$ | 7 | - | 1.7 | 2 | V |

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{\mathbb{N}(\mathrm{OFF})}$ current limit guarantees against partial turn-on of the output.
3. The $V_{I N(O N)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. $1,2,3$

| PARAMETER |  | TEST CONDITIONS | Test Fig. | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  | Typ | Max |  |
| tplH | Turn-on delay |  | $0.5 \mathrm{E}_{\text {IN }}$ to 0.5 EOUT | - | - | 1.0 | 5 | $\mu \mathrm{S}$ |
| tpHL | Turn-off delay | $0.5 \mathrm{E}_{\text {IN }}$ to $0.5 \mathrm{E}_{\text {OUT }}$ | - | - | 1.0 | 5 | $\mu \mathrm{S}$ |

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The IIN(OFF) current limit guarantees against partial turn-on of the output.
3. The $V_{I N(O N)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS

COLLECTOR CURRENT AS A FUNCTION
OF SATURATION VOLTAGE


INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2002

COLLECTOR CURRENT AS A FUNCTION OF
INPUT CURRENT


INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2003

ALLOWABLE AVERAGE PACKAGE POWER
DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2004


## TEST FIGURES



## TEST FIGURES (Cont'd)




Figure 7

## TYPICAL APPLICATIONS



## DESCRIPTION

The CA3081 and CA3082 are monolithic integrated circuits each consisting of seven separate npn transistors on a common substrate. The transistors are capable of driving loads up to 100 mA . At the same time the transistor geometry used gives maximum current gain at quite low currents, making the devices also suitable for small signal applications. In the CA3081 the transistors are connected in common emitter configuration while in the CA3082 the collectors are common. The transistor arrays are particularly suitable for driving light-emitting diodes and seven-segment displays as well as for general purpose applications.

## FEATURES

- $\mathrm{V}_{\text {CBO }}=50 \mathrm{~V}$
- $\mathrm{V}_{\text {CEO }}=35 \mathrm{~V}$
- Collector current 100 mA
- Common emitter or common collector configuration


## PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

| PARAMETER |  | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| VCeo | Collector-emitter voltage (open base) | 35 | V |
| Vcbo | Collector-base voltage (open emitter) | 50 | V |
| Vcso | Collector-substrate voltage (open base and emitter) | 50 | V |
| Vebo | Emitter-base voltage (open collector) | 6 | V |
| Ic | Collector current (dc) | 100 | mA |
| $\mathrm{IB}_{\mathrm{B}}$ | Base current (dc) | 20 | mA |
| P | Power dissipation: any one transistor | 500 | mW |
| Рtot | total package (see derating curve) | 750 | mW |
| $\mathrm{T}_{\mathrm{A}}$ | Operating ambient temperature | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {stg }}$ | Storage temperature | -50 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Tj | Junction temperature | 125 | ${ }^{\circ} \mathrm{C}$ |
|  | Lead temperature (10 sec) | 300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | CA3081/3082 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| VCEO Collector-emitter breakdown voltage | $\mathrm{IC}_{\mathrm{C}}=1 \mathrm{~mA}, \mathrm{I}_{\mathrm{B}}=0$ | 35 |  |  | V |
| Vcso Collector-substrate breakdown voltage | $\mathrm{IC}=1 \mathrm{~mA}, \mathrm{I}_{B}=0, \mathrm{I}_{\mathrm{E}}=0$ | 50 |  |  | V |
| $V_{C B O}$ Collector-base breakdown voltage | $I_{C}=10 \mu \mathrm{~A}, \mathrm{IE}=0$ | 50 |  |  | V |
| $V_{E B O}$ Emitter-base breakdown voltage | $\mathrm{IE}_{\mathrm{E}}=10 \mu \mathrm{~A}, \mathrm{IC}=0$ | 6.5 | 7.0 | 7.5 | V |
| hfe DC current gain | $\begin{aligned} & I_{E}=10 \mu \mathrm{~A}, V_{C E}=5 \mathrm{~V} \\ & I_{E}=1 \mathrm{~mA}, V_{C E}=5 \mathrm{~V} \\ & I_{E}=20 \mathrm{~mA}, V_{C E}=5 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 50 \\ & 50 \\ & 30 \end{aligned}$ |  | $\begin{aligned} & 300 \\ & 300 \\ & 200 \end{aligned}$ |  |
| VSAT Saturation voltage | $\begin{aligned} & I_{C}=5 \mathrm{~mA}, I_{B}=.5 \mathrm{~mA} \\ & I_{C}=50 \mathrm{~mA}, I_{B}=5 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 0.2 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |

NOTE
As each collector forms a parasitic diode with the substrate, the substrate has to be connected to a voltage which is lower than the lowest collector voltage.
To avoid parasitic coupling between the transistors, the substrate ( pin 5 ) should be connected to signal ground.

## TYPICAL PERFORMANCE CHARACTERISTICS



## sECTION 9 philups industrint

## DESCRIPTION

The NE502 is a MOS monolithic integrated circuit, generally intended to delay analogue signals (e.g. delay time $=512 / 2 \mathrm{f}_{0}$ ).

It can be used with clock frequencies in the range 5 kHz to 500 kHz .
The device contains 512 stages, so the input signal can be delayed from 51.2 ms to 0.512 ms .

## APPLICATIONS

- Fixed analog delay
- Vox control
- Equalizing speech delay in PA systems
- Vibrato and chorus effects
- Reverberation
- Variable compression/expansion of speech
- Speech scrambling and time scale conversion


## FEATURES

- 5 to 500 kHz clock frequency
- 512 stages
- Signal delay of $\mathbf{5 1 . 2}$ to .512 ms
- Signal frequency to $\mathbf{4 5 k H z}$


## PIN CONFIGURATION



## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{9-16}$ | Voltages* |  |  |
|  | Supply voltage | 0 to -20 | V |
|  | Clock input, data input, output voltage and $V_{13-16}$ | 0 to -18 | V |
|  | Current |  |  |
| $\mathrm{I}_{8,1} \mathrm{I}_{12}$ | Output current | 0 to +5 | mA |
|  | Temperatures |  |  |
| $\begin{aligned} & \mathrm{T}_{S T G} \\ & \mathrm{~T}_{\mathrm{A}} \end{aligned}$ | Storage temperature | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
|  | Operating ambient temperature | -20 to +85 | ${ }^{\circ} \mathrm{C}$ |

*NOTE
Though MOS integrated circuits incorporate protection against electrostatic discharge,
they can nevertheless be damaged by accidental over-voltages. To be totally safe, it is
desirable to take handling precautions into account.

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=-20^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{DD}}=-15 \mathrm{~V}, \mathrm{~V}_{\phi_{1}}=\mathrm{V}_{\phi_{2}}=-15 \mathrm{~V}$,
$V_{13-16}=-14 \mathrm{~V}, R_{L}=47 \mathrm{k} \Omega$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | NE502 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\begin{aligned} & \text { VDD } \\ & \text { IDD } \end{aligned}$ | Supply voltage ${ }^{1}$ Supply current |  |  | -18 | . 3 | -10 | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| $V_{\phi 1 H}, V_{\phi 2 H}$ $\mathrm{V} \phi_{1 \mathrm{~L}}, \mathrm{~V} \boldsymbol{\phi}_{2 \mathrm{~L}}$ | Clock voltage high Clock voltage low 1 |  | $\begin{array}{r} \hline-1.5 \\ -18 \\ \hline \end{array}$ | -15 | $\begin{gathered} 0 \\ -10 \end{gathered}$ | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| $\begin{aligned} & \mathrm{VIN} \\ & \mathrm{R} \end{aligned}$ | Input voltage Load resistance ${ }^{1}$ | Vout $\leq 1 \%$ THD | 10 | $\begin{aligned} & 2.5 \\ & 47 \end{aligned}$ |  | Vrms $\mathrm{k} \Omega$ |

AC ELECTRICAL CHARACTERISTICS $\quad T_{A}=-20^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}, \mathrm{V}_{D D}=-15 \mathrm{~V}, \mathrm{~V}_{\phi_{1}}=\mathrm{V}_{\phi_{2}}=-15 \mathrm{~V}$,
$V_{13-16}=-14 \mathrm{~V}, R_{L}=47 \mathrm{k} \Omega$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | NE502 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| $\mathrm{f}_{1},{ }_{1} \mathrm{f}_{\boldsymbol{2}}$ | Clock frequency ${ }^{2}$ |  | 5 |  | 500 | kHz |
| $\mathrm{T} \phi_{1}, \mathrm{~T} \phi_{2}$ <br> $T_{r} \phi_{1}, T_{r} \phi_{2}$ <br> $T_{f} \phi_{1}, T_{f} \phi_{2}$ | Clock pulse width ${ }^{3}$ Clock rise time ${ }^{3}$ Clock fall time ${ }^{3}$ |  |  | $\begin{aligned} & 0.05 \\ & 0.05 \\ & \hline \end{aligned}$ | . 5 | $\begin{aligned} & \hline T \\ & T \\ & T \end{aligned}$ |
| $\mathrm{f}_{\mathrm{s}}$ | Signal frequency Signal attenuation 1 | $\mathrm{f}_{\phi}=40 \mathrm{kHz}, \mathrm{f}_{\mathrm{s}}=1 \mathrm{kHz}$ | 0 | 4 | $\begin{aligned} & 45 \\ & 7 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{kHz} \\ \mathrm{~dB} \end{gathered}$ |
|  | Output signal variation Output signal variation | $\begin{gathered} \mathrm{f}_{\mathrm{s}}=1 \mathrm{kHz}, \mathrm{~V}_{\mathrm{s}}=1 \mathrm{Vrms}, 5 \mathrm{kHz} \leq \mathrm{f}_{\phi} \leq 100 \mathrm{kHz} \\ \mathrm{f}_{\mathrm{s}}=1 \mathrm{kHz}, \mathrm{~V}_{\mathrm{s}}=1 \mathrm{Vrms}, 100 \mathrm{kHz} \leq \mathrm{f}_{\phi} \leq 300 \mathrm{kHz} \\ \hline \end{gathered}$ |  | $\begin{array}{r} .5 \\ .5 \\ \hline \end{array}$ | $\begin{aligned} & 1 \\ & 1 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \hline \end{aligned}$ |
| $\Delta \mathrm{V}_{\text {OUT }}$ | DC voltage shift | $5 \mathrm{kHz} \leq \mathrm{f} \phi \leq 300 \mathrm{kHz}$ |  |  | . 5 | V |
| $\begin{aligned} & V_{N} \\ & S / N \end{aligned}$ | Noise voltage Signal to noise | $\mathrm{f} \phi=100 \mathrm{kHz}$ (weighted by "A" curve) |  | $\begin{aligned} & 25 \\ & 74 \end{aligned}$ |  | $\underset{\mathrm{dB}}{\mathrm{mVrms}}$ |

NOTES

1. It is recommended that $V_{13-16}=V_{\phi_{1 L}}+1 V=V_{\phi 2 L}+1 V ; V_{D D}$ more negative than $V_{\phi L}$.
2. In theory the clock frequency must be higher than twice the highest signal frequency; in practice $f_{S} \leq 0.3 f \phi$ to $0.5 f \phi$ is recommended, depending on the characteristics of the output filter.
3. $T=$ period time $=1 / \mathrm{f} \phi$. The data on fall and rise times are given to eliminate overlap between the two clock pulses. To be independent of these rise and fall times a clock generator with simple gating can be used. See also pages 5 and 8 .

TIMING DIAGRAM


TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


TYPICAL APPLICATIONS


TYPICAL APPLICATIONS (Cont'd)


TYPICAL APPLICATIONS (Cont'd)


## DESCRIPTION

The SAA1027 is intended for driving a four phase two stator stepper motor. The circuit consists of four output stages, a logic part and three input stages. The logic part is driven by three input stages; a trigger input stage, an input stage which can change the switching sequence of the logic part so that the motor can rotate clock wise (CW) or counter clock wise (CCW) and a set input stage to set the four output stages. The three inputs are compatible with high noise immunity logic to ensure proper operation, even in noisy environments. The output can deliver 350 mA in each phase. The right switching sequence of the four phases is obtained from the logic part of the circuit. Integrated diodes protect the outputs against transient spikes.

## FEATURES

- CW or CCW rotation
- 4-phase drive
- Few external components

PIN CONFIGURATION

| N PACKAGE |  |
| :---: | :---: |
| nc 1 | 16 nc |
| S (SET INPUT) 2 | 15 trigger input |
| R(CW/CCW input $\qquad$ | $14{ }^{14} \mathrm{~V}_{\text {P P POSITIVE }}$ |
| $\mathrm{V}_{\mathrm{B}}$ POSITIVE ${ }_{\text {SUPPLY }} 4$ | 13] ${ }^{\text {V }}$ SUPPSITIVE |
| Ground 5 | 12] Ground |
| OUTPUT Q1 6 | 11 OUTPUT $0_{4}$ |
| NC 7 | 10 NC |
| OUTPUT Q2 8 | 9 OUTPUT Q3 |
| ORDER PART NO. SAA 1027 N |  |

## EQUIVALENT SCHEMATIC

BI-DIRECTIONAL, 4 POSITION, SYNCHRONOUS COUNTER


EQUIVALENT SCHEMATIC (Cont'd)


ABSOLUTE MAXIMUM RATINGS Limiting values in accordance with the

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
|  | VOLTAGES |  |  |
| $V_{P}$ | Supply voltage (pin 4, 13, 14) | 20 | V |
| $\mathrm{V}_{1}$ | Input voltage; R (pin 3), S (pin 2), $T$ (pin 15) | 20 | v |
|  | CURRENT |  |  |
| 10 | Output current; $\mathrm{Q}_{1}($ pin 6$), \mathrm{Q}_{2}($ pin 8$), \mathrm{Q}_{3}$ | 500 | mA |
|  | POWER DISSIPATION | See figure 1 |  |
|  | TEMPERATURES |  |  |
| Tstg | Storage temperature | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {A }}$ | Operating ambient temperature | -20 to +70 | ${ }^{\circ} \mathrm{C}$ |
|  | THERMAL RESISTANCE |  |  |
| $\theta_{\mathrm{ja}}$ | From junction to ambient | 70 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*NOTE
Additional power caused by the self-inductance of the motor-coils will be dissipated in the diodes (D31 to D34).

TRUTH TABLE1,2

| $\mathbf{S}=\mathbf{H}$ |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}=\mathrm{H}$ |  |  |  |  | $\mathbf{R}=\mathbf{L}$ |  |  |  |  |
| T | Q1 | Q2 | Q3 | Q4 | T | Q1 | Q2 | Q3 | Q4 |
| 0 | L | H | L | H | 0 | L | H | L | H |
| 1 | H | L | L | H | 1 | L | H | H | L |
| 2 | H | L | H | L | 2 | H | L | H | L |
| 3 | L | H | H | L | 3 | H | L | L | H |
| 4 | L | H | L | H | 4 | L | H | L | H |

NOTES
Trigger Conditions(T)

1. Direction conditions (R)

The direction of rotation can be changed at any moment independent of the state of
the $T$ and $S$ inputs.
2. Set conditions (S)

When $T$ is HIGH and $S$ LOW then the outputs are set: $Q_{1}=L, Q_{2}=H, Q_{3}=L, Q_{4}=H$.

DC ELECTRICAL CHARACTERISTICS $-20^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 65^{\circ}, \mathrm{V}_{\mathrm{P}}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SAA1027 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $V_{P}$ | Supply voltage (pin 14) |  |  | 9.5 | 12 | 18 | V |
| $I_{P}$ $V_{I H}$ $I_{I H}$ $V_{I L}$ $I_{I L}$ | Supply current | Pin 4 open, without loads, all inputs high <br> R, S, T inputs <br> R, $S, T$ inputs <br> R, S, T inputs <br> R, S, T inputs | $\begin{aligned} & 2.0 \\ & 7.5 \end{aligned}$ | $\begin{gathered} 4.5 \\ 1 \\ 30 \end{gathered}$ | $6.5$ $4.5$ | $\begin{gathered} \mathrm{mA} \\ \mathrm{~V} \\ \mu \mathrm{~A} \\ \mathrm{~V} \\ \mu \mathrm{~A} \\ \hline \end{gathered}$ |
| $V_{Q}$ <br> lQ $V_{\text {SAT }}$ | Supply voltage Supply current Saturation voltage | Each output stage Each output stage | 1.5 | 12 | $\begin{gathered} 18 \\ 350 \\ 1 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \\ \mathrm{~V} \end{gathered}$ |
|  | Bias voltage and current <br> Bias resistor <br> Bias resistor power dissipation | Reference Figure 2. Reference Figure 3. Reference Figure 4. |  |  |  |  |
|  | Device power dissipation | Reference Figure 5. |  |  |  |  |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 1

BIAS VOLTAGE AND CURRENT


Figure 2

BIAS RESISTOR


Figure 3

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


Figure 4

TYPICAL APPLICATIONS


Figure 6

## DESCRIPTION

The TAA960 consists of three identical general-purpose amplifiers integrated in a single silicon chip. The amplifiers can be used separately or can be cascaded to give a voltage gain of 117 dB . One of the amplifiers has an additional emitter-follower stage. The TAA960 is very suitable for use in an active RC band-pass filter with $Q$ up to 60 .

## FEATURES

- Cascade voltage gain of 117 dB
- Typical Q of 45 in filter
- Input resistance > 25K
- Triple configuration
- Emitter follower output available


## EQUIVALENT SCHEMATIC



## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
|  | Voltages with respect to pin 10 |  |  |
| $V_{3}$ | Supply voltage | 10 | V |
| $\mathrm{V}_{8}, \mathrm{~V}_{7}, \mathrm{~V}_{1}$ | Input voltage | 4 | V |
| $\mathrm{V}_{6}, \mathrm{~V}_{5}, \mathrm{~V}_{4}, \mathrm{~V}_{2}$ | Output voltage | 10 | V |
| $\mathrm{I}_{8}, \mathrm{I}_{7}, \mathrm{I}_{1}$ | Input current | 50 | $\mu \mathrm{A}$ |
| Рtot | Total power dissipation | 250 | mW |
| Tstg | Storage temperature | -65 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{A}}$ | Operating ambient temperature | -55 to +65 | ${ }^{\circ} \mathrm{C}$ |

NOTES:

1. With lower dc potential on all other terminals.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=6 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TAA960 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Icc | Supply current ${ }^{2}$ |  |  | 1.5 | 2.0 | 2.5 | mA |
| Icc | Supply current ${ }^{2}$ | $\mathrm{V}_{3}=10 \mathrm{~V}$ | 1.5 | 2.6 | 3.8 | mA |
| Avol | Voltage gain (each amplifier) |  | 60 | 90 | 150 | V/V |
| RIN | Input resistance |  | 25 |  |  | k $\Omega$ |
| Rout Rout | Output resistance <br> Output resistance | Pins 2, 5 \& 6 <br> Pin 4 | $\begin{gathered} 8 \\ 135 \end{gathered}$ | 9 | 750 | $\begin{gathered} \mathrm{k} \Omega \\ \Omega \end{gathered}$ |

NOTES
2. Terminal 8 connected to terminal 6

Terminal 7 connected to terminal 5
Terminal 1 connected to terminal 2

## TYPICAL APPLICATIONS

ACTIVE RC FILTER FOR FREQUENCIES UP TO 150 kHz

$R=10 \mathrm{k} \Omega$
This frequency range can be extended to 200 kHz if a feed forward capacitor is connected between pin 5 and 8 .

| f | Frequency | $\frac{1}{2 \pi \mathrm{RC}}$ |  |
| :---: | :---: | :---: | :---: |
| $V_{p}$ | Supply voltage | 6 | v |
|  | Filter performance |  |  |
| Q | at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 40 to 55 |  |
| Q | at $\mathrm{T}_{\mathrm{A}}=-30$ to $+65^{\circ} \mathrm{C}$ | 35 to 55 |  |
| $\mathrm{V}_{\mathrm{i}}$ | Input voltage | 400 | mV |
| $V_{0}$ | Output voltage | 400 | mV |
| dtot | Distortion at $\mathrm{V}_{0}=350 \mathrm{mV}$ | 2 | \% |
| S/N | $\mathrm{S} / \mathrm{N}$ ratio at $\mathrm{V}_{0}=400 \mathrm{mV}$ | 50 | dB |
| Rs | Input resistor* | 470 | k $\Omega$ |

*NOTE
Value of input resistor to be determined for $\frac{V_{0}}{V_{i}}=0.90$ to 1.1.

## DESCRIPTION

The TCA210 is a monolithic integrated circuit comprising two amplifiers for use in intercoms and other audio systems. The first is a high-grain pre-amplifier with differential input and a class-A output stage which can deliver 2.5 mW into an $800 \Omega$ load. The second is a power amplifier with a class-B output stage capable of delivering 500 mW into a $25 \Omega$ load.

Speech rating: up to 800 mW can be delivered into a $15 \Omega$ load for short periods. When there is no signal, the current consumption is 8 mA (typ.). Squelch provision incorporated in both amplifiers can be used to ensure maximum battery life.

## FEATURES

- Noise figure < 6dB
- Separate supply and ground leads
- Preamp open loop gain of $10 \mathrm{KV} / \mathrm{V}$
- Output amplifier gain of 500V/V
- Output power 500 mW

PIN CONFIGURATION


## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Voltages |  |  |
| Pin 8 must be externally connected to pin 16 |  | V |
| Pins 3, 9, 10, 14 with respect to pin 16 | 17 | $\mathrm{~V}^{\star}$ |
| Pins 1, 15, 5, 13 with respect to pin 16 | 17 | V |
| Pin 1 with respect to pin 15 | $\pm 5$ | mA |
| Pin 5 with respect to pin 13 | $\pm 5$ | mA |
| Currents | 550 | mA |
| Pin 10 | mA |  |
| Pin 9 | 550 | mA |
| Pin 8 | 20 | mA |
| Pin 14 | 5 | mA |
| Pin 3 | 0,5 | ${ }^{\circ} \mathrm{C}$ |
| Pins 2, 4, 6, 7, 11, 12 | -55 to +125 |  |
| Pins 1, 15, 5, 13 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Temperatures |  |  |
| Storage temperature TSTG |  |  |
| Operating ambient temperature |  |  |
| (see also graph) TA |  |  |

*NOTE
For a supply voltage less than 14 V , the maximum input voltage is equal to the supply
voltage.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=12$ volts unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| IB Input bias current | Pins 1 and $151 / 2\left(l_{1}+1_{15}\right)$ |  | 2.5 |  | $\mu \mathrm{A}$ |
| ICC Supply current | Pin 14 |  | 4 |  | $\mu \mathrm{A}$ |
| $I_{B}$ Input bias current <br> $I_{B}$ Input bias current | Pin 2 Pins 5 and $13 \quad 1 / 2\left(I_{5}+I_{13}\right)$ |  | $\begin{gathered} 200 \\ 2 \end{gathered}$ |  | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| ICC Supply current | Pin 10, no signal |  | 4 |  | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{B}} \quad$ Bias current | Pin 7 |  | 150 |  | $\mu \mathrm{A}$ |
| Avol Open loop gain (Preamplifier) |  | 65 | 80 |  | $d B$ |
| Output transistor <br> Output amplifier Avol $\qquad$ Open loop voltage gain |  | 2.5 | 54 |  | $\mathrm{mA}$ <br> dB |
| Pout Output power |  |  | 450 |  | mW |
| Preamplifier  <br> $N_{F}$ Noise figure <br> $\mathrm{BW}_{W}$ Unity gain bandwidth | $\mathrm{R}_{\mathrm{S}}=5 \mathrm{~K} \Omega, \mathrm{BW}=300 \text { to } 4 \mathrm{KHz}$ <br> 6dB/octave compensation |  | $\begin{gathered} 4 \\ 10 \end{gathered}$ |  | dB <br> MHz |
| Output amplifier <br> THD Total distortion | $f=1 \mathrm{KHz}, \mathrm{Po}=50 \mathrm{~mW}, \mathrm{R}_{\mathrm{L}}=75 \Omega$ |  | 1.5 |  | \% |

NOTE
$V+=12$ volts, $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified

TYPICAL APPLICATION


TYPICAL PERFORMANCE CHARACTERISTICS


ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{P}}=12 \mathrm{~V}$

| PARAMETER | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: |
|  | Min | Typ | Max |  |
| PRE-AMPLIFIER |  |  |  |  |
| Po Output power at $R_{L 1}=800 \Omega$ |  |  | 2, 5 | mW |
| B Bandwidth (-3dB) |  |  | 4 | kHz |
| $\mathrm{I}_{14}$ Total current |  |  | 4, 0 | mA |
| $V_{i 1} \quad$ Input signal |  |  | 1, 5 | mV |
| $\left\|Z_{i}\right\| \quad$ Input impedance |  |  | 500 | $\Omega$ |
| OUTPUT AMPLIFIER |  |  |  |  |
| $\mathrm{P}_{0} \quad$ Output power at $\mathrm{R}_{\mathrm{L} 2}=25 \Omega$; $\mathrm{d}_{\text {tot }}=5 \%$ |  |  | 500 | mW |
| Po at $R_{L 2}=15 \Omega ; d_{\text {tot }}=5 \%$ |  |  | 800 | mW |
| B Bandwidth ( -3 dB ) |  |  | 4 | kHz |
| $\mathrm{d}_{\text {tot }}$ Total distortion at $\mathrm{P}_{\mathrm{O}}=50 \mathrm{~mW}$ |  |  | 1,5 | \% |
| $V_{i 2} \quad$ Input signal |  |  | 260 | mV |
| $\left\|Z_{i}\right\| \quad$ Input impedance |  |  | 1, 3 | $k \Omega$ |
| $\mathrm{I}_{10}$ Total current (dc; no signal; pin 10) |  |  | 4 | mA |

## DESCRIPTION

The TCA580 is a monolithic integrated gyrator circuit with floating inputs. It is intended mainly to replace the coils in telephony low-pass filters. The simulated inductance consists of the IC, two resistors

## FEATURES

- Frequency range dc to 10 kHz
- Q's of 500 to $\mathbf{5 0 0 0}$
- Operating temperature range -20 to $+70^{\circ} \mathrm{C}$
- Efficiency of 1.4\% $\mathrm{R}_{\mathrm{g} 1}$ and $\mathrm{Rg}_{\mathrm{g} 2}$ and a capacitor C 2 . With this configuration, inductances of up to $1 \mathrm{MH} \pm$ $2 \%$ can be achieved.


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| $\mathrm{V}+$ to V - | Supply voltages | 14 |
| $\pm \mathrm{V}_{\text {IC }}$ | Common mode input voltage | 14 |
| $\pm \mathrm{V}$ ID | Differential input voltage | 14 |
| TSTG | Storage temperature | V |
| TAMB | Operating ambient temperature | -55 to +125 |

PIN CONFIGURATIONS


## BLOCK DIAGRAMS



DC ELECTRICAL CHARACTERISTICS $\mathrm{T}_{\mathrm{A}} 25^{\circ} \mathrm{C}, \mathrm{V}+=4.4 \mathrm{~V}, \mathrm{~V}-=-7.6 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TCA580N |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Ip | Supply current |  | $\mathrm{RP}=50 \mathrm{k} \Omega$ |  | 0.8 |  | mA |
| n | Efficiency | (Signal Power $\div$ Supply Power) |  | 1.4 |  | \% |
| $\Delta \mathrm{L}$ | Inductor tolerance |  |  | $\pm 0.2$ |  | \% |
| Q | Quality factor | Pin 11 grounded, $\mathrm{f}=200 \mathrm{~Hz}, \mathrm{Rg}_{\mathrm{g} 1}=\mathrm{Rg}_{\mathrm{g} 2}=10 \mathrm{k} \Omega$ | 500 |  | 5000 |  |
| VOUT | Output voltage (peak) |  |  |  | 1.6 | V |
| Vos | Input offset voltage |  |  |  | 25 | mV |
| los | Input offset current |  |  |  | 9 | $\mu \mathrm{A}$ |

## EQUIVALENT SCHEMATIC



TYPICAL PERFORMANCE CHARACTERISTICS


## TYPICAL CONNECTION



The values for $L$ and $f_{\text {res }}$ in the circuit above are:
$L=R_{G 1} R_{G 2} C_{2}=8.2 \mathrm{H}$
$f_{\text {res }}=\frac{1=194 \mathrm{~Hz}}{2 \pi \sqrt{R_{G 1} R_{\mathrm{G} 2} \mathrm{C} 1 \mathrm{C} 2}}$
Figure 1

## TYPICAL APPLICATIONS

Circuit and response of a low-pass filter with three TCA580 gyrators.


## DESCRIPTION

The TCA980 is a monolithic integrated microphone amplifier. It is primarily intended for use with low-impedance microphones in telephone systems. The output of the amplifier is $22 \mathrm{mV} / \mu$ bar when used with a microphone having an impedance of $200 \Omega$ and a sensitivity of $100 \mu \mathrm{~V} / \mu$ bar. A capsule assembly containing the TCA980, a lowimpedance microphone and a $0.22 \mu \mathrm{~F}$ capacitor can directly replace a carbon microphone. The dc supply to the device may be of either polarity.

FEATURES

- Voltage gain - 220V/V
- Noise voltage 1.3 mVrms
- Single supply operation


## PIN CONFIGURATIONS



NOTES

1. Superimposed on 100 mA (dc)
2. See derating curve.

EQUIVALENT SCHEMATIC


DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$, Test Figure 1 unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TCA980 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\mathrm{V}_{\mathrm{cc}}$ | Supply voltage drop |  | $\pm \mathrm{I}_{2}=10 \mathrm{~mA}$ | 3.5 |  | 5.75 | v |
|  |  | $\pm 2_{2}=30 \mathrm{~mA}$ | 4.45 |  | 6.75 | V |
|  |  | $\pm \mathrm{l}_{2}=60 \mathrm{~mA}$ | 5.0 |  | 7.8 | v |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$, Test Figure 1 unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TCA980 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Avol | Voltage gain |  | Test Figure 1, $\mathrm{f}=2 \mathrm{kHz}, \mathrm{l}_{2}= \pm 30 \mathrm{~mA}$ Test Figure $1, f=2 \mathrm{kHz}, \mathrm{I}_{2}= \pm 10 \mathrm{~mA}$ | $\begin{aligned} & 190 \\ & 160 \end{aligned}$ | 220 | $\begin{aligned} & 260 \\ & 260 \end{aligned}$ | $\begin{aligned} & \mathrm{V} / \mathrm{V} \\ & \mathrm{~V} / \mathrm{V} \end{aligned}$ |
| $\triangle \mathrm{AvOL}$ | Voltage gain change | $\begin{gathered} -20^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 55^{\circ} \mathrm{C} \\ 300 \mathrm{~Hz} \leq \mathrm{f} \leq 2 \mathrm{kHz} \end{gathered}$ |  | 1 | $\begin{gathered} 10 \\ 3 \end{gathered}$ | $\begin{gathered} \% \\ \text { dB } \end{gathered}$ |
| VOUT | Output voltage | $\begin{aligned} & \mathrm{f}=2 \mathrm{kHz}, \text { dтOT }<5 \%(\mathrm{rms}), \mathrm{I}_{2}= \pm 10 \mathrm{~mA} \\ & \mathrm{f}=2 \mathrm{kHz}, \text { dтOT }<5 \%(\mathrm{rms}), \mathrm{I}_{2}= \pm 30 \mathrm{~mA} \\ & \mathrm{f}=2 \mathrm{kHz}, \text { dтOT }<5 \%(\mathrm{rms}), \mathrm{I}_{2}= \pm 60 \mathrm{~mA} \end{aligned}$ | $\begin{gathered} \hline 1 \\ 1.35 \\ 1 \\ \hline \end{gathered}$ | 1.5 |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| $V_{N}$ Rout | Output noise voltage Output impedance | $\begin{aligned} & \mathrm{BW}=.3 \mathrm{kHz} \text { to } 4 \mathrm{kHz} \\ & \mathrm{f}=2 \mathrm{kHz}, \mathrm{I}_{2}= \pm 30 \mathrm{~mA} \end{aligned}$ |  | 150 | 1.3 | mVrms $\Omega$ |

TYPICAL PERFORMANCE CHARACTERISTICS


TEST LOAD CIRCUITS


## DESCRIPTION

The TDA1024 is a monolithic integrated circuit intended for use in ON/OFF control of triacs in static switching applications. It incorporates zero voltage point triggering to minimize radio interference.
The TDA1024 is mainly intended for applications such as switching resistive loads and replacing mechanical thermostats in, for example:
Central heating installations,
Washing machine heaters,
Water heaters,
Smoothing irons.
Functions of the TDA1024 are:

1. A comparator with Schmitt-trigger action.
This circuit compares the control voltage at pin 5 with the reference voltage at pin 4 and switches on when the control voltage exceeds the reference voltage. The hysteresis of the circuit is adjustable between 20 mV and 300 mV by selection of the value of a resistor connected between pin 3 and pin 1.
2. An input buffer circuit with high input impedance and low output impedance. This circuit presents a low impedance to the comparator input so that the hysteresis of the circuit is independent of variations of the input voltage.
3. A control circuit dc supply which provides a zener-limited nominal 6.5 V supply, at a current of up to 30 mA , for application to the input bridge.
4. A zero-crossing detector which produces an output when the sinusoidal voltage applied to pin 6 passes through zero; advantage of this mode in minimum radio interference.
5. A control gate which inhibits the output trigger pulse from the TDA1024 unless there are outputs from both zerocrossing detector and comparator.
6. An output stage which delivers a positivegoing, mains-synchronized triac trigger pulse whenever the control gate is activated. The output from this stage is current-limited and protected against short-circuit. Since the current and voltage in the load must be in phase for mains-synchronized switching, the applications of the TDA1024 are restricted to the switching of resistive loads.

## FEATURES

- Trigger current $>100 \mathrm{~mA}$
- Supply derived from ac lines
- Adjustable hysteresis
- Minimum of external components


## BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| PARAMETER |  | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| Vcc | Supply voltage (pin 7) | 8 | V |
| VIN | Max applied voltage (pin 2, 3, 4,5 \& 8 reference to pin 1) | 8 | V |
| Icc | Supply current (pin 7) average | 30 | mA |
| Icc | Supply current (pin 7) peak | 80 | mA |
|  | Max current pins 4, 5, \& 6 | 10 | mA |
|  | Non-repetitive peak current (pin 7) $\quad T_{p}<50 \mu \mathrm{~S}$ | 2 | A |
| Iout | Output current (pin 2) average | 30 | mA |
| Iout | Output current (pin 2) peak $\mathrm{T}_{\mathrm{p}}<300 \mu \mathrm{~S}$ | 400 | mA |
| Tsg | Storage temperature | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {A }}$ | Operating ambient temperature | -20 to +80 | ${ }^{\circ} \mathrm{C}$ |
| PD | Power dissipation <br> Lead temperature (soldering, 10sec) | See derating curve 300 | ${ }^{\circ} \mathrm{C}$ |

## EQUIVALENT SCHEMATIC



## DC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TEST CONDITIONS | TDA1024 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Iout | Trigger output <br> Trigger output current |  | $\mathrm{V}_{8-1}=5.5 \mathrm{~V}$ | 100 |  |  | mA |
| $\mathrm{V}_{2-1}$ | Trigger output voltage | Iout $=100 \mathrm{~mA}$ | 4 |  |  | V |
| $\begin{aligned} & 1_{4} \\ & 15 \end{aligned}$ | Comparator Input current pin 4 Input current pin 5 | $\mathrm{V}_{4-1}>\mathrm{V}_{5-1}$ |  |  | $\begin{aligned} & 5 \\ & 5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \\ & \hline \end{aligned}$ |
| $\mathrm{V}_{8}$ | Control circuit dc supply (pin 8) | $17=10 \mathrm{~mA}$ | 5.5 | 6.5 | 7.5 | V |
| Icc <br> Icc | Supply current Supply current | $V_{5-1}>V_{4-1}, V_{8-1}=5.5 \mathrm{~V} \text {, pins } 2 \&$ 3 open minimum hysteresis Pin 2 open, pin $3=0 V, V_{5-1}>\mathrm{V}_{4-1}$ $\mathrm{V}_{8-1}=5.5 \mathrm{~V}$ maximum hysteresis |  |  | 1.8 3 | mA mA |

## AC ELECTRICAL CHARACTERISTICS

|  | PARAMETER | TEST CONDITIONS | TDA1024 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Ttrigger | Trigger pulse width | $\mathrm{I}_{6}=1 \mathrm{~mA}, \mathrm{~V}_{8-1}=5.5 \mathrm{~V}$ | 130 | 195 | 265 | $\mu \mathrm{S}$ |
| $\begin{aligned} & \Delta V_{5-4} \\ & \Delta V_{5-4} \end{aligned}$ | Comparator hysteresis Comparator hysteresis | $\begin{gathered} \text { Pin } 3 \text { open, } I_{3}=0 \\ V_{3}=0 \end{gathered}$ | 10 | 300 | 30 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |

TYPICAL PERFORMANCE CHARACTERISTICS

TRIGGER PULSE WIDTH vs SYNCHRONIZATION RESISTOR


Use Test Circuit CKT 1

AVAILABLE TRIGGER CURRENT


Use Test Circuit 3


Use Test Circuit CKT 2

AVAILABLE TRIGGER CURRENT


Use Test Circuit 3

TYPICAL PERFORMANCE CHARACTERISTICS


MINIMUM REQUIRED SUPPLY CURRENT


DROPPING RESISTOR POWER DISSIPATION USING DROPPING CAPACITOR



MAXIMUM SERIES RESISTANCE AS A FUNCTION OF REQUIRED SUPPLY CURRENT


POWER DISSIPATION DERATING CURVE


## TEST LOAD CIRCUITS



Use Test CKT 4. Minimum required supply current ( $\left(1_{7}\right)$ as a function of maximum average trigger current $\left.{ }^{( } I_{2(a v)}\right)$, with hysteresis setting as a parameter.
$\mathrm{I}_{3}=0 ; \mathrm{min}$. hysteresis.
$\mathrm{V}_{3}=0$; max. hysteresis.


COMPONENT VALUES AND CIRCUIT PARAMETERS

|  | PARAMETER | VALUE |  | TEST CIRCUIT |
| :---: | :---: | :---: | :---: | :---: |
|  |  | FIG. 1 | FIG. 2 |  |
| $t_{p}(\mu s)$ | Trigger pulse width | 105 | 105 |  |
| $\mathrm{R}_{\mathrm{S}}(\mathrm{k} \Omega)$ | Sync. resistor | 180 | 180 | 1 |
| $\left.\mathrm{RGG}^{( } \Omega\right)$ | Gate resistor | 33 | 33 | 2 |
| I2(av)(mA) | Average gate current | 3.7 | 3.7 | 3 |
| $17(\mathrm{~mA})$ | Min. required supply current | 6.5 | 6.5 | 4 |
| $\mathrm{R}_{\mathrm{d}}(\mathrm{k} \Omega)$ | Mains dropping resistor | 10 | - | 5 |
| $\mathrm{C}_{\mathrm{s}}(\mu \mathrm{F})$ | Smoothing capacitor | 470 | 470 | 5 |
| $\mathrm{C}_{\mathrm{d}}(\mathrm{nF})$ | Mains dropping capacitor | - | 270 | 6 |
| $\mathrm{P}_{\text {Rsd }}(\mathrm{mW})$ | Power dissipated by $\mathrm{R}_{\text {sd }}$ | - | 190 | 6 |

[^5]
## TYPICAL APPLICATIONS



NOTES

1. Spike suppressor (VDR): $350 \mathrm{~V} / 1 \mathrm{~mA}(2322594$ 13512)
2. $R_{25}=22 \mathrm{k} \Omega$

The TDA1024 used in a 1200 W thermostat covering the temperature range $5^{\circ} \mathrm{C}$ to $30^{\circ} \mathrm{C}$ and designed to minimize the power dissipated by mains dropping resistor $R_{d}$ by using a rectifier diode.

Figure 1


Figure 2

## DESCRIPTION

The TDA1060 is a monolithic integrated circuit intended for the control of switched mode power supplies. It incorporates all the control and protection functions likely to be required in switched mode power supplies for professional equipment.

## FEATURES

- Stabilized power supply
- Temperature compensated voltage reference
- Sawtooth generator
- Pulse width modulator
- Remote ON/OFF switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/over voltage protection
- Maximum duty cycle adjustment
- External synchronization input
- Feed forward


## FUNCTIONAL DESCRIPTION

A. Stabilized Power Supply

The circuit can be fed either by a current source (e.g. connected to the high voltage input of the SMPS via a series resistor), or a voltage source (e.g. a $12 \mathrm{Vbat-}$ tery). When fed from a 12 V supply the maximum current consumption is 10 mA .
The stabilized voltage is typically 8.4 V and is available on pin 2 for supplying external circuitry. Up to 5 mA can be drawn from this supply whereupon the total IC current consumption increases by the same amount. This stabilized supply is protected against short circuits.

## B. Reference Voltage Source

The reference voltage for the SMPS is incorporated in the IC. The temperature stability of this reference is $\pm 100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ maximum.

## C. Sawtooth Generator and Feed Forward

The frequency of the sawtooth generator is set by an external resistor (pin 7) and a capacitor (pin 8). The frequency can be determined with the aid of Figure 3. It may be set between 50 Hz and 100 KHz and is virtually independant of supply voltage.
The upper and lower levels of the sawtooth are fixed by an internal resistor divider. Since these resistors form a bridge configuration with the external voltage divider for the $\delta$-max setting; the accuracy of the $\delta$-max setting is deter-
mined by resistor matching rather than by absolute values.
During the flyback of the sawtooth the output pulse is inhibited. This acts as an internal duty cycle limiter. Since the flyback time is $1 \mu \mathrm{~s}$ (with 1 nF capacity), the maximum duty cycle is limited to $95 \%$ at 50 KHz .
The frequency of the sawtooth can be synchronized via the TTL-compatible input on pin 9. The synchronizing frequency must be lower than the oscillator free running frequency. When the input on pin 9 is Low the sawtooth generator is stopped, starting again when the input goes High. For free-running operation pin 9 is left dissconnected.

Feed forward can be provided via pin 16 which has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on pin 16 increased the upper level of the sawtooth is also increased. Since neither the $\delta$-max voltage level nor the feedback voltage are influenced by the feed forward; the duty cycle reduces. This is a linear function and can therefore compensate for supply voltage variations. If feed forward is not required pin 16 should be connected to pin 12.

## D. Feedback Amplifier

The difference between the feedback voltage ( pin 3 ) and the internal reference voltage is amplified in an operational amplifier. The output signal is compared with the sawtooth which has an amplitude of typically 4.5 V (without feed forward).
The gain can be controlled by a feedback circuit from the op. amp. output (pin 4). To avoid instability a capacitor should be connected across the op amp (i.e. between pins 3 and 4).

## E. Remote ON/OFF

Remote switching can be provided through the TTL-compatible input on pin 10. When this input is Low the circuit is switched off. With the input High the circuit switches on via the slow start procedure.

## F. Current Limiter

The current limiter comprises two comparators with trip-on levels of 480 mV and 600 mV respectively. When the voltage on the current sense input (pin 11) exceeds 480 mV , the output pulse is immediately cut off, starting again at the next period. If the voltage exceeds 600 mV , the output pulse is inhibited during a certain

## PIN CONFIGURATION


"dead time", during which the slow start capacitor is unloaded. After this the circuit starts again with slow start.

## G. Low Supply Voltage Protection

When the supply voltage is too low (less than $\mathrm{Vz}+0.2 \mathrm{~V}$ ) the circuit is automatically switched off. Starting takes place again via the slow start as soon as the supply voltage exceeds this threshold value.

## H. Feedback Loop Fault Protection

If the feedback loop is open, the feedback input (pin 3) is pulled high by an internal current source making the duty cycle zero. If the feedback loop is shortcircuited, or if the feedback voltage does not exceed 600 mV , the $\delta$-max pin is connected to the lower level of the sawtooth by a $1 \mathrm{k} \Omega$ resistor. This causes a lower $\delta$-max voltage as described in the maximum duty cycle and slow start section.

## I. Output

The output circuit comprises a latch and an output transistor. Both collector and emitter of the output transistor are available on pins 15 and 14 respectively. The collector is internally connected to the supply voltage of the integrated circuit by a clamping diode to limit the output voltage in the case of a fault in the external drive circuit of the switching transistor.

## J. Demagnetisation/Overvoltage

The demagnetisation/overvoltage input (pin 13) inhibits the output when the voltage at this pin exceeds the trip-on level of 600 mV . The combined function can be realized by a zener diode from the output voltage of the SMPS to this pin (e.g. a 5.6 zener in a 5 V supply) and the demagnetisation sensor connected also directly to this point.

## K. Maximum Duty Cycle and Slow Start

The voltage on pin 6 ( $\delta$-max setting) determines the maximum output duty ratio. As explained in section C the $\delta$ max setting accuracy is very good since the voltage at this pin is divided by a resistive divider from the Vz voltage.

In the event of a loop fault the $\delta$-max pin is connected via an internal $1 \mathrm{k} \Omega$ resistor to the lower limit of the sawtooth voltage. Thus the $\delta$-max value is decreased to a level determined by the impedance of the $\delta$-max resistive divider to the internal $1 \mathrm{k} \Omega$.

The capacitor connected to the $\delta$-max pin, together with the impedance of the resistive divider, determines the time constant for the slow start. For remote ON/OFF or when the current sensing voltage exceeds 600 mV , the value of the capacitor determines the dead time of the slow start procedure.

## L. Modulation Input

Pin 5 gives an input to the pulse width modulator which may be used for current mode regulation. The duty cycle reduces when the voltage at this point decreases.

## BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| PARAMETER |  | RATING |  | UNIT |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $\begin{aligned} & \mathrm{V}_{\mathrm{Cc}} \\ & \mathrm{Icc} \end{aligned}$ | Supply voltage | -0.5 | 18 | V |
|  | Supply current | 0 | 30 | mA |
|  | Output current | 0 | 40 | mA |
|  | Voltages at the pins with respect to pin 12 |  |  |  |
|  | Feed forward (pin 16) | 0 | V+ | V |
|  | Output emitter (pin 14) | 0 | 5 | V |
|  | Output collector (pin 15) | 0 | V+ | V |
|  | All other inputs | 0 | Vz | V |
|  | Storage temperature | -25 | +125 | ${ }^{\circ} \mathrm{C}$ |
|  | Operating temperature | -25 | +85 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{S}=12 \mathrm{~V}$ (VP) unless otherwise specified. $1,2,3,4,5$

| PARAMETER |  |  | TEST CONDITIONS | TDA1060 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| VIN $V_{z}$ | Pin 1 <br> Pin 1 <br> Pin 2 | Input voltages |  | Current FED $\mathrm{I}_{1}=10 \mathrm{~mA}$ <br> Current FED $I_{1}=30 \mathrm{~mA}$ | $\begin{aligned} & 20 \\ & 20 \\ & 7.8 \end{aligned}$ | $\begin{aligned} & 21 \\ & 25 \\ & 8.4 \end{aligned}$ | $\begin{aligned} & 23 \\ & 30 \\ & 9.0 \end{aligned}$ | $\begin{aligned} & V \\ & V \\ & V \end{aligned}$ |
| $\Delta \mathrm{V}$ z/temp. |  | $V_{z}$ drift |  | -1.3 |  | 1.3 | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
|  | Pin 10 <br> Pin 10 | Remote ON/OFF2 Remote ON/OFF2 | Circuit ON Circuit OFF | $\begin{aligned} & 2 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & V_{z} \\ & 0.8 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
|  | $\begin{aligned} & \text { Pin } 11 \\ & \text { Pin } 11 \end{aligned}$ | Inhibit Start | Single pulse inhibit Shutdown/slow start | $\begin{aligned} & 0.76 \\ & 470 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 600 \end{aligned}$ | $\begin{aligned} & 0.84 \\ & 720 \end{aligned}$ | $\begin{gathered} \mathrm{V}_{11} \text { (Start) } \\ \mathrm{mV} \end{gathered}$ |
|  | Pin 3 | Feedback loop protection | Trip on | 470 | 600 | 700 | mV |
|  | Pin 14 Pin 14-15 | Maximum emitter voltage Saturation voltage | $\mathrm{I}_{15}=40 \mathrm{~mA}$ | 5 |  | 400 | $\begin{gathered} \mathrm{V} \\ \mathrm{mV} \end{gathered}$ |
|  | Pin 13 | Over voltage input ${ }^{4}$ | Trip on level | 470 | 600 | 720 | mV |
|  | Pin 6 | $\delta$-max voltage level | Duty cycle $=50 \%(15-50 \mathrm{kHz})$ | 0.38 Vz | 0.4 V z | 0.42 V z | V |
|  | Pin 9 <br> Pin 9 | Synchronization input Synchronization input | Sawtooth stopped Sawtooth running | $\begin{aligned} & 0 \\ & 2 \end{aligned}$ |  | $\begin{aligned} & 0.8 \\ & V_{z} \end{aligned}$ | $\begin{aligned} & V \\ & V \end{aligned}$ |
| VREF $\Delta V_{\text {REF }}$ | Reference | oltage |  | 3.42 | 3.72 | 4.03 | V |
|  | Temperatu of referen Lower saw Upper saw | coefficient voltage ooth level ooth level |  | -100 | $\begin{aligned} & 1.1 \\ & 5.6 \end{aligned}$ | 100 | $\begin{gathered} \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \mathrm{~V} \\ \mathrm{~V} \end{gathered}$ |
| VPT $\Delta V_{P T}$ | Supply vo Supply vo Temperatu | ge protection ge protection coefficient | Trip-on level | $\begin{gathered} V_{z}+.2 \\ -6.5 \end{gathered}$ |  | $\mathrm{V} z+1.7$ | $\begin{gathered} \mathrm{V} \\ \mathrm{mV} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| IIN | Input curr Pin 1 Pin 2 | ts <br> Supply current <br> Maximum allowable external current drain | Voltage FED | 5 |  | $\begin{gathered} 10 \\ 5 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
|  | Pin 3 <br> Pin 10 | Input current Sink current ${ }^{2}$ | $V_{10}=0$ |  | -40 | -90 | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
|  | Pin 11 <br> Pin 15 | Input current <br> Available output current | $\mathrm{V}_{11}=250 \mathrm{mV}$ | 40 |  | 12 | $\begin{array}{r} \mu \mathrm{A} \\ \mathrm{~mA} \\ \hline \end{array}$ |
| IIN | Pin 13 <br> Pin 6 <br> Pin 16 | Input currents Input current ${ }^{4}$ Input current Input current | $\begin{gathered} V_{13}=250 \mathrm{mV} \\ V_{6}=1 \mathrm{~V} \end{gathered}$ |  |  | $\begin{gathered} 10 \\ 20 \\ 5 \end{gathered}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
|  | $\begin{aligned} & \text { Pin } 9 \\ & \operatorname{Pin} 5 \end{aligned}$ | Sink current Input current | $\begin{gathered} V_{9}=0 \\ V_{5}=1 V \end{gathered}$ |  |  | $\begin{aligned} & -90 \\ & -40 \\ & \hline \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| $\begin{aligned} & \mathrm{R} \\ & \mathrm{R} \end{aligned}$ | Sawtooth resistor value Amplifier resistor value |  |  | $\begin{gathered} 10 \\ 100 \end{gathered}$ |  | 40 | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| Avol | Amplifier Internal du <br> $\delta$-max sett | en loop gain cycle limiting g | Period time $T \mu \mathrm{~S}$ $c=1 \mathrm{nF}$ | 0 | 60 | $\begin{aligned} & (T-1) / T \\ & (T-1) / T \end{aligned}$ | dB |

NOTES

1. The remote ON/OFF is not active when this pin is not connected.
2. The synchronization is not active when this pin is not connected.
3. The demagnetisation/overvoltage protection is active when this pin is not connected.
4. The current limiter is active when this pin is not connected.
5. All voltages with respect to pin 9.

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | то | FROM | TEST CONDITIONS | TDA1060 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max |  |
| TD | Delay time |  | Output | Pin 11 | $25 \%$ overdrive, 40 mA output current |  |  | 0.8 | $\mu \mathrm{s}$ |
| F | Sawtooth frequency range |  |  | Figure 3 | 0.05 |  | 100 | kHz |
| $\Delta F / \Delta V$ | Frequency drift with supply |  |  | $8 \leq \mathrm{V} 16 \leq \mathrm{V}+$ |  |  | 2.3 | \% |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL APPLICATION


## sECTION IO DISPLAY DRIVERS

## DESCRIPTION

The DS8880 is a high voltage sevensegment decoder/driver designed to decode BCD and drive gas filled sevensegment display tubes.
Decoding is performed by a $16 \times 7$ read only memory. Thus, for applications desiring other fonts, or applications not using standard BCD inputs, the ROM contents can be altered via metal mask change to produce any seven-segment combination for any 16 binary input combinations.

The output of the ROM is used to drive high voltage constant current sink generators. The current sinks of the DS8880 will withstand 80 V output min. while those of DS8880-1 will withstand 100V. The current sinks are ratioed to the $B$ output current as required for even illumination of the segments. Output currents may be varied over a 0.2 to 1.5 mA range through use of the external current programming input.

Blanking input provides unconditional blanking of any output display, while the ripple blanking pins allow simple leading or trailing zero blanking.

## LOGIC AND CONNECTION DIAGRAMS



## PIN CONFIGURATION

| F,N PACKAGE |  |  |
| :---: | :---: | :---: |
| B Input 1 | 16 | $\mathrm{V}_{\mathrm{Cc}}$ |
| C Input 2 | 15 | f Output |
| Program 3 | 14 | g Output |
| BI/RBO 4 | 13 | a Output |
| RBI 5 | 12 | b Output |
| D Input 6 | 11 | c Output |
| A Input 7 | 10 | d Output |
| GND 8 | 9 | e Output |

- Current source outputs
- High output breakdown voltage-110V
- Suitable for multiplex operation
- Blanking and ripple blanking provisions
- Low fan-in and low power


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| VCC | 7 | V |
| Input voltage | 6 | V |
| Except B1 | VCC |  |
| B1 |  |  |
| Segment output voltage | 80 | V |
| DS8880 | 100 | V |
| DS8880-1 | 600 | mW |
| Power dissipation* | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  |  |
| (soldering, 10 sec ) |  |  |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V} C \mathrm{C}=5 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | DS8880/8880-1 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Logic "1" input voltage Logic "0" input voltage | $\begin{aligned} & V_{C C}=4.75 \mathrm{~V} \\ & V_{C C}=4.75 \mathrm{~V} \end{aligned}$ | 2.0 |  | 0.8 | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| Logic " 1 " output voltage (RBO) Logic " 0 " output voltage (RBO) | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \text { Iout }=-200 \mu \mathrm{~A} \\ \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \text { IouT }=8 \mathrm{~mA} \end{gathered}$ | 2.4 | $\begin{gathered} \hline 3.7 \\ 0.13 \\ \hline \end{gathered}$ | 0.4 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| Logic " 1 " input current (except BI) <br> Logic "0" input current (except BI) <br> Logic " 0 " input current (BI) | $\begin{gathered} V_{C C}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=2.4 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=5.5 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0.4 \\ \mathrm{VCC}^{2} 5.25 \mathrm{~V}, \mathrm{~V}_{\text {IN }}+0.4 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} \hline 2 \\ 4 \\ -300 \\ -1.2 \\ \hline \end{gathered}$ | $\begin{gathered} 15 \\ 400 \\ -600 \\ -2.0 \\ \hline \end{gathered}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> mA |
| Power supply current | $\mathrm{V}_{\mathrm{cc}}=5.25 \mathrm{~V}$, all inputs $=0 \mathrm{~V}, \mathrm{Rp}=2.2 \mathrm{k}$ |  | 27 | 43 | mA |
| Input diode clamp voltage | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{l}_{\mathrm{I}}=-12 \mathrm{~mA}$ |  | -0.9 | -1.5 | V |
| Segment outputs: <br> Outputs a, f,g on current ratio <br> Output c on current ratio <br> Output d on current ratio <br> Output e on current ratio | All outputs $=50 \mathrm{~V}$, output b curr. $=$ ref. <br> All outputs $=50 \mathrm{~V}$, output b curr. $=$ ref. <br> All outputs $=50 \mathrm{~V}$, output b curr. $=$ ref. <br> All outputs $=50 \mathrm{~V}$, output b curr. $=$ ref. | $\begin{aligned} & 0.84 \\ & 1.12 \\ & 0.90 \\ & 0.99 \end{aligned}$ | $\begin{aligned} & 0.93 \\ & 1.25 \\ & 1.00 \\ & 1.10 \end{aligned}$ | $\begin{aligned} & 1.02 \\ & 1.38 \\ & 1.10 \\ & 1.21 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Output b on current |  | $\begin{aligned} & \hline 0.15 \\ & 0.45 \\ & 0.90 \\ & 1.35 \end{aligned}$ | $\begin{aligned} & 0.20 \\ & 0.50 \\ & 1.00 \\ & 1.50 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 0.55 \\ & 1.10 \\ & 1.65 \end{aligned}$ | mA <br> mA <br> mA <br> mA |
| Output saturation voltage | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \text { lout }=2 \mathrm{~mA}, \\ \mathrm{Rp}=1 \mathrm{k} \pm 5 \% \end{gathered}$ |  | 0.8 | 2.5 | V |
| Output leakage current: <br> DS8880 <br> DS8880-1 | $\begin{aligned} & V_{\text {OUT }}=75 \mathrm{~V}, \mathrm{BI}=0 \mathrm{~V} \\ & \mathrm{~V}_{\text {OUT }}=95 \mathrm{~V}, \mathrm{BI}=0 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & .003 \\ & .005 \\ & \hline \end{aligned}$ | 3 3 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Output breakdown voltage: DS8880 DS8880-1 | lout $=250 \mu \mathrm{~A}, \mathrm{BI}=0 \mathrm{~V}$ | $\begin{gathered} 80 \\ 100 \\ \hline \end{gathered}$ | $\begin{array}{r} 110 \\ 110 \\ \hline \end{array}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| Propagation delays: BCD input to segment output BI to segment output RBI to segment output RBI to RBO | $\begin{aligned} & V_{C C}=5 V \\ & V_{C C}=5 V \\ & V_{C C}=5 V \\ & V_{C C}=5 V \end{aligned}$ |  | $\begin{aligned} & 0.4 \\ & 0.4 \\ & 0.7 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 10 \\ & 10 \\ & 10 \\ & 10 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{S} \\ & \mu \mathrm{~S} \\ & \mu \mathrm{~S} \\ & \mu \mathrm{~S} \\ & \hline \end{aligned}$ |

*NOTE
$\mathrm{Min} /$ max limits apply across the guaranteed operating temperature range of $0^{\circ} \mathrm{C}$ to
$70^{\circ} \mathrm{C}$ unless otherwise specified. Positive current is defined as current into the referenced pin.

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL APPLICATION


## PRELIMINARY SPECIFICATION

Contact factory for product status.

## DESCRIPTION

The NE580 is a dual bar-graph logic circuit designed to provide all the functions necessary to drive a gas discharge self-scan ${ }^{(1)}$ bar-graph panel. The NE580 is configured to drive a 201 element bar-graph in either 5 or 6 phase operation. Phase number selection is obtained by applying a logic 0 or 1 level to the phase select pin. 3 phase operation for a 101 element device can be attained by a wire-or connection of adjacent cathode phase outputs.

The device inputs accept an analog voltage in the range 0 to 2.5 V and performs an $A / D$ conversion with reference to a fixed input voltage at the reference terminal. On-chip functions include a clock generator, linear ramp generator, control logic and ROM decoding. Output functions comprise 2 anode control lines, 2 overrange indication outputs, 6 cathode phase outputs and 1 cathode reset output. Refer to the system block diagram for clarification.
A minimum of external components are required for the whole conversion and display system shown in the typical application. The NE580 can be expanded to handle more analog channels using external comparators. Either LM393A or LM339A type comparators will function well. A few external low-cost logic packages can in addition provide binary or BCD encoded data to interface with a logic control system.

The device is supplied in a 22 -pin plastic molded or ceramic dual-in-line package.
(5)-self-scan is a trademark of Burroughs Corporation.

## FEATURES

- Dual channel device
- Easily expandable to handle more channels.
- Single 5 volt supply
- 3,5 or 6 phase operation
- Can be custom masked for different cathode segment counts, (maximum 240)
- Equivalent 8 -bit resolution of displayed information.
- Overrange indication outputs.

PIN CONFIGURATION


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage, VCC | +7 | V |
| Output voltage (all outputs) | +VCC | V |
| Analog input voltage range | -0.3 to +7 | V |
| Reference voltage input | +VCC | V |
| Phase select input | +5.5 | V |
| Analog/digital ground voltage | $\pm 0.3$ | V |
| differential |  |  |
| Power dissipation | 500 | mW |
| plastic | 800 | mW |
| cerdip* | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | 300 | ${ }^{\circ} \mathrm{C}$ |
| Soldering temperature |  |  |

*NOTE
The plastic 22 pin package has a thermal impedance $\theta_{J A}$ of $120^{\circ} \mathrm{C} / \mathrm{W}$ and the cerdip package, $\theta_{\mathrm{JA}}$ of $75^{\circ} \mathrm{C} / \mathrm{W}$. Provided the maximum junction temperature is kept below $150^{\circ} \mathrm{C}$ then more power may be dissipated to a maximum of 1 watt.

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=5 \mathrm{~V}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
|  | Operating supply voltage range |  | 4.75 | 5.0 | 5.25 | V |
| VIN <br> VREF | Input voltage range <br> Applied reference voltage ${ }^{1}$ |  | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & 2.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| IBREF <br> IIB | Bias current at reference voltage input Bias current at analog input | $\begin{aligned} V_{\text {REF }} & =2.5 \mathrm{~V} \\ V_{\text {REF }} & =2.5 \mathrm{~V} \\ V_{\text {IN }} & =0 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 500 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & \text { nA } \\ & \text { nA } \end{aligned}$ |
| Vout (1) | All outputs2 | Iout $=-500 \mu \mathrm{~A}$ |  | 3.5 |  | V |
| IOUT (1) lout (sc) | All outputs ${ }^{2}$ All outputs? | $\begin{gathered} \mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} \\ \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & -1.0 \\ & -1.5 \end{aligned}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Vout (0) | All outputs | $\mathrm{I}_{\text {SINK }}=1.6 \mathrm{~mA}$ |  |  | 0.4 | V |
| FC | Clock generator frequency | Timing capacitor $=.022 \mu \mathrm{~F}$ |  | 25 |  | KHz |
| Accuracy |  | $\begin{gathered} 2 \mathrm{~V} \leq \mathrm{V}_{\text {REF }} \leq 2.5 \mathrm{~V} \\ \mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {REF }} \\ \hline \end{gathered}$ |  | $\pm 1$ |  | bar |
| Icc | Supply current |  |  | 50 |  | mA |

NOTES

1. Displayed accuracy is a function of reference voltage. Values of $V_{\text {REF }}$ below 2 volts will
impair conversion accuracy.
2. All logic outputs comprise an NPN transistor with $3 \mathrm{k} \Omega$ pull-up resistor to 5 volts.

BLOCK DIAGRAM


TIMING DIAGRAM


TYPICAL APPLICATION


## BAR-GRAPH SYSTEM OPERATION

The bar-graph display is a thick-film planar, gas discharge device. The principal of operation is called self-scan ${ }^{\top} \mathrm{M}$, in which a neon glow-discharge is propagated from one cathode spot to another under one anode. The bar-graph device appears as a series of cathode bars arranged in a column. A glow discharge is continually propagated along the column from a keep-alive cathode at one end. Provided the scan rate for a whole column is above the eye flicker detection rate, then the glow appears as a continuous column of light.

## BAR-GRAPH SIGNAL REQUIREMENTS

The NE580 comprises most of the electronic components necessary to interface an analog voltage level to the bar-graph display. Each column of the display requires an anode control signal and each cathode (usually from 4 to 7 in number) requires an interlaced logic signal of $1 / \mathrm{N}$ duty cycle (where N is the number of cathode phases). The pulse width of each cathode signal is of the order of 50 to $100 \mu \mathrm{~s}$. The cathode signals clock continuously throughout the frame period. The anode signal is on only for a proportion of time corresponding to the input voltage.

$$
\begin{aligned}
& \text { Thus } \\
& V_{\text {IN }}=V_{\text {REF }} \times \frac{T_{A N}}{200}
\end{aligned}
$$

for a 200 element device, where TAN is the number of cathode clock cycles for which
the anode is on. Figure 2 illustrates the relative output phasing of the linear ramp cathode and anode lines for 5 phase operation.

## CIRCUIT OPERATION

The NE580 provides the circuitry to generate all these signals to the point where they drive the high voltage display elements. An on-chip clock generator drives the master counter and cathode phase generator.

The clock also gates a constant current source which charges the ramp capacitor with a staircase waveform of equal increment steps. These steps correspond to the cathode segments. There are two steps per segment so that the comparison of input voltage with respect to the ramp is made at the mid-point of each segment. The master counter inhibits the current source and discharges the ramp after 200 cathode counts. At the 200th count, the ramp voltage is strobed into a sample-and-hold amplifier. This voltage is compared with the reference voltage and a signal fed back to the ramp constant current source. Hence, the maximum value of the ramp will be adjusted to the same level as the reference voltage.
The anode output goes low at the beginning of each frame and goes high again when the ramp voltage becomes greater than the input voltage. If the ramp reaches full scale before setting the anode output high, then the over-range output goes low and stays low until the end of the next frame if the input signal recovers to an in-range value. A continuing over-range signal will cause the output to go low indefinitely.

Because the ramp is the result of accumulated charge on the integrating capacitor, it is inherently monotonic; thus, each step is greater than the previous one by the expression

$$
\Delta V=\frac{\Delta Q}{C}
$$

Errors in the ramp can occur due to

1) Starting the ramp from a voltage other than zero. Some capacitors have a time related polarization.
2) Sag in the sampled and hold ramp voltage causing an inconstant charging current.
3) Offset errors in the sample and hold amplifier.
4) Leakage currents into or out of the ramp capacitor.

The zero starting point is achieved by using a very low offset transistor to fully discharge the ramp capacitor to within $1-5 \mathrm{mV}$ of ground. The maximum voltage end of the ramp is made stable by using a large value capacitor to overcome the effects of any leakage.

The classical histogram has cells which represent a nominal value plus/minus $1 / 2$ cell width. The NE580 works in the same way. This is realized by having a clock rate which is twice the cathode switching rate, and so the staircase ramp has two steps per cathode dwell time. Each comparison step is made at the nominal cell value plus $1 / 2$ cell, and the anode remains on (anode output low) as long as the ramp voltage is less than the input voltage.

## DESCRIPTION

The NE582 is a general interface device comprising a high current output transistor and drive circuitry in each of 6 elements. Each output transistor is individually capable of sinking 400 mA with a typical saturation voltage of 0.5 V . Input loading is such that direct interfacing with P-MOS, N-MOS, C-MOS or TTL is possible.
The NE582 has applications as a LED display driver, low voltage relay/lamp drivers and many others where high current capability without speed constraints is required.

The NE582 is supplied in a $16-$ pin high dissipation dual-in-line plastic package.

## FEATURES

- Low saturation voltage (typically 0.5 V ) for minimum power dissipation
- High output sink current capability400mA
- Low input current loading for MOS compatibility
- Low standby power consumption
- Suitable for 3 volt battery operation
- Inputs/outputs are compatible with 75494


## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Input voltage range1 | -12 to $\mathrm{VSS}^{2}$ | V |
| Output voltage ${ }^{2}$ | 10 | V |
| Output to input voltage differential | 10 | V |
| Voltage at VSS (pin 1) | 10 | V |
| Output current-each output | 400 | mA |
| Output current-all outputs | 800 | mA |
| Continuous total power dissipation | 800 | mW |
| at or below $25^{\circ} \mathrm{C} 3$ |  |  |
| Current in VR (pin 9 or 16) | 25 | mA |
| Operating free-air temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature 1/16 inch from | 260 | ${ }^{\circ} \mathrm{C}$ |
| case for 10sec |  |  |

## EQUIVALENT SCHEMATIC



## NOTES

1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above $25^{\circ} \mathrm{C}$, derate power dissipation at $6.25 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$.

ELECTRICAL CHARACTERISTICS $T_{A}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vol | Low level output voltage |  | $$ <br> (Series input resistance) |  | $\begin{aligned} & .025 \\ & .320 \\ & .500 \end{aligned}$ | $\begin{aligned} & .060 \\ & .450 \\ & .750 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| IOH | High level output current | $\begin{aligned} & \mathrm{VOH}_{\mathrm{OH}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{N}}=40 \mu \mathrm{~A} \\ & \mathrm{VOH}_{\mathrm{OH}}=10 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0.5 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & 400 \\ & 400 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| IIN | Input current at maximum Input voltage | $\mathrm{VIN}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{OL}}=20 \mathrm{~mA}, \mathrm{I}_{\mathrm{R}}=2 \mathrm{~mA}$ |  | 2.2 | 3.3 | mA |
| $\begin{aligned} & V_{R} \\ & \text { ISS } \end{aligned}$ | Current into pin 1 | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=6.5 \mathrm{~V}, \mathrm{I}_{\mathrm{R}}=6 \mathrm{~mA}, \mathrm{IOL}^{2}=80 \mathrm{~mA} \\ \mathrm{~V}_{\mathrm{SS}}=10 \mathrm{~V} \end{gathered}$ |  | . 9 | $\begin{aligned} & 1.5 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mu \mathrm{~A} \end{gathered}$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| TPLH | Switching characteristics Propagation delay, low to high level input | $\begin{gathered} R_{R}=680 \Omega \\ R_{L}=39 \Omega \\ C_{L}=15 p F \end{gathered}$ |  | 300 |  | ns |
| TPHL | Propagation delay, high to low level input | $\begin{gathered} \mathrm{V}_{\mathrm{IH}}=7.5 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V} \\ \mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}} \leq 10 \mathrm{~ns} \\ \mathrm{t}_{\mathrm{w}}=1 \mu \mathrm{~s} \\ \mathrm{PRR}=100 \mathrm{kHz} \end{gathered}$ |  | 30 |  | ns |

TYPICAL APPLICATION FOR DIGIT DRIVING OF AN LED DISPLAY


## 1/6 NE582 AS A RELAY DRIVER


$1 / 6$ NE582 AS A RELAY DRIVER

## PRELIMINARY SPECIFICATION

OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT,
$I_{R}=25 \mathrm{~mA}$
$\mathrm{V}_{\text {IN }}=6.5 \mathrm{VOLTS}$


INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE,
$I_{R}=25 \mathrm{~mA}, V_{S S}=10 \mathrm{~V}, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}$


CHIP LAYOUT


## DESCRIPTION

The NE584 is a Cathode Driver for multiplexed, 7 -segment gas discharge displays.

The display segments are driven by floating current sources maintaining uniform brightness across the display panel with a minimum of system components as shown in the Display Drivers illustration. A current feedback circuit is included to adjust the anode voltage steady under optimum load conditions. The maximum voltage ripple is typically held to less than 1 V .

FEATURES

- Capable of driving up to 9 segments
- 1 external resistor provides for current programming
- Minimum component count for system cost effectiveness
- Segment current programmability for optimum operation of all character sizes
- Internal current limiting protection
- Internal feedback network ensures optimum operating conditions
- High system reliability
- Compatible with MOS and TTL inputs

ABSOLUTE MAXIMUM RATINGS


## DISPLAY DRIVERS



## PIN CONFIGURATION



DC ELECTRICAL CHARACTERISTICS $\mathrm{V}_{\mathrm{B}-}=-100 \mathrm{~V}, \mathrm{v}_{\mathrm{CC}}=5$ to 15 V


EQUIVALENT SCHEMATIC


## DESCRIPTION

The NE585 is an Anode Driver for multiplexed, 7 -segment gas discharge displays.

The display segments are driven by floating current sources maintaining uniform brightness across the display panel with a minimum of system components as shown in the Display Drivers illustration. A current feedback circuit is included to adjust the anode voltage steady optimum load conditions. The maximum voltage ripple is typically held to less than 1 V .

## FEATURES

- Capable of driving up to 9 digits
- Minimum component count for system cost effectiveness
- Segment current programmability for optimum operation of all character sizes
- Internal current limiting protection
- Internal feedback network ensures optimum operating conditions
- High system reliability
- Compatible with MOS and TTL inputs


## ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {B }+}$ | Positive supply voltage | +110 | V |
| $V_{\text {A }}$ | Anode bus voltage ${ }^{1}$ | 90 or VB+ | V |
| $V_{\text {IN }}$ | Input voltage | +15 | V |
| TJ | Junction temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {A }}$ | Ambient operating temperature range | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| ${ }_{T}{ }_{\text {S }}$ | Storage temperature range | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {sold }}$ | Soldering temperature (10secs) | 300 | ${ }^{\circ} \mathrm{C}$ |
| $P_{\text {D }}$ | Power dissipation at $25^{\circ} \mathrm{C}$ |  | mW |
|  | Plastic DIP-16 pin | 800 |  |
|  | Plastic DIP-22 pin | 1000 |  |
|  | Cerdip-16 pin | 1000 |  |
|  | Cerdip-22 pin | 1200 |  |

NOTE
Whichever is the lesser of these values is the maximum allowable anode bus voltage

## DISPLAY DRIVERS



## PIN CONFIGURATION




DC ELECTRICAL CHARACTERISTICS $\mathrm{V}_{\mathrm{B}^{+}}=100 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=60 \mathrm{~V}$ unless otherwise specified

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\mathrm{V}_{\text {B+ }}$ | Positive supply voltage |  | Operating voltage range | 90 | 100 | 110 | V |
| $\begin{aligned} & v_{I H} \\ & v_{I L} \end{aligned}$ | Input voltage High Low | For TTL type inputs | 2.6 |  | 1.1 | V |
| $I_{1}$ | Input current | $\begin{aligned} & \mathrm{V}_{\text {IN }}=2.6 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}=6 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}=15 \mathrm{~V} \end{aligned}$ | $\begin{array}{r} 100 \\ 325 \end{array}$ | $\begin{gathered} 60 \\ 200 \\ 650 \end{gathered}$ | $\begin{gathered} 200 \\ 400 \\ 1300 \end{gathered}$ | $\mu \mathrm{A}$ |
| $\begin{aligned} & I_{\mathrm{IH}} \\ & I_{\mathrm{IL}} \end{aligned}$ | High Low | For MOS type inputs | 90 |  | 5 |  |
|  | Feedback current gain $\left(=I_{A} / I_{F}\right)$ | $\begin{gathered} I_{F} \text { pulse width }<500 \mu \mathrm{~s}, \text { Duty cycle }<20 \% \\ I_{F}=2 \mathrm{~mA} \\ I_{F}=200 \mu \mathrm{~A} \end{gathered}$ | $\begin{array}{r} 24 \\ 26 \\ \hline \end{array}$ | $\begin{aligned} & 33 \\ & 33 \end{aligned}$ | $\begin{aligned} & 40 \\ & 40 \\ & \hline \end{aligned}$ | dB |
| $V_{\text {OUT }}$ | Output voltage On Off Breakdown | $\begin{gathered} \mathrm{I}_{\mathrm{OUT}}=-10 \mathrm{~mA} \\ \mathrm{~V}_{\mathrm{B}+}=100 \mathrm{~V}, \mathrm{~V}_{\mathrm{A}}=90 \mathrm{~V}, \mathrm{I}_{\mathrm{OUT}}=-100 \mu \mathrm{~A} \end{gathered}$ | $V_{A^{-55}}$ | $\mathrm{V}_{\mathrm{A}^{-38}}$ | $\mathrm{V}_{A^{-2}}$ | V |
|  | Available output current <br> Leakage current <br> Output Input | $\begin{gathered} V_{O}=V_{A}-5 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=3.5 \mathrm{~V} \\ V_{A}-V_{\text {OUT }}=50 \mathrm{~V} \\ V_{I N}=0 \end{gathered}$ |  | 35 | $\begin{aligned} & -10 \\ & -10 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| ${ }^{1} \mathrm{~B}+$ | Propagation delay <br> Power supply current | $\mathrm{C}_{\mathrm{OUT}}=15 \mathrm{pF}$ <br> 1 input high, All others open |  | $\begin{gathered} \hline 5 \\ 1.6 \end{gathered}$ | 2.5 | $\begin{aligned} & \mu \mathrm{s} \\ & \mathrm{~mA} \end{aligned}$ |

## EQUIVALENT SCHEMATIC



## section il D/A-n/D CONVERTERS

## DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

## FEATURES

- Fast settling time-300ns (typ)
- Relative accuracy $\pm 0.19 \%$ (max error)
- Non-inverting digital inputs are TTL and CMOS compatible
- High speed multiplying rate $4.0 \mathrm{~mA} / \mu \mathrm{s}$ (input slew)
- Output voltage swing +.5 V to -5.0 V
- Standard supply voltages +5.0 V and -5.0 V to -15 V
- Military qualifications pending


## APPLICATIONS

- Tracking A-to-D converters
- 21⁄2-digit panel meters and DVM's
- Waveform synthesis
- Sample and hold
- Peak detector
- Programmable gain and attenuation
- CRT character generation
- Audio digitizing and decoding
- Programmable power supplies
- Analog-digital multiplication
- Digital-digital multiplication
- Analog-digital division
- Digital addition and subtraction
- Speech compression and expansion
- Stepping motor drive

TYPICAL PERFORMANCE CHARACTERISTICS


## CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, and R-2R ladder, and 8 high speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

ABSOLUTE MAXIMUM RATNGS
$\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise specified

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| VCC | Power supply voltage |  | V |
| VEE | Positive | +5.5 |  |
| $V_{5}-V_{12}$ | Negative | -16.5 |  |
| Vo | Digital input voltage | +5.5, 0 | V |
| 114 | Applied output voltage | +0.5, -5.2 | V |
| $\mathrm{V}_{14}, \mathrm{~V}_{15}$ | Reference current | 5.0 | mA |
|  | Reference amplifier inputs | $V_{c c}, V_{\text {ee }}$ | V |
| $P_{D}$ | Power dissipation (package limitation) <br> Ceramic package <br> Plastic package | $\begin{gathered} 1000 \\ 800 \end{gathered}$ | mW |
| $T_{\text {A }}$ | Operating temperature range |  | ${ }^{\circ} \mathrm{C}$ |
|  | MC1508 | -55 to +125 |  |
|  | MC1408 | 0 to +75 |  |
| Tstg | Storage temperature range | -65 to +70 | ${ }^{\circ} \mathrm{C}$ |

PIN CONFIGURATION


## BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS 1 V cc $=+5.0 \mathrm{Vdc}, \mathrm{V}_{\mathrm{EE}}=-15 \mathrm{Vdc}, \frac{\mathrm{V}_{\mathrm{ref}}}{\mathrm{R}_{14}}=2.0 \mathrm{~mA}$ unless otherwise specified.
MC1508: $T_{A}=-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$. MC1408: $T_{A}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$

| PARAMETER |  | TEST CONDITIONS | MC1508-8 |  |  | MC1408-8 |  |  | MC1408-7 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| $\mathrm{Er}_{\text {r }}$ | Relative accuracy |  | Error relative to full scale lo, Figure 3 |  |  | $\pm 0.19$ | 。 |  | $\pm 0.19$ |  |  | $\pm 0.39$ | \% |
| $\mathrm{t}_{\mathrm{s}}$ | Setting time ${ }^{1}$ | To within $1 / 2$ LSB, includes t'PLH, $\mathrm{T}^{\prime} \mathrm{A}=+25^{\circ} \mathrm{C}$, Figure 4 |  | 300 |  |  | 300 |  |  | 300 |  | ns |
| tpLH <br> tphL | Propagation delay time Low-to-high High-to-low | $T_{A}=+25^{\circ} \mathrm{C},$ <br> Figure 4 |  | 30 | 100 |  | 30 | 100 |  | 30 | 100 | ns |
| TClo | Output full scale current drift |  |  | -20 |  |  | -20 |  |  | -20 | . | PPM $/{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & V_{\text {IH }} \\ & V_{\text {IL }} \\ & \hline \end{aligned}$ | Digital input logic level (MSB) High Low | Figure 5 | 2.0 |  | 0.8 | 2.0 |  | 0.8 | 2.0 |  | 0.8 | Vdc |
| $\begin{aligned} & \mathrm{I}_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{LL}} \end{aligned}$ | Digital input current (MSB) High Low | Figure 5 $\begin{aligned} & V_{I H}=5.0 \mathrm{~V} \\ & V_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \hline \end{aligned}$ |  | $\begin{gathered} 0 \\ -0.4 \\ \hline \end{gathered}$ | $\begin{aligned} & 0.04 \\ & -0.8 \end{aligned}$ |  | $\begin{gathered} 0 \\ -0.4 \end{gathered}$ | $\begin{array}{r} 0.04 \\ -0.8 \\ \hline \end{array}$ |  | $\begin{gathered} 0 \\ -0.4 \end{gathered}$ | $\begin{array}{r} 0.04 \\ -0.8 \\ \hline \end{array}$ | mA |
| $\mathrm{I}_{15}$ | Reference input bias current | Pin 15, Figure 5 |  | -1.0 | -3.0 |  | -1.0 | -3.0 |  | -1.0 | -3.0 | $\mu \mathrm{A}$ |
| IoR | Output current range | Figure 5 $\begin{aligned} & \mathrm{V}_{\mathrm{EE}}=-5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{EE}}=-6.0 \mathrm{~V} \text { to } \\ & -15 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 4.2 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 4.2 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 4.2 \end{aligned}$ | mA |
| 10 Io(min) | Output current <br> Off-state | Figure 5 <br> $V_{\text {ref }}=2.000 \mathrm{~V}$, <br> $R 14=1000 \Omega$ <br> All bits low | 1.9 | $\begin{gathered} 1.99 \\ 0 \\ \hline \end{gathered}$ | $\begin{aligned} & 2.1 \\ & 4.0 \end{aligned}$ | 1.9 | $\begin{gathered} 1.99 \\ 0 \\ \hline \end{gathered}$ | $\begin{array}{r} 2.1 \\ 4.0 \\ \hline \end{array}$ | 1.9 | $\begin{aligned} & 1.99 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{array}{r} 2.1 \\ 4.0 \\ \hline \end{array}$ | mA <br> $\mu \mathrm{A}$ |
| Vo | Output voltage compliance | $\mathrm{E}_{\mathrm{r}} \leq 0.19 \%$ at $T_{A}=+25^{\circ} \mathrm{C}$ <br> Figure 5 <br> $V_{E E}=-5 V$ <br> $V_{E E}$ below -10 V |  |  | $\left\|\begin{array}{l} -0.6,+0.5 \\ -5.0,+0.5 \end{array}\right\|$ |  |  | $\left\|\begin{array}{l} -0.6,+0.5 \\ -5.0,+0.5 \end{array}\right\|$ |  |  | $\left\|\begin{array}{l} -0.6,+0.5 \\ -5.0,+0.5 \end{array}\right\|$ | Vdc |
| SRI ${ }_{\text {ref }}$ | Reference current slew rate | Figure 6 |  | 4.0 |  |  | 4.0 |  |  | 4.0 |  | $\mathrm{mA} / \mu \mathrm{s}$ |
| $\operatorname{PSRR}_{(-)}$ | Output current power supply sensitivity | $I_{\text {ref }}=1 \mathrm{~mA}$ |  | 0.5 | 2.7 |  | 0.5 | 2.7 |  | 0.5 | 2.7 | $\mu \mathrm{A} / \mathrm{V}$ |
| ICC <br> IEE | Power supply current Positive Negative | All bits low, Figure 5 |  | $\begin{gathered} +13.5 \\ -7.5 \end{gathered}$ | $\begin{aligned} & +22 \\ & -13 \\ & \hline \end{aligned}$ |  | $\begin{gathered} +13.5 \\ -7.5 \\ \hline \end{gathered}$ | $\begin{aligned} & +22 \\ & -13 \end{aligned}$ |  | $\begin{gathered} +13.5 \\ -7.5 \\ \hline \end{gathered}$ | $\begin{aligned} & +22 \\ & -13 \\ & \hline \end{aligned}$ | mA |
| VCCR <br> Veer | Power supply voltage range Positive Negative | $T_{A}=+25^{\circ} \mathrm{C}$ <br> Figure 5 | $\begin{aligned} & +4.5 \\ & -4.5 \end{aligned}$ | $\begin{aligned} & +5.0 \\ & -15 \end{aligned}$ | $\begin{array}{r} +5.5 \\ -16.5 \end{array}$ | $\begin{aligned} & +4.5 \\ & -4.5 \end{aligned}$ | $\begin{aligned} & +5.0 \\ & -15 \end{aligned}$ | $\begin{array}{r} +5.5 \\ -16.5 \end{array}$ | $\begin{aligned} & +4.5 \\ & -4.5 \end{aligned}$ | $\begin{gathered} +5.0 \\ -15 \end{gathered}$ | $\begin{array}{r} +5.5 \\ -16.5 \end{array}$ | Vdc |
| PD | Power dissipation | All bits low, Figure 5 $\begin{aligned} & \mathrm{V}_{\mathrm{EE}}=-5.0 \mathrm{Vdc} \\ & \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{Vdc} \end{aligned}$ | $\square$ | $\begin{aligned} & 105 \\ & 190 \end{aligned}$ | $\begin{array}{r} 170 \\ 305 \\ \hline \end{array}$ |  | $\begin{aligned} & 105 \\ & 190 \end{aligned}$ | $\begin{aligned} & 170 \\ & 305 \\ & \hline \end{aligned}$ | . | $\begin{aligned} & 105 \\ & 190 \end{aligned}$ | $\begin{aligned} & 170 \\ & 305 \end{aligned}$ | mW |
|  |  | All bits high, Figure 5 $\begin{aligned} & \mathrm{V}_{\mathrm{EE}}=-5.0 \mathrm{Vdc} \\ & \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{Vdc} \end{aligned}$ |  | $\begin{gathered} 90 \\ 160 \end{gathered}$ |  |  | $\begin{gathered} 90 \\ 160 \end{gathered}$ |  |  | $\begin{gathered} 90 \\ 160 \end{gathered}$ |  |  |

## NOTES

1. All bits switched

## EQUIVALENT CIRCUIT SCHEMATIC



## FUNCTIONAL DESCRIPTION

## Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current ( $\mathrm{I}_{14}$ ) must always flow into pin 14 regardless of the setup method or reference voltage polarity.
Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full current $\left.\right|_{14}$. For bipolar reference signals, as in the multiplying mode, $\mathrm{R}_{15}$ can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate $\mathrm{R}_{15}$ with
only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in $\mathrm{R}_{14}$ to maintain proper phase margin; for R $\mathrm{R}_{14}$ values of 1.0 , 2.5 and $5.0 \mathrm{k} \Omega$, minimum capacitor values are 15,37 , and 75 pF . The capacitor may be tied to either $V_{E E}$ or ground, but using $V_{E E}$ increases negative supply rejection.
A negative reference voltage may be used if $\mathrm{R}_{14}$ is grounded and the reference voltage is applied to $\mathrm{R}_{15}$ as shown in Figure 2. A high input impedance is the main advantage of this method. Compensation involves a capacitor to $\mathrm{V}_{\mathrm{EE}}$ on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 V above the $V_{E E}$ supply. Bipolar input signals may be
handled by connecting $\mathrm{R}_{14}$ to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, $\mathrm{R}_{14}$ should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the 2 resistors with $0.1 \mu \mathrm{~F}$ to ground. For reference voltages greater than 5.0 V , a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high inpedance such as a transistor current source, none of the above compensation methods apply and
the amplifier must be heavily compensated, decreasing the overall bandwidth.

## Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.6 to +0.5 V at $-24^{\circ} \mathrm{C}$, due to the current switching methods employed in the MC1508/MC1408. When a current switch is turned off, the positive voltage on the output terminal can turn on the output diode and increase the output current level. When a current switch is turned on, the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is 1 diode voltage below ground when pin 1 is grounded, so a negative voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508/MC1408 may be extended to -5.0 V by opening the circuit at pin 1 . The negative supply voltage must be more negative than -10 V . Using a full scale current of 1.992 mA and load resistor of $2.5 \mathrm{k} \Omega$ between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 V . Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of $R_{L}$ up to $500 \Omega$ do not significantly affect performance, but $2.5 \mathrm{k} \Omega$ load increases worst case settling time to $1.2 \mu \mathrm{~s}$ (when all bits are switched on). Refer to the subsequent text section on settling time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1 . The value of this voltage will be the maximum allowable negative output swing.

## Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than -7.0 V , due to the increased voltage drop across the $350 \Omega$ resistors in the reference current amplifier.

## Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508/MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in
the absolute accuracy of output current. However, the MC1508/MC1408 has a very low full scale current drift with temperature.

The MC1508/ $\pm$ MC1408 series is guaranteed accurate to within $\pm 1 / 2 \mathrm{LSB}$ at $+25^{\circ} \mathrm{C}$ at a full scale output current of 1.992 mA . This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA , with the loss of $1 \mathrm{LSB}=8.0 \mu \mathrm{~A}$ which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA , allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 3. The 12 -bit converter is calibrated for a full scale output current of 1.992 mA . This is an optional step since the MC1508/MC1408 accuracy is essentially the same between 1.5 and 2.5 mA . Then the MC1508/MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total error $\pm 1 / 2$ of 1 part in 65,536 , or $\pm 0.00076 \%$, which is much more accurate than the $\pm 0.19 \%$ specification provided by the MC1508/MC1408.

## Multiplying Accuracy

The MC1508/MC1408 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of $256: 1$. The major source of error is the bias current of the termination amplifier. Under worst case conditions, these 8 amplifiers can contribute a total of $1.6 \mu \mathrm{~A}$ extra current at the output terminal. If the reference current in the multiplying mode ranges from $16 \mu \mathrm{~A}$ to 4.0 mA , the $1.6 \mu \mathrm{~A}$ contributes an error of 0.1 LSB. This is well within 8-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508/MC1408 in monotonic for all values of reference current above 0.5 mA . The recommended range for operation with a dc reference current is 0.5 to 4.0 mA .

## Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within $\pm 1 / 2$ LSB for 8 -bit accuracy and 200 ns to $1 / 2$ LSB for 7 -bit accuracy. The turnoff is typically under 100ns. These times apply when $R_{L} \leq 500 \Omega$ and $C_{0} 25 p F$.

The slowest single switch is the least significant bit, which turns on and settles in 250ns and truns off in 80 ns . In applications where the D-to-A converter functions in a positive going ramp mode, the worst case switching condition does not occur, and a settling time of less than 300ns may be realized. Bit A7 turns on in 200 ns and off in 80 ns , while bit A6 turns on in 150 ns and off in 80 ns .

The test circuit of Figure 4 requires a smaller voltage swing for the current switches due to internal voltage clamping in MC1508/MC1408. A 1.0k $\Omega$ load resistor from pin 4 to ground gives a typical settling time of 400 ns . Thus, it is voltage swing and not the output $\mathrm{R}_{\mathrm{C}}$ time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, $100 \mu \mathrm{~F}$ supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

## TEST CIRCUITS



Figure 1


Figure 2

RELATIVE ACCURACY


Figure 3

## TRANSIENT RESPONSE AND SETTLING TIME



Figure 4


Figure 5


Figure 6

## DESCRIPTION

The $5007 / 5008$ series of 8 -bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All 5007/5008 series models guarantee full 8-bit monotonicity and linearities as tight as $0.1 \%$ over the entire operating temperature range are available. Device performance is essentially unchanged over the $\pm 4.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$ power supply range, with 33 mW power consumption attainable at $\pm 5 \mathrm{~V}$ supplies.
The compact size and low power consumption make the 5007/5008 attractive for portable and military/aerospace applications.

## FEATURES

- Fast settling output current-85ns
- Full scale current prematched to $\pm 1$ LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Relative accuracy to $0.1 \%$ maximum over temperature range
- High output compliance- -10 V to +18 V
- True and complemented outputs
- Wide range multiplying capability
- Low FS current drift- $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$
- Wide power supply range- $\pm 4.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$
- Low power consumption-33mW at $\pm 5 \mathrm{~V}$
- SE5008 military qualifications pending


## APPLICATIONS

- 8-bit, $1 \mu \mathrm{~s}$ A-to-D converters
- Servo-motor and pen drivers
- Waveform generators
- Audio encoders and attenuators
- Analog meter drivers
- Programmable power supplies
- CRT display drivers
- High speed modems
- Other applications where low cost, high speed and complete input/output versatility are required


## ORDERING INFORMATION

RELATIVE

| ACCURACY | $\mathbf{0}$ to $\mathbf{7 0}{ }^{\circ} \mathrm{C}$ | $\mathbf{- 5 5}$ to $\mathbf{1 2 5}^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: |
|  | NE5007N |  |
| $0.39 \%$ FS | NE5007F | - |
|  | NE5008N |  |
|  | SE5008F |  |
| $0.19 \%$ FS | NE5008F |  |

## DEFINITION OF TERMS

Accuracy-The maximum deviation of the Dac output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination
Differential linearity-The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero
Full scale tempco-The change in Dac full scale current with change in temperature expressed in ppm/ ${ }^{\circ} \mathrm{C}$

Monotonicity-For a 1 LSB increase of input code, the output either increases or remains the same

Output voltage compliance-The range of allowable voltage levels the output pins can assume without a major effect on circuit performance

Power supply sensitivity-The change in Dac output current with changes in power supply voltage

PIN CONFIGURATION


## CROSS REFERENCE

The 5007/5008 series are pin and functionally compatible with the monoDAC-08 series of devices.

PMI
monoDAC-08A
monoDAC-08 SE5008
monoDAC-08E NE5008
monoDAC-08C NE5007

## BLOCK DIAGRAM



## TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise noted

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| TA | Operating temperature range $\begin{aligned} & \text { SE5008 } \\ & \text { NE5007/8 } \end{aligned}$ | $\begin{gathered} -55 \text { to }+125 \\ 0 \text { to }+70 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{t}_{\text {stg }}$ | Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| PD | Power dissipation | 500 | mW |
|  | Lead soldering temperature (60sec) | 300 | ${ }^{\circ} \mathrm{C}$ |
|  | V+ to V-supply | 36 | V |
|  | Logic inputs | V- to V-plus 36 V |  |
| V LC | Logic threshold control | V - to $\mathrm{V}+$ |  |
|  | Analog current outputs | See output current or output voltage performance curve |  |
| $\mathrm{V}_{14}, \mathrm{~V}_{15}$ | Reference inputs | V - to $\mathrm{V}+$ |  |
| $V_{14}$ to $V_{15}$ | Reference input differential voltage | $\pm 18$ | v |
| $\mathrm{I}_{14}$ | Reference input current | 5.0 | mA |

AC ELECTRICAL CHARACTERISTICS $V_{S}= \pm 15 \mathrm{~V}, I_{\text {REF }}=2.0 \mathrm{~mA}$, Output characteristics refer to both IOUT and IOUT unless otherwise noted. NE5008: $T_{A}=0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$. SE5008: $T_{A}=-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$.

| PARAMETER |  | TEST CONDITIONS | NE5007 |  |  | NE5008 |  |  | SE50081 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
|  | Resolution Monotonicity |  |  | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | Bits <br> Bits |
|  | Relative accuracy | Over temperature range |  |  | $\pm 0.39$ |  |  | $\pm 0.19$ |  |  | $\pm 0.19$ | \%FS |
| $\mathrm{t}_{\mathrm{s}}$ | Settling time | To $\pm 1 / 2$ LSB, all bits switched on or off, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 100 |  |  | 100 |  |  | 100 |  | ns |
| $\begin{aligned} & { }^{\mathrm{t}} \mathrm{PLH} \\ & { }^{\mathrm{t}} \mathrm{PHL} \end{aligned}$ | Propagation delay Low-to-high High-to-low | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, each bit. All bits switched |  | 35 |  |  | 35 |  |  | 35 | 60 | ns |
| TCI ${ }_{\text {FS }}$ | Full scale tempco |  |  | $\pm 10$ |  |  | $\pm 10$ |  |  | $\pm 10$ |  | ppm $/{ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {OC }}$ | Output voltage compliance | Full scale current change $<1 / 2$ LSB | -10 |  | +18 | -10 |  | +18 | -10 |  | +18 | v |
| ${ }_{\text {I FS4 }}$ | Full scale current | $V_{\text {REF }}=10.000 \mathrm{~V}$, <br> $\mathrm{R}_{14}, \mathrm{R}_{15}=5.000 \mathrm{k} \Omega$, <br> $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 1.94 | 1.99 | 2.04 | 1.94 | 1.99 | 2.04 | 1.94 | 1.99 | 2.04 | mA |
| $I_{\text {FSS }}$ | Full scale symmetry | ${ }^{1} \mathrm{FS4}^{-1} \mathrm{FS} 2$ |  | $\pm 2.0$ | $\pm 16$ |  | $\pm 1.0$ | $\pm 8.0$ |  | $\pm 1.0$ | $\pm 8.0$ | $\mu \mathrm{A}$ |
| ${ }^{\prime} \mathrm{ZS}$ | Zero scale current |  |  | 0.2 | 4.0 |  | 0.2 | 2.0 |  | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| ${ }^{\prime}$ FSR | Output current | $\begin{array}{\|l\|} \hline V-=-5.0 \mathrm{~V} \\ \mathrm{~V}-=-7.0 \mathrm{~V} \text { to }-18 \mathrm{~V} \end{array}$ | $\begin{aligned} & \hline 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \hline 2.1 \\ & 4.2 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 4.2 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 4.2 \end{aligned}$ | mA |
| $\begin{aligned} & \mathrm{v}_{\mathrm{IL}} \\ & \mathrm{v}_{\mathrm{IH}} \\ & \hline \end{aligned}$ | Logic input levels Low High | $\mathrm{V}_{\mathrm{LC}}=0 \mathrm{~V}$ | 2.0 |  | 0.8 | 2.0 |  | 0.8 | 2.0 |  | 0.8 | V |
| $\left\lvert\, \begin{aligned} & 1_{\mathrm{IL}} \\ & 1_{\mathrm{IH}} \end{aligned}\right.$ | Logic input current Low High | $V_{\mathrm{LC}}=0 \mathrm{~V}$ <br> $\mathrm{V}_{\text {IN }}=-10 \mathrm{~V}$ to +0.8 V <br> $\mathrm{V}_{1 \mathrm{~N}}=2.0 \mathrm{~V}$ to 18 V |  | $\begin{gathered} -2.0 \\ 0.002 \end{gathered}$ | $\begin{gathered} -10 \\ 10 \end{gathered}$ |  | $\begin{gathered} -2.0 \\ 0.002 \end{gathered}$ | $\begin{gathered} -10 \\ 10 \end{gathered}$ |  | $\begin{gathered} -2.0 \\ 0.002 \end{gathered}$ | $\begin{gathered} -10 \\ 10 \end{gathered}$ | $\mu \mathrm{A}$ |
| $V_{\text {IS }}$ | Logic input swing | $\mathrm{V}-=-15 \mathrm{~V}$ | -10 |  | +18 | -10 |  | +18 | -10 |  | +18 | V |
| $\mathrm{V}_{\text {THR }}$ | Logic threshold range | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ | -10 |  | +13.5 | -10 |  | +13.5 | -10 |  | +13.5 | V |
| $\mathrm{I}_{15}$ | Reference bias current |  |  | -1.0 | -3.0 |  | -1.0 | -3.0 |  | -1.0 | -3.0 | $\mu \mathrm{A}$ |
| dl/dt | Reference input slew rate | Figures 1, 3 |  | 8.0 |  |  | 8.0 |  |  | 8.0 |  | $\mathrm{mA} / \mu \mathrm{s}$ |
| $\begin{aligned} & \mathrm{PSSI}_{\mathrm{FS}+} \\ & \mathrm{PSSI}_{\mathrm{FS}}- \end{aligned}$ | Power supply sensitivity Positive <br> Negative | $\begin{aligned} & \text { IREF }=1 \mathrm{~mA} \\ & \mathrm{~V}+=4.5 \text { to } 5.5 \mathrm{~V}, \mathrm{~V}=-15 \mathrm{~V} ; \\ & \mathrm{V}+=13.5 \text { to } 16.5 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V} \\ & \mathrm{~V}=-4.5 \text { to }-5.5 \mathrm{~V}, \mathrm{~V}+=+15 \mathrm{~V} ; \\ & \mathrm{V}=-13.5 \text { to }-16.5, \mathrm{~V}+=+15 \mathrm{~V} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 0.0003 \\ & 0.002 \end{aligned}$ | $\begin{aligned} & 0.01 \\ & 0.01 \end{aligned}$ |  | $\begin{aligned} & 0.0003 \\ & 0.002 \end{aligned}$ | $\begin{aligned} & 0.01 \\ & 0.01 \end{aligned}$ |  | $\begin{aligned} & 0.0003 \\ & 0.002 \end{aligned}$ | $\begin{aligned} & 0.01 \\ & 0.01 \end{aligned}$ | \%FS/\%VS |
| $\begin{aligned} & 1+ \\ & 1- \end{aligned}$ | Powersupply current Positive Negative | $\mathrm{V}_{\mathrm{S}}= \pm 5 \mathrm{~V}, \mathrm{IREF}=1.0 \mathrm{~mA}$ |  | $\begin{gathered} 2.3 \\ -4.3 \end{gathered}$ | $\begin{gathered} 3.8 \\ -5.8 \end{gathered}$ |  | $\begin{array}{r} 2.3 \\ -4.3 \end{array}$ | $\begin{gathered} 3.8 \\ -5.8 \end{gathered}$ |  | $\begin{gathered} 2.3 \\ -4.3 \end{gathered}$ | $\begin{gathered} 3.8 \\ -5.8 \end{gathered}$ | mA |
| $\begin{aligned} & 1+ \\ & 1- \end{aligned}$ | Positive Negative | $\mathrm{V}_{\mathrm{S}}=+5 \mathrm{~V},-15 \mathrm{~V}, \mathrm{I}_{\text {REF }}=2.0 \mathrm{~mA}$ |  | $\begin{gathered} \hline 2.4 \\ -6.4 \\ \hline \end{gathered}$ | $\begin{array}{\|c\|} \hline 3.8 \\ -7.8 \\ \hline \end{array}$ |  | $\begin{gathered} 2.4 \\ -6.4 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 3.8 \\ -7.8 \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline 2.4 \\ -6.4 \\ \hline \end{gathered}$ | $\begin{array}{\|c\|} \hline 3.8 \\ -7.8 \\ \hline \end{array}$ |  |
| $\begin{aligned} & 1+ \\ & 1- \end{aligned}$ | Positive Negative | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{I}_{\text {REF }}=2.0 \mathrm{~mA}$ |  | $\begin{gathered} \hline 2.5 \\ -6.5 \end{gathered}$ | $\begin{gathered} \hline 3.8 \\ -7.8 \end{gathered}$ |  | $\begin{gathered} \hline 2.5 \\ -6.5 \end{gathered}$ | $\begin{gathered} \hline 3.8 \\ -7.8 \end{gathered}$ |  | $\begin{gathered} \hline 2.5 \\ -6.5 \end{gathered}$ | $\begin{gathered} \hline 3.8 \\ -7.8 \end{gathered}$ |  |
| $P_{D}$ | Power dissipation | $\begin{aligned} & \pm 5 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=1.0 \mathrm{~mA} \\ & +5 \mathrm{~V},-15 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA} \\ & \pm 15 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA} \end{aligned}$ |  | $\begin{gathered} \hline 33 \\ 108 \\ 135 \end{gathered}$ | $\begin{gathered} 48 \\ 136 \\ 174 \end{gathered}$ |  | $\begin{gathered} 33 \\ 108 \\ 135 \end{gathered}$ | $\begin{gathered} 48 \\ 136 \\ 174 \end{gathered}$ |  | $\begin{gathered} \hline 33 \\ 108 \\ 135 \end{gathered}$ | $\begin{gathered} 48 \\ 136 \\ 174 \end{gathered}$ | mW |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


POWER SUPPLY CURRENT vs V-


## TYPICAL APPLICATION

PULSED REFERENCE OPERATION


TYPICAL VALUES
$R_{I N}=5 K$
$+\mathrm{V}_{\text {IN }}=10 \mathrm{~V}$

## DESCRIPTION

The 5009 monolithic 8-bit digital-to-analog converter is an electrical selection of the $5007 / 8$ series of 8 -bit D/A converters. Relative accuracy is specified to $\pm 1 / 4$ LSB maximum over the operating temperature range. Differential nonlinearity and settling times are also specified to maximum limits.
The device is specifically designed for precision applications in process control and military systems. The SE5009 is specified as equal or superior to the PMI DAC-08A in all respects. Additional relevant testing and application material is shown in the data sheet and application notes for the NE5007/8.

## FEATURES

- Fast settling output current-60ns typical, 135ns maximum
- Relative accuracy- $\pm 0.1 \%$ maximum
- Differential nonlinearity $- \pm 0.19 \%$ maximum
- Low full-scale current drift, $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ typical
- SE5009 military qualifications pending


## APPLICATIONS

- Fast 8-bit A/D converter
- Variable gain amplifiers
- Waveform generators
- 3 digit BCD D/A converter (0.1\%)
- Programmable power supplies


## DEFINITION OF TERMS

Relative Accuracy-The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination.
Differential Nonlinearity-The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero.
Full Scale Tempco-The change in DAC full scale current with change in temperature expressed in ppm $/{ }^{\circ} \mathrm{C}$.
Monotonicity—For a 1 LSB increase of input code, the output either increases or remains the same.

Output Voltage Compliance-The range of allowable voltage levels the output pins can assume without a major effect on circuit performance.

Power Supply Sensitivity-The change in DAC output current with changes in power supply voltage.

PIN CONFIGURATION


NOTE
*SE5009 is in F package only

## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Total supply voltage (V+- V-) | 36 | V |
| Logic input voltage | $\mathrm{V}-+36$ | V |
| VLC Voltage at pin 1 | $\mathrm{V}-$ to $\mathrm{V}+$ | V |
| Reference input voltage | $\mathrm{V}-$ to $\mathrm{V}+$ | V |
| Reference input differential voltage | $\pm 18$ | V |
| Reference input current | 5.0 | mA |
| Operating temperature range |  | ${ }^{\circ} \mathrm{C}$ |
| SE5009 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| NE5009 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead soldering temperature (10sec) | 300 | mW |
| Power dissipation* | 500 |  |

NOTE
*Derate F package at $10 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $100^{\circ} \mathrm{C}$.

DC ELECTRICAL CHARACTERISTICS
These specs apply for $V_{S}= \pm 15 \mathrm{~V}$, $I_{\text {REF }}=2 \mathrm{~mA}$, $T_{A}$ for NE5009 $0^{\circ}$ to $70^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{A}}$ for SE5009 $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$. Output char. for both lout and lout.

| PARAMETER |  | TEST CONDITIONS | NE5009 |  |  | SE5009 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
|  | Resolution Monotonicity |  |  | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | $\begin{aligned} & 8 \\ & 8 \end{aligned}$ | bits bits |
|  | Relative accuracy Differential nonlinearity | Over temperature range |  | $\pm 0.1$ | $\begin{array}{\|c\|} \hline \pm 0.1 \\ \pm 0.19 \end{array}$ |  | $\pm 0.1$ | $\begin{gathered} \pm 0.1 \\ \pm 0.19 \end{gathered}$ | $\begin{aligned} & \hline \% \text { FS } \\ & \% \mathrm{FS} \end{aligned}$ |
| TClfs Voc | Full scale tempco Output voltage compliance | Full scale current change $<1 / 2 \mathrm{LSB}$ | -10 | $\pm 10$ | $\begin{array}{r}  \pm 50 \\ +18 \\ \hline \end{array}$ | -10 | $\pm 10$ | $\begin{array}{r}  \pm 50 \\ +18 \end{array}$ | $\underset{\mathrm{V}}{\mathrm{ppm} /{ }^{\circ} \mathrm{C}}$ |
| IfS4 <br> Ifss <br> Izs | Full scale current <br> Full scale symmetry <br> Zero scale current | $\begin{gathered} \mathrm{V}_{\text {REF }}=10.000 \mathrm{~V}, \mathrm{R}_{14} \cdot \mathrm{R}_{15}=5.000 \mathrm{k} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{IFS}_{\mathrm{FS}}-\mathrm{I}_{\mathrm{FS} 2} \end{gathered}$ | 1.984 | $\begin{array}{\|c\|} \hline 1.992 \\ \\ \pm 0.5 \\ 0.1 \\ \hline \end{array}$ | $\begin{array}{c\|} \hline 2.000 \\ \\ \pm 4.0 \\ 1.0 \end{array}$ | 1.984 | $\begin{gathered} 1.992 \\ \\ \pm 0.5 \\ 0.1 \end{gathered}$ | $\begin{gathered} 2.000 \\ \\ \pm 4.0 \\ 1.0 \\ \hline \end{gathered}$ | mA <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| IfSR | Output current range | $\begin{gathered} \mathrm{V}-=-5.0 \mathrm{~V} \\ \mathrm{~V}-=-7.0 \mathrm{~V} \text { to }-18 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 4.2 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 4.2 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{array}{\|l\|l} \mathrm{v}_{\mathrm{IL}} \\ \mathrm{v}_{\mathrm{H}} \end{array}$ | Logic input levels Logic "0" Logic " 1 " | $\begin{aligned} & \mathrm{V}_{\mathrm{LC}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{LC}}=0 \mathrm{~V} \\ & \hline \end{aligned}$ | 2.0 |  | 0.8 | 2.0 |  | 0.8 | $\begin{aligned} & v \\ & v \end{aligned}$ |
| $\begin{aligned} & \mathrm{ILL}_{2} \\ & \mathrm{IH}_{2} \end{aligned}$ | Logic input current Logic "0" Logic "1" | $\begin{gathered} \mathrm{V}_{\mathrm{LC}}=0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=-10 \mathrm{~V} \text { to }+0.8 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=2.0 \mathrm{~V} \text { to } 18 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & -2.0 \\ & 0.002 \end{aligned}$ | $\begin{gathered} -10 \\ 10 \end{gathered}$ |  | $\begin{aligned} & -2.0 \\ & 0.002 \end{aligned}$ | $\begin{gathered} -10 \\ 10 \end{gathered}$ | ${ }_{\mu \mathrm{A}}^{\mu \mathrm{A}}$ |
| $\begin{array}{\|l} V_{\text {IS }} \\ V_{\text {THR }} \\ \hline \end{array}$ | Logic input swing Logic threshold range | $\begin{aligned} & \mathrm{V}-=-15 \mathrm{~V} \\ & \mathrm{~V}= \pm 15 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & -10 \\ & -10 \\ & \hline \end{aligned}$ |  | $\begin{array}{\|c\|} \hline+18 \\ +13.5 \\ \hline \end{array}$ | $\begin{aligned} & -10 \\ & -10 \\ & \hline \end{aligned}$ |  | $\begin{array}{\|c\|} \hline+18 \\ +13.5 \\ \hline \end{array}$ | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| $l_{15}$ di/dt | Reference bias current Reference input slew rate |  | 4.0 | $\begin{gathered} \hline-1.0 \\ 8.0 \\ \hline \end{gathered}$ | -3.0 | 4.0 | $\begin{gathered} \hline-1.0 \\ 8.0 \\ \hline \end{gathered}$ | -3.0 | $\begin{gathered} \mu \mathrm{A} \\ \mathrm{~mA} / \mu \mathrm{s} \\ \hline \end{gathered}$ |
| PSSIFS+ <br> PSSIFS- | Power supply sensitivity | $\begin{gathered} \text { IREF }=1 \mathrm{~mA}, V-=-15 \mathrm{~V}: \\ \mathrm{V}+=4.5 \text { to } 5.5 \mathrm{~V} \\ \mathrm{~V}+=13.5 \text { to } 16.5 \mathrm{~V} \\ \text { IREF }=1 \mathrm{~mA}, \mathrm{~V}+=+15 \mathrm{~V}: \\ \mathrm{V}-=-4.5 \text { to }-5.5 \mathrm{~V} \\ \mathrm{~V}-=-13.5 \text { to }-16.5 \mathrm{~V} \end{gathered}$ |  | $\begin{aligned} & 0.0003 \\ & 0.0003 \\ & 0.0003 \\ & 0.0003 \end{aligned}$ | $\begin{aligned} & 0.01 \\ & 0.01 \\ & 0.01 \\ & 0.01 \end{aligned}$ |  | 0.0003 0.0003 0.0003 0.0003 | $\begin{aligned} & 0.01 \\ & 0.01 \\ & 0.01 \\ & 0.01 \end{aligned}$ | \%FS/\%VS <br> \%FS/\%VS <br> \%FS/\%VS <br> \%FS/\%VS |
| $\begin{aligned} & 1+ \\ & 1- \end{aligned}$ | Power supply current | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{I}_{\text {ReF }}=1.0 \mathrm{~mA}$ |  | $\begin{gathered} 2.3 \\ -4.3 \end{gathered}$ | $\begin{gathered} 3.8 \\ -5.8 \end{gathered}$ |  | $\begin{gathered} 2.3 \\ -4.3 \end{gathered}$ | $\begin{gathered} 3.8 \\ -5.8 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & 1+ \\ & 1- \end{aligned}$ | Power supply current | $\mathrm{V}_{\mathrm{S}}=+5 \mathrm{~V},-15 \mathrm{~V} ; \mathrm{IREF}=2.0 \mathrm{~mA}$ |  | $\begin{gathered} 2.4 \\ -6.4 \end{gathered}$ | $\begin{array}{r} 3.8 \\ -7.8 \\ \hline \end{array}$ |  | $\begin{array}{r} 2.4 \\ -6.4 \\ \hline \end{array}$ | $\begin{gathered} 3.8 \\ -7.8 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & 1+ \\ & 1- \end{aligned}$ | Power supply current | $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{l}$ REF $=2.0 \mathrm{~mA}$ |  | $\begin{gathered} 2.5 \\ -6.5 \end{gathered}$ | $\begin{gathered} 3.8 \\ -7.8 \end{gathered}$ |  | $\begin{array}{r} 2.5 \\ -6.5 \end{array}$ | $\begin{gathered} 3.8 \\ -7.8 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| PD Pow | Power dissipation | $\begin{gathered} \pm 5 \mathrm{~V}, I_{\mathrm{REF}}=1.0 \mathrm{~mA} \\ +5 \mathrm{~V},-15 \mathrm{~V}, I_{\mathrm{REE}}=2.0 \mathrm{~mA} \\ \pm 15 \mathrm{~V}, I_{\mathrm{REF}}=2.0 \mathrm{~mA} \end{gathered}$ |  | $\begin{gathered} \hline 33 \\ 108 \\ 135 \end{gathered}$ | $\begin{gathered} 48 \\ 136 \\ 174 \end{gathered}$ |  | $\begin{gathered} \hline 33 \\ 108 \\ 135 \end{gathered}$ | $\begin{aligned} & 48 \\ & 136 \\ & 174 \end{aligned}$ | $\begin{aligned} & \mathrm{mW} \\ & \mathrm{~mW} \\ & \mathrm{~mW} \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS These specs apply for $V_{S}= \pm 15 \mathrm{~V}, I_{R E F}=2 \mathrm{~mA}$, Output char. for both lout and lout.

| PARAMETER |  | TEST CONDITIONS | SE/NE5009 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\mathrm{t}_{\text {s }}$ | Settling time <br> Major carry transition |  | To $\pm 1 / 2$ LSB all bits switched ON or $\mathrm{OFF}, \mathrm{T}_{A}=25^{\circ} \mathrm{C}$ <br> To $90 \%$ complete, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{aligned} & 60 \\ & 20 \end{aligned}$ | 135 | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |
| tPLH, ${ }^{\text {, PHL }}$ | Propagation delay Each bit All bits switched | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\begin{aligned} & 35 \\ & 35 \end{aligned}$ | $\begin{aligned} & 60 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |

## TEST CIRCUIT



## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


LOGIC INPUT CURRENT vs INPUT VOLTAGE

$\mathbf{V}_{\text {TH }}-V_{\text {LC }}$ vs TEMPERATURE



BASIC 5008/5009 CONFIGURATION

$I_{F S} \approx \frac{+V_{\text {Ref }}}{R_{\text {Ref }}} \times \frac{255}{256} ; I_{0}+T_{0}=I_{\text {FS }}$ for all logic states

RECOMMENDED FULL SCALE AND ZERO SCALE ADJ.


UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT


UNIPOLAR VOLT OUTPUT FOR HIGH IMPEDANCE OUTPUT


BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)


CODE CHART

|  | $\begin{array}{llllllllll}B_{1} & B_{2} & B_{3} & B_{4} & B_{5} & B_{6} & B_{7} & B_{8}\end{array}$ |  |  |  |  |  |  |  | V OUT | $\overline{V_{\text {OUT }}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| POS full scale | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -9.920V | +10.000 |
| POS f.s. - 1LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -9.840V | +9.920 |
| + Zero scàle + 1LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -0.080V | +0.160 |
| Zero scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | +0.080 |
| Zero scale - 1LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.080 | 0.000 |
| Neg full scale - 1LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +9.920 | -9.840 |
| Neg full scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +10.000 | -9.920 |

## SYMMETRICAL OFFSET BINARY (BIPOLAR)


$V_{\text {OUT }}=0$ to $\pm \mathrm{V}^{*}$
$\pm \mathrm{V}$ *Range:
$\pm 5 \mathrm{~V}$ for $\mathrm{R}_{1}=\mathrm{R}_{2}=2.5 \mathrm{k}$
$\pm 10 \mathrm{~V}$ for $\mathrm{R}_{1}=\mathrm{R}_{2}=5.0 \mathrm{k}$

## 3 DIGIT BCD CONVERTER

A 3 digit BCD converter, using inexpensive 8 -bit binary DACs, can achieve $\pm 0.1 \%$ accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9 . The feedback resistor $\left(R_{7}\right)$ sets the full scale at 9.99 V .

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are $8,4,2$ and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.
In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.


## DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{\mathrm{LE}}$ input is in the low state. When $\overline{\mathrm{LE}}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{\mathrm{LE}}$ again goes low. This feature allows easy compatibility with most microprocessors.
The chip also comprises a stable voltage reference ( 5 V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.
The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

## FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm 1 / 2$ LSB
- Monotonic to 8 bits
- Amplifier and reference both shortcircuit protected
- Compatible with 2650, 8080 and many other $\mu$ P's.


## APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

PIN CONFIGURATION


SE5018 available in F package only.

## ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}+$ | Positive supply voltage | 18 | V |
| $V_{\text {cc }}{ }^{-}$ | Negative supply voltage | -18 | V |
| VIN | Logic input voltage | 0 to 18 | V |
| $V_{\text {REF }}$ IN | Voltage at $\mathrm{V}_{\text {ref }}$ input | 12 | V |
| VREFADJ | Voltage at Vref adjust | 0 to VREF | V |
| VSUM | Voltage at sum node | 12 | V |
| Irefsc | Short-circuit current to ground at $\mathrm{V}_{\text {REF }}$ OUT | Continuous |  |
| IOUTSC | Short-circuit current to ground or either supply at Vout | Continuous |  |
| IREF Pd | Reference input current | 5 | mA |
| PD | -N package | 800 | mW |
|  | -F package | 1000 | mW |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range SE5018 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
|  | NE5018 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Tstg | Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| TSOLD | Lead soldering temperature (10 seconds) | 300 | ${ }^{\circ} \mathrm{C}$ |

*NOTE
For N package, derate at $120^{\circ} \mathrm{C} / \mathrm{W}$ above $35^{\circ} \mathrm{C}$
For F package, derate at $75^{\circ} \mathrm{C} / \mathrm{W}$ above $75^{\circ} \mathrm{C}$

DC ELECTRICAL CHARACTERISTICS $V_{C C}+=15 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}-=-15 \mathrm{~V}$, SE5018. $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$,
NE5018. $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | SE5018 |  |  | NE5018 |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| VCC+ | Positive supply voltage |  | ```To }\pm1/2LSB,10V ste VCC+ +12 to +18V VCC- -12 to -18V VCc+ = 15V``` | 2.0 | $\begin{gathered} 15 \\ -15 \\ 8 \end{gathered}$ | $\pm 0.19$ |  | 15 | $\pm 0.19$ | V <br> V <br> bits <br> $\%$ |
| Vcc- | Negative supply voltage |  |  |  |  |  | -15 |  |  |
|  | Resolution |  |  |  |  |  | 8 |  |  |
|  | Relative accuracy |  |  |  |  |  |  |  |  |
| Ts | Settling time | $\begin{gathered} 2 \\ \pm 1 \end{gathered}$ |  |  |  |  | $\begin{gathered} 2 \\ \pm 1 \end{gathered}$ | $\mu \mathrm{S}$ |  |  |
| PSRR | Power supply |  |  |  |  |  |  |  | $\mathrm{mV} / \mathrm{V}$ |  |
|  | Rejection ratio |  |  |  |  |  |  |  |  |  |
| Icc+ | Positive supply current | 8 |  |  |  |  | 8 |  | mA |  |
| Icc- | Negative supply current | $\mathrm{V}_{\text {CC }}-=-15 \mathrm{~V}$ | -10 |  |  |  | -10 |  | mA |  |
| lin 0 ) | Logic " 0 " input current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ | 5 |  |  |  | 5 |  | $\mu \mathrm{A}$ |  |
| $\mathrm{V}_{1 \times}(0)$ | Logic "0" input voltage |  |  |  | 0.8 |  |  | 0.8 | v |  |
| $\mathrm{V}_{1 \times}(1)$ | Logic "1" input voltage |  |  |  |  | 2.0 |  |  | V |  |
| TpwLe | Latch enable pulse width |  | 400 |  |  |  | 400 |  | ns |  |

## BLOCK DIAGRAM



EQUIVALENT SCHEMATIC


## sECTION 12 AUDIO CIRCUITS

## DESCRIPTION

The LM381/LM381A is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (112dB), large output voltage swing (VCC -2V p-p), and wide power bandwidth ( $75 \mathrm{kHz}, 20 \mathrm{~V}$ p-p.). The LM381/LM381A operates from a single supply across the wide range of 9 to 40 V .
Either differential input or single ended input configurations may be selected. The amplifier is internally compensated with the provision for additional external compensation for narrow band applications.

## TYPICAL APPLICATIONS



TYPICAL MAGNETIC PHONO
PREAMP


NOTE
All resistors standard and are measured in ohms.

## FEATURES

- Low noise-. $5_{\mu} \mathrm{V}$ total input noise
- High gain-112dB open loop
- Single supply operation
- Wide supply range 9-40V
- Power supply rejection 120 dB
- Large output voltage swing(VCC $-2 V p-p)$
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 75kHz, 20V p-p
- Internally compensated
- Short circuit protected

PIN CONFIGURATION


EQUIVALENT CIRCUIT


## TYPICAL APPLICATIONS




NOTE
All resistors standard and are measured in ohms.

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | +40 | V |
| Power dissipation | 600 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering, 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LM381/381A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Voltage gain | Open loop (differential input) Open loop (single ended) |  | $\begin{aligned} & 160,000 \\ & 320,000 \end{aligned}$ |  | $\begin{aligned} & V / V \\ & V / V \end{aligned}$ |
| Supply current | VCC 9 to 40V, RL $=\infty$ |  | 10 |  | mA |
| Input resistance | Positive input Negative input |  | $\begin{aligned} & 100 \\ & 200 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| Input current Output resistance | Negative input Open loop |  | $\begin{aligned} & \hline 0.5 \\ & 150 \\ & \hline \end{aligned}$ | . | $\begin{gathered} \mu \mathrm{A} \\ \Omega \end{gathered}$ |
| Output current | Source Sink |  | 8 2 |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Output voltage swing | Peak-to-peak |  | Vcc-2 |  | V |

AC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LM381/381A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Small signal bandwidth Power bandwidth Maximum input voltage | 20 V p-p $(\mathrm{V} \mathrm{Cc}=24 \mathrm{~V})$ <br> Linear operation |  | $\begin{aligned} & 15 \\ & 75 \end{aligned}$ | 300 | $\begin{gathered} \mathrm{MHz} \\ \mathrm{kHz} \\ \mathrm{mVrms} \end{gathered}$ |
| Supply rejection ratio Channel separation | $\begin{aligned} & f=1 \mathrm{kHz} \\ & f=1 \mathrm{kHz} \end{aligned}$ |  | $\begin{gathered} 120 \\ 60 \end{gathered}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Total harmonic distortion <br> Total equivalent input noise <br> LM381A <br> LM381 | $\begin{gathered} 75 \mathrm{~dB} \text { gain, } \mathrm{f}=1 \mathrm{kHz} \\ \mathrm{RS}=600 \Omega, 100-10,000 \mathrm{~Hz} \\ \text { (single ended input) } \end{gathered}$ |  | $\begin{aligned} & 0.1 \\ & \\ & 0.5 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 0.7 \\ & 1.0 \end{aligned}$ | \% <br> $\mu$ Vrms <br> $\mu$ Vrms |
| Noise figure | $\left.\begin{array}{c}50 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz} \\ 10 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz} \\ 5 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz}\end{array}\right\}$Single <br> Ended <br> Input |  | $\begin{aligned} & 1.0 \\ & 1.3 \\ & 1.6 \end{aligned}$ |  | dB <br> dB <br> dB |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


PSRR vs FREQUENCY


NOISE VOLTAGE vs FREQUENCY

${ }^{\mathrm{t}}\left(\mathrm{H}_{\mathrm{z}}\right)$
\% DISTORTION


GAIN AND PHASE RESPONSE


NOISE CURRENT vs FREQUENCY

$\mathrm{f}_{\mathrm{t}}^{\mathrm{Hz})}$

CHANNEL SEPARATION


VOLTAGE GAIN vs SUPPLY VOLTAGE


PULSE RESPONSE


## DESCRIPTION

The LM382 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (100dB), large output voltage swing ( $V C C-2 V$ ) $p-p$, and wide power bandwidth ( $75 \mathrm{kHz}, 20 \mathrm{~V}$ p-p). The LM382 operates from a single supply across the wide range of 9 to 40 V .
A resistor matrix is provided on the chip to allow the user to select a variety of closed loop gain options and frequency response characteristics such as flat-band, NAB or RIAA equalization. The circuit is supplied in the 14 lead dual-in-line package.

## TYPICAL APPLICATIONS



## FEATURES

- Low noise- $0.8 \mu \mathrm{~V}$ total equivalent input noise
- High gain-100dB open loop
- Single supply operation
- Wide supply range 9 to 40 V
- Power supply rejection-120dB
- Large output voltage swing
- Wide bandwidth -15 MHz unity gain
- Power bandwidth-75kHz, 20V p-p
- Internally compensated
- Short circuit protected

PIN CONFIGURATION


EQUIVALENT SCHEMATIC


ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | +40 | V |
| Power dissipation | 600 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature |  |  |
| (soldering, 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

## TYPICAL APPLICATIONS



DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LM382 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Voltage gain Supply current | Open loop (differential input) $\mathrm{V}_{\mathrm{CC}} 9$ to $40 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty$ |  | $\begin{gathered} 100,000 \\ 10 \end{gathered}$ | 16 | $\begin{aligned} & \mathrm{V} / \mathrm{V} \\ & \mathrm{~mA} \end{aligned}$ |
| Input resistance | Positive input Negative input |  | $\begin{aligned} & 100 \\ & 200 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| Input current Output resistance | Negative input Open loop |  | $\begin{aligned} & 0.5 \\ & 150 \end{aligned}$ |  | $\begin{gathered} \mu \mathrm{A} \\ \Omega \end{gathered}$ |
| Output current | Source Sink |  | $\begin{aligned} & 8 \\ & 2 \end{aligned}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Output voltage swing | Peak-to-peak, $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ |  | Vcc-2 |  | V |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | LM382 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Small signal bandwidth Power bandwidth Maximum input voltage | $20 \mathrm{~V}-\mathrm{p}(\mathrm{Vcc}=24 \mathrm{~V})$ Linear operation |  | $\begin{aligned} & 15 \\ & 75 \end{aligned}$ | 300 | $\begin{gathered} \mathrm{MHz} \\ \mathrm{kHz} \\ \mathrm{mVrms} \end{gathered}$ |
| Supply rejection ratio Channel separation | $\begin{aligned} & f=1 \mathrm{kHz} \\ & f=1 \mathrm{kHz} \end{aligned}$ | 40 | $\begin{aligned} & 120 \\ & 60 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Total harmonic distortion <br> Total equivalent input noise | $\begin{gathered} 60 \mathrm{~dB} \text { gain, } \mathrm{f}=1 \mathrm{kHz} \\ \text { Rs }=600 \Omega, 100-10,000 \mathrm{~Hz} \end{gathered}$ |  | $\begin{aligned} & 0.1 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & 0.3 \\ & 1.2 \end{aligned}$ | $\stackrel{\%}{\mu \mathrm{Vrms}}$ |
| Noise figure | $50 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz}$ $10 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz}$ $5 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz}$ |  | $\begin{aligned} & 1.0 \\ & 1.6 \\ & 2.6 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS


## DESCRIPTION

The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain ( 104 dB ), large output voltage swing ( $V c c-2 \vee p-p$ ), and wide power bandwidth $(75 \mathrm{kHz}, 20 \mathrm{~V}$ p-p). The LM387 operates from a single supply across the wide range of 9 to 40 V .
The amplifiers are internally compensated for all gains greater than 10. The LM387 is available in an 8 lead dual-in-line package.

## TYPICAL APPLICATIONS



FEATURES

- Low noise- $0.8 \mu \mathrm{~V}$ total input noise
- High gain-104dB open loop
- Single supply operation
- Wide supply range 9 to 40 V
- Power supply rejection-110dB
- Large output voltage swing (VCC - 2V p-p)
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 75kHz, 20V p-p
- Internally compensated
- Short circuit protected


## PIN CONFIGURATION



EQUIVALENT CIRCUIT


TYPICAL APPLICATIONS


TYPICAL TAPE PLAYBACK AMPLIFIER


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | +40 | V |
| Power dissipation | 500 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering, 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LM387 |  | UNIT |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ |  |  |
| Voltage gain | Open loop |  | 160,000 |  | $\mathrm{~V} / \mathrm{V}$ |
| Supply current | VCc 9 to 40V, RL $=\infty$ |  | 10 |  | mA |
| Input resistance | Positive input |  | 100 |  | $\mathrm{k} \Omega$ |
|  | Negative input |  | 200 |  | $\mathrm{k} \Omega$ |
| Input current | Negative input |  | 0.5 |  | $\mu \mathrm{~A}$ |
| Output resistance | Open loop |  | 150 |  | $\Omega$ |
| Output current | Source |  | 8 |  | mA |
|  | Sink |  | 2 |  | mA |
| Output voltage swing | Peak-to-peak |  | $\mathrm{V}_{\mathrm{Cc}}-2$ |  | V |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{VCC}=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LM387 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Small signal handwidth Power bandwidth Maximum input voltage | $20 \mathrm{~V}-\mathrm{p}(\mathrm{Vcc}=24 \mathrm{~V})$ <br> Linear operation |  | $\begin{aligned} & 15 \\ & 75 \end{aligned}$ | 300 | $\begin{gathered} \text { iviriz } \\ \text { kHz } \\ \mu \text { Vrms } \end{gathered}$ |
| Supply rejection ratio Channel separation | $\begin{aligned} & f=1 \mathrm{kHz} \\ & f=1 \mathrm{kHz} \end{aligned}$ |  | $\begin{gathered} 110 \\ 60 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Total harmonic distortion Total equivalent input noise | $\begin{gathered} 75 \mathrm{~dB} \text { gain, } \mathrm{f}=1 \mathrm{kHz} \\ \mathrm{R}_{\mathrm{S}}=600 \Omega, 100-10,000 \mathrm{~Hz} \end{gathered}$ |  | $\begin{aligned} & 0.1 \\ & 0.8 \\ & \hline \end{aligned}$ | 1.4 | \% $\mu$ Vrms |
| Noise figure | $\begin{gathered} 50 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz} \\ 10 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz} \\ 5 \mathrm{k} \Omega, 100-10,000 \mathrm{~Hz} \end{gathered}$ |  | $\begin{aligned} & 1.0 \\ & 1.6 \\ & 2.8 \end{aligned}$ |  | dB <br> dB <br> dB |

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


PSRR vs FREQUENCY


NOISE VOLTAGE vs FREQUENCY

\% DISTORTION


GAIN AND PHASE RESPONSE


NOISE CURRENT vs FREQUENCY

${ }^{1}(\mathrm{~Hz})$

CHANNEL SEPARATION


VOLTAGE GAIN vs SUPPLY VOLTAGE


PULSE RESPONSE


## DESCRIPTION

The NE/SE540 is a monolithic, class $A B$ power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use an audio power amplifier.

## FEATURES

- Internal current limiting
- Low standby current
- High output current capability
- Wide power bandwidth
- Low distortion


## PIN CONFIGURATION



## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Supply voltage |  |  |
| SE540 | $\pm 27$ | V |
| NE540 | $\pm 22$ | V |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE540 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE540 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | Indefinite |  |
| Output short circuit duration |  |  |
| (Not exceeding maximum dissipation.) |  |  |

DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE540 |  |  | NE540 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Operating supply voltage Quiescent current |  | $\pm 5$ | 13 | $\begin{gathered} \pm 25 \\ 20 \end{gathered}$ | $\pm 5$ | 13 | $\begin{gathered} \pm 20 \\ 20 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Input offset voltage Input offset current |  |  | $\begin{gathered} 5 \\ 0.3 \end{gathered}$ | $\begin{gathered} 7 \\ 0.7 \end{gathered}$ |  | $\begin{gathered} 7 \\ 0.5 \end{gathered}$ | $\begin{gathered} 10 \\ 1 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input bias current Input impedance |  |  | $\begin{aligned} & 1.5 \\ & 20 \end{aligned}$ | 3 |  | $\begin{gathered} 2 \\ 20 \end{gathered}$ | 5 | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{k} \Omega \end{aligned}$ |
| Current gain Gain variation over temperature range | 40dB gain | 80 | $\begin{gathered} 100 \\ \pm 0.1 \end{gathered}$ |  | 70 | $\begin{gathered} 90 \\ \pm 0.1 \end{gathered}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Power supply rejection ratio Common mode rejection ratio | 40dB gain | 80 | $\begin{gathered} 90 \\ 110 \end{gathered}$ |  | 60 | $\begin{aligned} & 80 \\ & 90 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Output drive current |  | $\pm 120$ | $\pm 150$ |  | $\pm 80$ | $\pm 100$ |  | mA |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{C C}= \pm 20 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE540 |  |  | NE540 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Frequency response Distortion | 40 dB gain $\pm 1 \mathrm{~dB}$ <br> 40dB gain, Output 3dB below maximum $\begin{aligned} R_{\mathrm{L}} & =600 \Omega \\ R_{\mathrm{L}} & =2 \mathrm{k} \Omega \end{aligned}$ |  | $\begin{aligned} & 500 \\ & 0.25 \\ & \\ & 0.06 \end{aligned}$ | 0.5 |  | $\begin{array}{r} 100 \\ 0.5 \\ \\ 0.06 \end{array}$ | 1.0 | $\begin{gathered} \mathrm{kHz} \\ \% \end{gathered}$ |
| Equivalent input noise voltage | $\begin{gathered} \mathrm{Rs}_{\mathrm{S}}=600 \Omega \\ 50 \mathrm{~Hz} \text { to } 500 \mathrm{kHz} \end{gathered}$ |  | 10 |  |  | 10 |  | $\mu \mathrm{V}$ |
| Slew rate | $\begin{aligned} & V_{\text {CC }}= \pm 20 \mathrm{~V} \\ & V_{\text {OUT }}= \pm 15 \mathrm{~V} \end{aligned}$ |  | 200 |  |  | 200 |  | $\mathrm{V} / \mu \mathrm{s}$ |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


TEST CIRCUITS
OFFSET VOLTAGE MEASUREMENT

35 WATT AMPLIFIER


## DESCRIPTION

The NE541 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use as an audio power amplifier.

FEATURES

- Internal current limiting
- Low standby current
- High output current capability
- Wide power bandwidth
- Low distortion

PIN CONFIGURATION


## PIN DESIGNATION

| PIN NO. | NAME AND FUNCTION |
| :---: | :---: |
| 1 | Output 2 (base) |
| 2 | Output 3 (collector) |
| 3 | V + |
| 4 | Power limit |
| 5 | NC |
| 6 | Non-inverting input |
| 7 | NC |
| 8 | Inverting input |
| 9 | Power limit |
| 10 | V- |
| 11 | NC |
| 12 | Output 1 (emitter) |

## BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}= \pm 40 \mathrm{~V}$ unless otherwise specified. 1

| PARAMETER | TEST CONDITIONS | NE541 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Operating temperature range Operating supply voltage |  | $\begin{gathered} 0 \\ \pm 5 \end{gathered}$ |  | $\begin{aligned} & +70 \\ & \pm 40 \end{aligned}$ | $\begin{gathered} { }^{\circ} \mathrm{C} \\ \mathrm{~V} \end{gathered}$ |
| Quiescent current |  |  | 14 | 25 | mA |
| Input offset voltage Input offset current |  |  | $\begin{gathered} 7 \\ 0.5 \end{gathered}$ | $\begin{gathered} 10 \\ 1 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input bias current Input impedance | 40dB gain |  | $\begin{gathered} 2 \\ 20 \end{gathered}$ | 6 | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{k} \Omega \end{aligned}$ |
| Current gain <br> Gain variation over temperature range | 40dB gain | 70 | $\begin{gathered} 90 \\ \pm 0.1 \end{gathered}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Power supply rejection ratio Common mode rejection ratio | 40 dB gain | 60 | $\begin{aligned} & 70 \\ & 90 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Output drive current |  | 55 | 80 |  | mA |

NOTES

1. Heat sink tab is tied to substrate-do not ground or tie to any voltage.
2. Not exceeding maximum dissipation.

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}= \pm 40 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE541 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Frequency response Distortion | 40 dB gain $\pm 1 \mathrm{~dB}$ <br> 40 dB gain, Output 3dB below maximum, $R_{L}=600 \Omega$ |  | $\begin{aligned} & 100 \\ & 0.4 \end{aligned}$ | 1.0 | $\begin{gathered} \mathrm{kHz} \\ \% \end{gathered}$ |
| Equivalent input noise voltage | Rs $=600 \Omega, 50 \mathrm{~Hz}$ to 500 kHz |  | 10 |  | $\mu \mathrm{V}$ |

## DESCRIPTION

The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110 dB supply rejection and 70 dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing ( $V c c-2 V p-p$ ), and internal compensation to 10 dB . The NE542 operates from a single supply across the wide range of 9 to 24 V .

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplication of small signals.

## FEATURES

- Low noise-. $7 \mu \mathrm{~V}$ total input noise
- High gain-104dB open loop
- Single supply operation
- Wide supply range 9 to 24 V
- Power supply rejection 110 dB
- Large output voltage swing (Vcc-2V p-p)
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 100 kHz ( 15 V p-p)
- Internally compensated (stable at 10 dB )
- Short circuit protected
- High slew rate $5 \mathrm{~V} / \mu \mathrm{s}$

PIN CONFIGURATION


## EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | +24 | V |
| Power dissipation | 500 | mW |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (soldering, 60sec) | +300 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE542 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Supply voltage Supply current | $V_{C C}=9$ to $18 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty$ | 9 | 9 | $\begin{aligned} & 24 \\ & 12 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Input resistance Positive input Negative input |  |  | $\begin{aligned} & 100 \\ & 200 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| Output resistance | Open loop |  | 150 |  | $\Omega$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE542 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Voltage gain | Open loop |  | 160,000 |  | V/V |
| Input current Negative input |  |  | . 5 |  | $\mu \mathrm{A}$ |
| Output current | Source Sink (linear operation) | $\begin{aligned} & 8 \\ & 2 \end{aligned}$ | $\begin{gathered} 14 \\ 3 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Output voltage swing <br> Small signal bandwidth Slew rate Power bandwidth | $15 \mathrm{~V} p-\mathrm{p}$ | $V_{C C}-2.5$ | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}-2 \\ 15 \\ 5 \\ 100 \\ \hline \end{gathered}$ | . | V MHz $\mathrm{V} / \mu \mathrm{s}$ kHz |
| Maximum input voltage | Linear operation |  |  | 300 | mVrms |
| Supply rejection ratio <br> Channel separation | $\begin{gathered} f=60,120 \mathrm{~Hz} \\ f=1 \mathrm{kHz} \\ f=1 \mathrm{kHz} \end{gathered}$ |  | $\begin{gathered} 100 \\ 110 \\ 70 \\ \hline \end{gathered}$ |  | dB <br> dB <br> dB |
| Total harmonic distortion Total equivalent input Noise | $\begin{gathered} 75 \mathrm{~dB} \text { gain, } f=1 \mathrm{kHz} \\ \mathrm{RS}=600 \Omega, 100-10,000 \mathrm{~Hz} \end{gathered}$ |  | . 1 <br> .7 | 1,2 |  |
| Noise figure | $\begin{aligned} \mathrm{RS} & =50 \mathrm{k} \Omega, 10-10,000 \mathrm{~Hz} \\ \mathrm{RS} & =20 \mathrm{k} \Omega, 10 \quad 10,000 \mathrm{~Hz} \\ \mathrm{RS} & =10 \mathrm{k} \Omega, 10-10,000 \mathrm{~Hz} \\ \mathrm{RS} & =5 \mathrm{k} \Omega, 10-10,000 \mathrm{~Hz} \end{aligned}$ |  | $\begin{aligned} & 1.2 \\ & 1.2 \\ & 1.5 \\ & 2.4 \end{aligned}$ |  | dB <br> dB <br> dB <br> dB |

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## TYPICAL APPLICATIONS

## TYPICAL TAPE PLAYBACK AMPLIFIER



TWO-POLE FAST TURN-ON NAB TAPE PREAMP


NOTE: All resistors values are typical and in ohms.

R1AA MAGNETIC PHONO PREAMP


AUDIO MIXER


## DESCRIPTION

The 570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The 570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

## FEATURES

- Complete compressor and expandor in 1 IC
- Temperature compensated
- Greater than 110 dB dynamic range
- Operates down to 6 Vdc
- System levels adjustable with external components
- Distortion may be trimmed out


## CIRCUIT DESCRIPTION

The 570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.
The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at $V_{\text {REF }}$. The rectified current is averaged on an external filter capacitor tied to the $C_{\text {RECT }}$ terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than $.1 \mu \mathrm{~A}$.

$$
\begin{aligned}
& G \propto \frac{\left|V_{I N}-V_{R E F}\right| \text { ave }}{R_{1}} \\
& G \propto \frac{\left|V_{I N}\right| \text { ave }}{R_{1}}
\end{aligned}
$$

or

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or com-

## APPLICATIONS

- Telephone trunk compandor-570
- Telephone subscriber compandor-571
- High level limiter
- Low level expandor-noise gate
- Dynamic noise reduction systems
- Voltage controlled amplifier
- Dynamic filters


## PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Positive supply |  | Vdc |
|  | 570 | 24 |
| TA | 571 | 18 |
| PD | Operating temperature range | -40 to +70 |

## BLOCK DIAGRAM


pressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$
\begin{aligned}
& \mathrm{G}(\mathrm{t})=\left(\mathrm{G}_{\text {initial }}-\mathrm{G}_{\text {final }}\right) \mathrm{e}^{-\mathrm{t} / \tau} \\
& +\mathrm{G}_{\text {final }} ; \tau=10 \mathrm{~K} \times \mathrm{C}_{\text {RECT }}
\end{aligned}
$$

The variable gain cell is a current in, current out device with the ratio IOUT/I IN controlled by the rectifier. IIN is the current which flows from the $\Delta G$ input to an internal summing node biased at $V_{\text {REF }}$. The following equation applies for capacitively coupled inputs. The output current, IOUT, is fed to the summing node of the op amp.

$$
I_{I N}=\frac{V_{I N}-V_{\text {REF }}}{R_{2}}=\frac{V_{I N}}{R_{2}}
$$

A compensation scheme built into the $\Delta G$ cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to $V_{\text {REF }}$, and the inverting input connected to the $\Delta G$ cell output as well as brought out externally. A resistor, $\mathrm{R}_{3}$, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components. The output stage is capable of $\pm 20 \mathrm{~mA}$ output current. This allows a $+13 \mathrm{dBm}(3.5 \mathrm{~V}$ rms) output into a $300 \Omega$ load which, with a series resistor and proper transformer, can result in +13 dBm with a $600 \Omega$ output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and $\Delta G$ cell, and a bias current for the $\Delta G$ cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

## TYPICAL PERFORMANCE

 CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$

| PARAMETER | TEST CONDITIONS | NE570 |  |  | NE571 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $V_{\text {CC }}$ Supply voltage |  | 6 |  | 24 | 6 |  | 18 | V |
| ${ }^{1} \mathrm{CC}$ Supply current | No signal |  | 3.2 | 4.0 |  |  |  | mA |
| Output current capability |  | $\pm 20$ |  |  |  |  |  | mA |
| Output slew rate |  |  | $\pm .5$ |  |  |  |  | V/us |
| Gain cell distortion ${ }^{2}$ | Untrimmed |  | . 3 | 1.0 |  | . 5 | 2.0 | \% |
|  | Trimmed |  | . 05 |  |  | . 1 |  |  |
| Resistor tolerance |  |  | $\pm 5$ | $\pm 15$ |  |  |  | \% |
| Internal reference voltage |  | 1.7 | 1.8 | 1.9 | 1.65 | 1.8 | 1.95 | V |
| Output dc shift ${ }^{3}$ | Untrimmed |  | $\pm 20$ | $\pm 50$ |  | $\pm 30$ | $\pm 100$ | $m V$ |
| Expandor output noise | No signal, $20 \mathrm{~Hz}-20 \mathrm{kHz}$ |  | 20 |  |  |  |  | $\mu \mathrm{V}$ |
|  |  |  | -15 |  |  |  |  | dBRNC |
| Unity gain level |  | -1 | 0 | +1 | -1.5 | 0 | +1.5 | dBm |
| Gain change ${ }^{2,4}$ | $-40^{\circ} \mathrm{C}<\mathrm{T}<70^{\circ} \mathrm{C}$ |  | $\pm .1$ | $\pm .3$ |  | $\pm .1$ | $\pm .5$ | dB |
|  | $0^{\circ} \mathrm{C}<\mathrm{T}<70^{\circ} \mathrm{C}$ |  | $\pm .1$ | $\pm .2$ |  | $\pm .1$ | $\pm .4$ |  |
| Reference drift ${ }^{4}$ | $-40^{\circ} \mathrm{C}<\mathrm{T}<70^{\circ} \mathrm{C}$ |  | +2, -25 | -10, -40 |  | $+2,-25$ | $+20,-50$ | mV |
|  | $0^{\circ} \mathrm{C}<\mathrm{T}<70^{\circ} \mathrm{C}$ |  | $\pm 5$ | $\pm 10$ |  | $\pm 5$ | $\pm 20$ |  |
| Resistor drift ${ }^{4}$ | $-40^{\circ} \mathrm{C}<\mathrm{T}<70^{\circ} \mathrm{C}$ |  | +8,-0 |  |  |  |  | \% |
|  | $0^{\circ} \mathrm{C}<\mathrm{T}<70^{\circ} \mathrm{C}$ |  | +1,-0 |  |  |  |  |  |
| Tracking error ${ }^{5}$ | Rectifier input= |  |  |  |  |  |  | dB |
|  | +6dBm |  | $\pm .2$ |  |  |  |  |  |
|  | -10dBm |  | +. 2 | $-.2,+.4$ |  | +. 2 | $-.2,+.5$ |  |
|  | -20dBm |  | +. 2 | $-.3,+.6$ |  | +. 2 | $-.4,+.7$ |  |
|  | -30dBm |  | +. 2 | $-.5,+1$ |  | +. 2 | $-1,+1.5$ |  |
|  | -40dBm |  | +.2,-. 4 |  |  | +.2,-. 4 |  |  |

## NOTES

1. Except where indicated, the 571 specifications are identical to the 570

Measured at OdBm
3. Expandor ac input change from no signal to OdBm
4. Relative to value at $T_{A}=25^{\circ} \mathrm{C}$
5. Relative to OdBm

## sECTION IS RADIO CIRCUITS

## DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.
The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8 to +18 volts.
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.

## FEATURES

- Exceptional limiting sensitivity: $10 \mu \mathrm{~V}$ typ. at -3dB point
- Low distortion: $0.1 \%$ typ. (with doubletuned coil)
- Single-coil tuning capability
- High recovered audio: 400 mV typ.
- Provides specific signal for control of interchannel muting (squelch)
- Provides specific signal for direct drive of a tuning meter
- Provides delayed AGC voltage for RF amplifier
- Provides a specific circuit for flexible AFC
- Internal supply/voltage regulators


## APPLICATIONS

- High-fidelity FM receivers
- Automotive FM receivers
- Communications FM receivers


## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| DC supply voltage: |  |  |
| Between terminals 11 and 4 | 18 | V |
| Between terminals 11 and 14 | 18 | mA |
| DC Current (out of terminal 15) | 2 | mW |
| Device dissipation: | 600 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Up to $T_{A}=60^{\circ} \mathrm{C}$ | derate linearly |  |
| Above $\mathrm{T}_{\mathrm{A}}=60^{\circ} \mathrm{C}$ | 6.7 | ${ }^{\circ} \mathrm{C}$ |
| Ambient temperature range: | -40 to +85 |  |
| Operating <br> Storage | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (during soldering): | +265 |  |
| At distance not less than 1/32" $(0.79 \mathrm{Cm})$ <br> from case for 10 seconds max. |  |  |

## BLOCK DIAGRAM



EQUIVALENT SCHEMATIC


[^6]DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | CA3089 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| STATIC (DC) CHARACTERISTICS <br> $l_{11}$ Quiescent circuit current <br> DC Voltages: 4 <br> $\mathrm{V}_{1} \quad$ Terminal 1 (IF input) | No signal input, non-muted <br> No signal input, non-muted | $\begin{array}{r} 16 \\ 1.2 \end{array}$ | $\begin{aligned} & 23 \\ & 1.9 \end{aligned}$ | 30 <br> 2.4 | $\begin{gathered} \mathrm{mA} \\ \mathrm{~V} \end{gathered}$ |
| $V_{2}$ Terminal 2 (ac return to input) <br> $V_{3}$ Terminal 3 (dc bias to input) | No signal input, non-muted No signal input, non-muted | $\begin{aligned} & 1.2 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 1.9 \end{aligned}$ | $\begin{aligned} & 2.4 \\ & 2.4 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{6}$ Terminal 6 (audio output) <br> $\mathrm{V}_{7}$ Terminal 7 (A.F.C.) <br> $\mathrm{V}_{10}$ Terminal 10 (dc reference) | No signal input, non-muted No signal input, non-muted No signal input, non-muted | $\begin{aligned} & 5.0 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 5.6 \\ & 5.6 \\ & 5.6 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 6.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| DYNAMIC CHARACTERISTICS <br> $\mathrm{V}_{1(\text { lim })} \quad$ Input limiting voltage ( -3 dB point) ${ }^{3}$ |  |  | 10 | 25 | $\mu \mathrm{V}$ |
| AMR AM Rejection (terminal 6)4 <br> Vo Recovered audio voltage (terminal 6)3 | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=0.1 \mathrm{~V}, \mathrm{~F}_{\mathrm{O}}=10.7 \mathrm{MHz} \\ f_{\bmod }=400 \mathrm{~Hz}, \mathrm{AM} \operatorname{Mod}=30 \% \end{gathered}$ | $\begin{gathered} 45 \\ 300 \end{gathered}$ | $\begin{gathered} 55 \\ 400 \end{gathered}$ | 500 | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{mV} \end{aligned}$ |
| Total harmonic distortion:1  <br> THD Single tuned (terminal 6)3 <br> THD Double tuned (terminal 6) 4 | $f_{\text {mod }}=400 \mathrm{~Hz}, \mathrm{~V}_{1 \mathrm{~N}}=0.1$ |  | $\begin{aligned} & 0.5 \\ & 0.1 \\ & \hline \end{aligned}$ | 1.0 | $\begin{aligned} & \% \\ & \% \\ & \hline \end{aligned}$ |
| $\begin{array}{ll}S+N / N & \text { Signal plus noise to noise ratio (terminal 6)3 } \\ M U_{\text {IN }} & \text { Mute input (terminal 5) }\end{array}$ | $\begin{gathered} \text { Deviation }= \pm 75 \mathrm{kHz} \\ V_{5}=2.5 \mathrm{~V} \end{gathered}$ | 60 | $\begin{aligned} & 67 \\ & 70 \end{aligned}$ |  | dB <br> dB |
| MUOUT Mute output (terminal 12) | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=50 \mu \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V} \end{gathered}$ | 4.0 |  | . 5 | $\begin{aligned} & \hline \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| MTR Meteroutput (terminal 13) | $\begin{gathered} V_{I N}=0.1 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IN}}=500 \mu \mathrm{~V} \\ \mathrm{~V}_{\text {IN }}=0 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 1.5 \end{aligned}$ | . 7 | $V$ $V$ $V$ |
| AGC Delayed AGC (terminal 15) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=0.1 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IN}}=10 \mu \mathrm{~V} \end{aligned}$ | 4.0 | 5.0 | . 5 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| THD Double tuned (terminal 6)4 | $\begin{gathered} f_{\text {mod }}=400 \mathrm{~Hz} \\ \mathrm{~V}_{\mathrm{IN}}=0.1 \end{gathered}$ |  | 0.1 |  | \% |

NOTES

1. THD characteristics and Audio Level are essentially a function of the phase and $Q$ characteristics of the network connected between terminals 8,9 and 10.
Test circuit Figure 1.
2. Test circuit Figure 2.
3. Test circuit Figures 1 and 2.

## TEST CIRCUITS



## SYSTEM DESIGN <br> CONSIDERATIONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input by-pass capacitors should be located close to the input terminals and the values should not be
large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good bypass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.
The input impedance of the CA3089 is approximately 10,000 ohms. It is not recommended to match this impedance. The value

NOTES: All resistors values are typical and in ohms.

1. Waller 4SN3FIC or equivalent
2. Murate SFG 10.7 mA or equivalent
3. Rs will affect stability depending on circuit layout. To increase stability RS is decreased. Range of RS is 330 to $50 \Omega, R_{1}+R_{s} \leq 330 \Omega$
4. L tunes with $100 \mathrm{pF}(\mathrm{C})$ at 10.7 MHz Qo unloaded $\cong 75$ (G.I. EX2274I or equivalent)

Performance data at $\mathrm{f}_{0}=98 \mathrm{MHz}, \mathrm{f}_{\mathrm{MOD}}=400 \mathrm{~Hz}$, deviation $=$ $\pm 74 \mathrm{kHz}$ :
-3 dB limiting sensitivity $\quad 2 \mu \mathrm{~V}$ (antenna level)
20 dB quieting sensitivity $\quad 1 \mu \mathrm{~V}$ (antenna level) 30 dB quieting sensitivity $\quad 1.5 \mu \mathrm{~V}$ (antenna level)
of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

## TYPICAL PERFORMANCE CHARACTERISTICS



## TEST CIRCUITS



## *NOTE

L tunes with 100 pF (C) at 10.7 MHz .
All resistors values are typical and in ohms.
$Q_{0}($ unloaded $) \cong 75$ (G.I. automatic mfg. div. EX22741 or equivalent).

*NOTE: All resistors values are typical and in ohms.
T: Pri. - Qo (unloaded) $\cong 75$ (tunes with 100 pF (C1) $20 \dagger$ of 34 e on $7 / 32^{\prime \prime}$ dia. form) Sec. - Qo (unloaded) $\cong 75$ (tunes with $100 \mathrm{pF}(\mathrm{C} 2) 20 \dagger$ of 34 e on $7 / 32$ " dia. form) $k Q$ (percent of critical coupling) $>70 \%$
(Adjusted for coil voltage $\mathrm{V}_{\mathrm{C}}$ ) $=150 \mathrm{mV}$
Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4 mm

Figure 2

## DESCRIPTION

The 5596 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The S5596 will operate over the full military temperature range of $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. The N5596 is intended for applications within the range of $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$.

## APPLICATIONS

- Suppressed carrier and amplitude modulation
- Synchronous detection
- FM detection
- Phase detection
- Sampling
- Single sideband
- Frequency doubling


## FEATURES

- Excellent carrier suppression 65dB typ @ 0.5MHz 50dB typ @ 10MHz
- Adjustable gain and signal handling
- Balanced inputs and outputs
- High common-mode rejection-85dB typ


## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Applied voltage1,2 | 30 | V |
| Differential input signal $\left(\mathrm{V}_{7}-\mathrm{V}_{8}\right)$ | $\pm 5.0$ | V |
| Differential input signal $\left(\mathrm{V}_{4}-\mathrm{V}_{1}\right)$ | $\left(5 \pm I_{5} \mathrm{R}_{\mathrm{e}}\right)$ | V |
| Input signal $\left(\mathrm{V}_{2}-\mathrm{V}_{1}, \mathrm{~V}_{3}-\mathrm{V}_{4}\right)$ | 5.0 | V |
| Bias current $\left(\mathrm{I}_{5}\right)$ | 10 | mA |
| Power dissipation (pkg. limitation) | 680 | mW |
| K package | 5.4 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Derate above $25^{\circ} \mathrm{C}$ | 900 | mW |
| A package (TO-116) | 7.2 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Derate above $25^{\circ} \mathrm{C}$ | ${ }^{\circ} \mathrm{C}$ |  |
| Operating temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -65 to +150 |  |

[^7]PIN CONFIGURATIONS



## K PACKAGE

5596, MC1496, MC1596 (Top View)

$\qquad$

DC ELECTRICAL CHARACTERISTICS $\mathrm{V}^{+}=+12 \mathrm{Vdc}, \mathrm{V}^{-}=-9.0 \mathrm{Vdc}, \mathrm{I}_{5}=1.0 \mathrm{mAdc}, \mathrm{R}_{\mathrm{L}}=3.9 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{e}}=1.0 \mathrm{k} \Omega$, $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | MC1596 |  |  | MC1496/5596 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \mathrm{R}_{\mathrm{ip}} \\ & \mathrm{C}_{\mathrm{ip}} \\ & \hline \end{aligned}$ | Single-ended input impedance Parallel input resistance Parallel input capacitance |  | Signal port, $\mathrm{f}=5.0 \mathrm{MHz}$ |  | $\begin{array}{r} 200 \\ 2.0 \\ \hline \end{array}$ |  |  | $\begin{array}{r} 200 \\ 2.0 \\ \hline \end{array}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \mathrm{R}_{\mathrm{op}} \\ & \mathrm{C}_{\mathrm{op}} \end{aligned}$ | Single-ended output impedance Parallel output resistance Parallel output capacitance | $\mathrm{f}=10 \mathrm{MHz}$ |  | $\begin{aligned} & 40 \\ & 5.0 \end{aligned}$ |  |  | $\begin{aligned} & 40 \\ & 5.0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \end{aligned}$ |
| lbs lbc | Input bias current $\begin{aligned} & I_{b s}=\frac{I_{1}+I_{4}}{2} \\ & I_{b s}=\frac{I_{7}+I_{8}}{2} \end{aligned}$ |  |  | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ |  | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| $\begin{aligned} & \mathrm{lios} \\ & \mathrm{lioC} \end{aligned}$ | Input offset current $\begin{aligned} & I_{\text {ioS }}=I_{1}-I_{4} \\ & I_{\text {ioC }}=I_{7}-I_{8} \end{aligned}$ |  |  | $\begin{aligned} & 0.7 \\ & 0.7 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ |  | $\begin{aligned} & 0.7 \\ & 0.7 \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 7.0 \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| Tclio <br> 100 | Average temperature coefficient of input offset current Output offset current $1_{6}-1_{9}$ | $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  | $\begin{gathered} 2.0 \\ 14 \end{gathered}$ | 50 |  | 2.0 <br> 15 | 80 | $n A /{ }^{\circ} \mathrm{C}$ <br> $\mu \mathrm{A}$ |
| Tcloo $V_{0}$ | Average temperature coefficient of output offset current Common-mode quiescent Output voltage (Pin 6 or Pin 9) | $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  | $\begin{aligned} & 90 \\ & 8.0 \end{aligned}$ |  |  | $\begin{aligned} & 90 \\ & 8.0 \end{aligned}$ |  | $\mathrm{nA} /{ }^{\circ} \mathrm{C}$ <br> Vdc |
| $\begin{aligned} & \mathrm{ld}+ \\ & \mathrm{l}- \end{aligned}$ | Power supply current $I_{6}+I_{9}$ $l_{10}$ |  |  | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 4.0 \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 4.0 \\ & 5.0 \end{aligned}$ | mAdc |
| PD | DC power dissipation |  |  | 33 |  |  | 33 |  | mW |

NOTE
Pin number references pertain to K package pinout only.


SIGNAL GAIN AND OUTPUT SWING


AC ELECTRICAL CHARACTERISTICS
$\mathrm{V}^{+}=+12 \mathrm{Vdc}, \mathrm{V}^{-}=-9.0 \mathrm{Vdc}, \mathrm{I}_{5}=1.0 \mathrm{mAdc}, \mathrm{R}_{\mathrm{L}}=3.9 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{e}}=1.0 \mathrm{k} \Omega$,
$\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | MC1596 |  |  | MC1496/5596 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| VCFT | Carrier feedthrough |  | $\mathrm{V}_{\mathrm{C}}=60 \mathrm{mVrms}$ sinewave and offset adjusted to zero $\begin{aligned} & \mathrm{fC}=1.0 \mathrm{kHz} \\ & \mathrm{fc}=10 \mathrm{MHz} \end{aligned}$ <br> $\mathrm{V}_{\mathrm{c}}=300 \mathrm{mVp}-\mathrm{p}$ squarewave: <br> Offset adjusted to zero $\mathrm{fC}_{\mathrm{C}}=1.0 \mathrm{kHz}$ Offset not adjusted $\mathrm{f}_{\mathrm{C}}=1.0 \mathrm{kHz}$ |  | $\begin{gathered} 40 \\ 140 \\ \\ 0.04 \\ 20 \end{gathered}$ | $\begin{aligned} & 0.2 \\ & 100 \end{aligned}$ |  | $\begin{gathered} 40 \\ 140 \\ \\ 0.04 \\ 20 \end{gathered}$ | $\begin{gathered} 0.4 \\ 200 \end{gathered}$ | $\mu$ Vrms <br> mVrms |
| Vcs | Carrier suppressions | $\mathrm{f}_{\mathrm{S}}=10 \mathrm{kHz}, 300 \mathrm{mVrms}$ sinewave $\mathrm{fc}=500 \mathrm{kHz}, 60 \mathrm{mVrms}$ sinewave $\mathrm{f}_{\mathrm{C}}=10 \mathrm{MHz}, 60 \mathrm{mVrms}$ sinewave | 50 | $\begin{aligned} & 65 \\ & 50 \end{aligned}$ |  | 40 | $\begin{aligned} & 65 \\ & 50 \\ & \hline \end{aligned}$ |  | dB |
| $\mathrm{BW}_{3 \mathrm{~dB}}$ | Transadmittance bandwidth (Magnitude) ( $\mathrm{R}_{\mathrm{L}}=50 \Omega$ ) | Carrier input port, $\mathrm{V}_{\mathrm{C}}=60 \mathrm{mVrms}$ sinewave fs $=1.0 \mathrm{kHz}$, 300 mVrms sinewave <br> Signal input port, $\mathrm{V}_{\mathrm{S}}=300 \mathrm{mVrms}$ sinewave $\left\|\mathrm{V}_{\mathrm{C}}\right\|=0.5 \mathrm{Vdc}$ |  | $\begin{aligned} & 300 \\ & 80 \end{aligned}$ |  |  | $\begin{aligned} & 300 \\ & 80 \end{aligned}$ |  | $\mathrm{MHz}$ $\mathrm{MHz}$ |
| $\mathrm{AV}_{\mathrm{S}}$ | Signal gain | $\begin{gathered} \mathrm{V}_{\mathrm{s}}=100 \mathrm{mVrms} ; \mathrm{f}=1.0 \mathrm{kHz} \\ \|\mathrm{VC}\|=0.5 \mathrm{Vdc} \end{gathered}$ | 2.5 | 3.5 |  | 2.5 | 3.5 |  | V/v |
| $\begin{aligned} & \text { CMV } \\ & \text { ACM } \end{aligned}$ | Common-mode input swing Common-mode gain | Signal port, $\mathrm{f}_{\mathrm{s}}=1.0 \mathrm{kHz}$ <br> Signal port, fs $=1.0 \mathrm{kHz}$ $\|\mathrm{V}\|=0.5 \mathrm{Vdc}$ |  | $\begin{gathered} 5.0 \\ -85 \end{gathered}$ |  |  | $\begin{gathered} 5.0 \\ -85 \end{gathered}$ |  | $\begin{gathered} \mathrm{Vp-p} \\ \mathrm{~dB} \end{gathered}$ |
| DVOUT | Differential output voltage swing capability |  |  | 8.0 |  |  | 8.0 |  | Vp-p |

NOTE
Pin number references pertain to $K$ package pinout only.

CARRIER REJECTION AND SUPPRESSION


## DESCRIPTION

The NE546 is a monolithic integrated circuit that provides an RF amplifier, IF amplifier, mixer, oscillator, AGC detector, and voltage regulator in a single IC. The primary application is super heterodyne AM radio receiver particularly in automobile radios. The NE546 is available in a 14 lead dual inline package.

## FEATURES

- Low noise
- Build in AGC circuit
- Separately accessable amplifiers
- Mixer-oscillator stage with internal feedback
- High selectivity
- High image rejection

PIN CONFIGURATION

| N PACKAGE |  |  |  |
| :---: | :---: | :---: | :---: |
| MIXER <br> INPUT 1 $\qquad$ |  | 14 | MIXER OUTPUT |
| oscillator 2 |  | 13 | RF output |
| SUPPLY 3 |  | 12 | rfinput |
| MIXER ${ }_{\text {M }}$ |  | 1. | RF decouple |
| detector INPUT |  | 10 | AGC FILTER |
| IF OUTPUT 6 |  | 9 | ground 1 |
| IFINPUT 7 |  | 8 | Ground 2 |
| ORDER PART NO. NE546N |  |  |  |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING |
| :---: | :---: | :---: |
| VCC | Supply voltage pins $3,13,14$ <br> at pin 6 | 16 |
|  | Supply voltage (V+) |  |
| DC | Supply current |  |
|  | Internal power dissipation* | 35 |
|  | Lead temperature | 750 |
|  | Operating temperature range | 300 |
|  | Storage temperature range | -40 to +85 |
|  | -65 to +150 | mW |
|  |  | ${ }^{\circ} \mathrm{C}$ |
|  |  | ${ }^{\circ} \mathrm{C}$ |

*NOTE
Rating applies for temperatures up to $55^{\circ} \mathrm{C}$.
Derate linearly at $6.67 \mathrm{nW} /{ }^{\circ} \mathrm{C}$ above $55^{\circ} \mathrm{C}$.

NE546

## EQUIVALENT SCHEMATIC



## DC ELECTRICAL CHARACTERISTICS

| PARAMETER |  | TEST CONDITIONS | NE546 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| DC VOLTAGE $+\mathrm{Vcc}$ $\operatorname{Vos}_{0}\left(V_{1}-\mathrm{V}_{4}\right)$ | Supply voltage Mixer balance |  |  | 9.0 | 1.0 | 15.0 | mV |
| $\begin{aligned} & \hline \mathrm{V}_{3} \\ & \mathrm{~V}_{5} \end{aligned}$ | Zener voltage: at terminal 5 AGC voltage | . | $\begin{aligned} & \hline 5.5 \\ & 0.1 \end{aligned}$ | $\begin{gathered} \hline 6.0 \\ 0.25 \end{gathered}$ | $\begin{aligned} & \hline 7.0 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \mathrm{v} \\ & \mathrm{v} \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{V}_{7} \\ & \mathrm{~V}_{12} \\ & \mathrm{~V}_{13} \end{aligned}$ | Pin 7 voltage Pin 12 voltage Pin 13 voltage |  | $\begin{gathered} 0.55 \\ 0.6 \end{gathered}$ | $\begin{aligned} & \hline 0.70 \\ & 0.71 \\ & 4.0 \end{aligned}$ | $\begin{gathered} \hline 0.80 \\ 0.8 \end{gathered}$ | $\begin{aligned} & \hline v \\ & v \\ & v \end{aligned}$ |
| ```DC CURRENT Icc I``` | Supply current Oscillator current |  | 15 | $\begin{aligned} & 18 \\ & 1.0 \end{aligned}$ | 22 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \hline I_{3} \\ & I_{6} \end{aligned}$ | Zener current IF current |  | $\begin{aligned} & \hline 12 \\ & 3.5 \end{aligned}$ | $\begin{aligned} & 14 \\ & 4.3 \end{aligned}$ | $\begin{gathered} 16 \\ 6 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \mathrm{I}_{13} \\ & \mathrm{I}_{14} \\ & \hline \end{aligned}$ | RF current Mixer current |  |  | $\begin{gathered} \hline 4.0 \\ 0.17 \end{gathered}$ | $\begin{gathered} 5 \\ 0.38 \\ \hline \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \text { STATIC } \\ & \mathrm{V}_{6} \end{aligned}$ | I.F. breakdown and linearity | Apply 5 volts to pin 6 only. $\mathrm{V}_{\mathrm{CC}}=0$ volts. Measure pin 6. | 400 | 500 | 600 | $\mu \mathrm{A}$ |
| V6 | I.F. breakdown and linearity | Apply 25 volts to pin 6 only. $\mathrm{V}_{\mathrm{CC}}=0$ volts. Measure pin 6.* | 2.0 | 2.5 | 3.0 | mA |

## AC ELECTRICAL CHARACTERISTICS

|  | PARAMETER | TEST CONDITIONS | NE546 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| $V_{\text {sat }}$ | Saturation | Per sensitivity test interrupting input signal measure output voltage. | 500 |  |  | mV |
| $V_{\text {sen }}$ | Sensitivity | Input signal to dummy antenna at $\mathrm{f}_{\mathrm{IN}}=1 \mathrm{MHz}, 30 \%$ AM modulation at $\mathrm{f}_{\mathrm{MOD}}=400 \mathrm{~Hz}$, for 11 mV output at $\mathrm{V}_{0}$. |  | 2.5 | 5 | $\mu \mathrm{A}$ |
| S/N | Signal-to-noise ratio | Ratio of output at $\mathrm{V}_{0}$ with modulation ON and then OFF, input signal $=100 \mu \mathrm{~V}$, $30 \%$ AM modulation at $\mathrm{f}_{\mathrm{MOD}}=400 \mathrm{~Hz}$. | 34 |  |  | dB |
| Dist. | Overload distortion | Input signal set at $1 \mathrm{MHz}, 90 \%$ AM modulation, distortion at $\mathrm{V}_{0}$ must be $10 \%$. | 100 | 155 | 250 | mV |

note
Performance characteristics in circuit of Figure 3.
TYPICAL PERFORMANCE CHARACTERISTICS


AGC CURVE



SIGNAL TO NOISE RATIO

rf signal input voltage (nv)

NOTE
$R x$ is external resistor between pins 3 and $V$ supply.

TYPICAL APPLICATIONS
AM RADIO (Capacitor Tuned)


VARIABLE CAPACITOR (Air Varicon)
ANT \& RF

$$
13 \mathrm{pF} \sim 190 \mathrm{pF}
$$

$$
12 \mathrm{pF} \sim 80 \mathrm{pF}
$$

ANTENNA COIL
$10 \mathrm{~mm} \phi<120 \mathrm{~mm}$ Ferrite Antenna


1st. IF COIL


2nd. IF COIL


Figure 1

## OBJECTIVE SPECIFICATION

## FEATURES

- Single crystal ( 10.24 MHz )
- Generates both receive L.O.'s for dual conversion plus transmit frequency
- Binary input
- ROM programmed
- Up to 64 channel capability
- High or low side L.O. injection
- Wide supply range: $\mathbf{8 V} \rightarrow \mathbf{1 6 V}$
- Single line T/R programming
- Regulated 5 volt output ( 10 mA )
- Internal transmit squelch


## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Power supply | 16 | V |
| Max. VCO input frequency | 40 | MHz |
| Reference frequency | 10.24 | MHz |
| Logic input current | 1 | $\mu \mathrm{~A}$ |

## TYPICAL APPLICATION



## DESCRIPTION

TCA440 is a monolithic IC, especially developed for AM receivers up to 50 MHz . It includes a RF stage with AGC, a balanced mixer, separate oscillator and an IF amplifier with AGC. Because of its low current consumption and of its internal stabilization the TCA440 is perfectly suited for battery operated portables, car and home radios.

## FEATURES

- Balanced circuit
- Separately controllable prestage
- Multiplicative push-pull mixer with separate oscillator
- High signal handling capability even with 4.5 V supply voltage
- 100 dB feedback control range in 5 stages
- Direct connection for tuning meter
- Minimum external components

ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :--- | :--- | :---: | :---: |
| $V_{c C}$ | Supply voltage | 15 | V |
| $\mathrm{~T}_{\mathrm{amb}}$ | Ambient temperature in operation | -15 to +80 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{s}}$ | Storage temperature | -30 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{CC}}$ | Range of operation | 4.5 to 15 | V |

BLOCK DIAGRAM


PIN CONFIGURATION


## TUNING METER

Recommended instruments:

$$
\begin{aligned}
& \text { or } \quad 500 \mu \mathrm{~A}\left(R_{1}=800 \mathrm{k} \Omega\right) \\
& 300 \mu \mathrm{~A}\left(\mathrm{R}_{1}=1.5 \mathrm{k} \Omega\right)
\end{aligned}
$$

The IC offers at pin 10 a tuning meter voltage of 600 mV EMP max. with a source impedance of approx. $400 \Omega$.

## FUNCTION

As pictured in the circuit diagram the TCA440 comprises two control loops independent of each other which control the RF stage and the IF stages. By AGCing the RF stage, excellent signal handling is obtained. A voltage of 2.6 V pp on the IC input can be handled with very low distortion. The pushpull mixer operates multiplicatively, thereby resulting in few harmonic mixing products and whistling points. The oscillator which is separated from the mixer is also apted excellently for short waves. From the AGC of the RF amplifier a voltage is derived for a tuning meter which can be connected directly to the meter. The symmetric composition of the circuit provides high stability against oscillation and, at the same time, an AGC range of more than 100 dB . The bridge circuit of the mixer provides good isolation of the oscillator.

## EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V_{C C}=9 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | TCA 440 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Icc | Total current consumption at: | $\begin{gathered} V_{C C}=4.5 \mathrm{~V} \\ V_{C C}=9 \mathrm{~V} \\ V_{C C}=15 \mathrm{~V} \end{gathered}$ |  | $\begin{gathered} 7 \\ 10.5 \\ 12 \end{gathered}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS $\mathrm{V}_{C C}=9 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{f}_{\mathrm{I} R F}=600 \mathrm{kHz}$, food $=1 \mathrm{kHx}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TCA 440 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\Delta \mathrm{G}_{\mathrm{RF}}$ | RF level deviation for ( $m=80 \%$ ) |  | $\begin{gathered} \Delta V_{\mathrm{AF}}=6 \mathrm{~dB} \\ \Delta \mathrm{~V}_{\mathrm{AF}}=10 \mathrm{~dB} \end{gathered}$ |  | $\begin{aligned} & 65 \\ & 80 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| $\mathrm{V}_{\text {AFeff }}$ | AF output voltage for VIRF (symm. measured at 1-2) | $\begin{array}{r} m=80 \% \quad V_{\text {IRF }}=20 \mu \mathrm{~V} \\ V_{\text {IRF }}=1 \mathrm{mV} \\ V_{\text {IRF }}=500 \mathrm{mV} \\ \mathrm{~m}=30 \% V_{\text {IRF }}=20 \mu \mathrm{~V} \\ V_{\text {IRF }}=1 \mathrm{mV} \\ \mathrm{IRF}^{2}=500 \mathrm{~V} \end{array}$ |  | $\begin{gathered} \hline 140 \\ 260 \\ 350 \\ 50 \\ 100 \\ 130 \end{gathered}$ |  | mV <br> $m V$ |
| VIRF | Input sensitivity (measured at $60 \Omega, \mathrm{f}_{\mathrm{IRF}}=1 \mathrm{MHz}$, $\left.\mathrm{m}=30 \% / 0 \%, \mathrm{R}_{\mathrm{G}}=540 \Omega\right)$ | At signal-to-noise distance $\begin{aligned} & \frac{S+N}{N}=6 \mathrm{~dB} \\ & \frac{S+N}{N}=26 \mathrm{~dB} \\ & \frac{S+N}{N}=58 \mathrm{~dB} \end{aligned}$ |  | $1$ |  | $\mu \mathrm{V}$ <br> $\mu \mathrm{V}$ <br> mV |
| RF unit figF $\mathrm{f}_{\mathrm{IF}}$ $\Delta \mathrm{Gv}$ Virfpp | Input frequency range <br> Output frequency <br> Control range <br> Input voltage | $\begin{gathered} f_{I F}=f o s C=f_{I R F} \\ \text { for } 600 \mathrm{kHz}, m=80 \% \text {, for } \\ \text { Overdrive, } k_{A F}=10 \%, \\ \text { Symmetrically measured at pins } 1 \& 2 \\ \text { (mean carrier value) } \end{gathered}$ |  | $\begin{gathered} 0 \text { to } 50 \\ 460 \\ 38 \\ 2.6 \end{gathered}$ |  | $\begin{gathered} \mathrm{MHz} \\ \mathrm{kHz} \\ \mathrm{~dB} \\ \mathrm{Vpp} \end{gathered}$ |
| ViRFeff SIF $Z_{1}$ | IF suppression between 1-2 to 15 RF input impedance <br> Mixer output impedance | Asymmetrical coupling at: <br> GRFmax <br> $G_{\text {RFmin }}$ <br> Symmetrical coupling at: <br> $G_{\text {RFmax }}$ <br> GRFmin <br> Pins 15 or 16 |  | $\begin{gathered} .5 \\ 20 \\ 2 / 5 \\ 2.2 / 1.5 \\ 4 / 5 \\ 4.5 / 1.5 \\ 250 / 4.5 \end{gathered}$ |  | v <br> dB <br> $\mathrm{k} \Omega / \mathrm{pF}$ <br> $\mathrm{k} \Omega / \mathrm{pF}$ <br> k $\Omega / \mathrm{pF}$ <br> $\mathrm{k} \Omega / \mathrm{pF}$ <br> $\mathrm{k} \Omega / \mathrm{pF}$ |
| IF unit  <br> $f_{I I F}$ Input frequency range <br> $\Delta G_{V}$ Control range at 460 kHz <br> $\mathrm{V}_{\text {IFeff }}$ Input voltage |  | Mean carrier value at $\mathrm{G}_{\text {min }}$ for Overdrive ( $\mathrm{k}_{\mathrm{AF}}=10 \%$ ), measured at Pin $12(60 \Omega$ to ground, $\mathrm{f}_{\mathrm{IF}}=460 \mathrm{kHz}, \mathrm{m}=80 \%, \mathrm{f}_{\mathrm{mod}}=1 \mathrm{kHz}$ ) <br> $V_{\text {IIF }}$ at $60 \Omega$ (Pin 12) $f_{\text {mod }}=1 \mathrm{kHz}$ $\begin{aligned} & V_{I F}=30 \mu V, m=80 \% \\ & V_{I F}=3 \mathrm{mV}, m=80 \% \\ & V_{I F}=3 \mathrm{mV}, \mathrm{~m}=30 \% \end{aligned}$ <br> Asymmetrical coupling Pin 7 |  |  |  |  |
|  |  |  | $\begin{gathered} 0 \text { to } 2 \\ 62 \\ 200 \end{gathered}$ |  | MHz dB mV |  |
| $V_{\text {AFeff }}$ | AF output voltage |  |  | $\begin{gathered} 50 \\ 200 \\ 70: \end{gathered}$ |  | $\begin{aligned} & m V \\ & m V \\ & m V \end{aligned}$ |
| $\begin{aligned} & \mathrm{Z}_{\mathrm{l}} \\ & \mathrm{Z}_{\mathrm{g}} \end{aligned}$ | IF input impedance <br> IF output impedance |  |  | $\begin{gathered} 3 / 3 \\ 200 / 8 \end{gathered}$ |  | $\mathrm{k} \Omega / \mathrm{pF}$ $\mathrm{k} \Omega / \mathrm{pF}$ |

## TYPICAL APPLICATIONS



APPLICATION EXAMPLE FOR MW


## Prestage control is derived from IF control



TYPICAL APPLICATIONS (Cont'd)

APPLICATION EXAMPLE FOR AM USING VARICAP DIODES BB 113


$$
\begin{array}{lc}
\text { L1 } & 105 \text { turns } 12 \times 0.04 \mathrm{CuLS} \\
\text { L2 } & 7 \text { turns } \quad 0.10 \mathrm{CuL} \\
\text { L3 } & 80 \text { turns } 12 \times 0.04 \mathrm{CuLS} \\
\text { L4 } & 35 \text { turns } 12 \times 0.04 \mathrm{CuLS} \\
\text { L5 } & 15 \text { turns } \quad 0.10 \mathrm{CuL} \\
\text { L8 } & 20 \text { turns } 12 \times 0.04 \mathrm{CuLS} \\
\text { L9 } & 50 \text { turns } 12 \times 0.04 \mathrm{CuLS} \\
\text { L10 } & 22 \text { turns } 12 \times 0.04 \mathrm{CuLS} \\
\text { L11 } & 400 \text { turns } \\
0.06 \mathrm{CuL}
\end{array}
$$

L1-L2 with Vogt coil set D21-23751 L3-L11 with Vogt coil set D41-2519
$V_{D}=8.5 \mathrm{~V} \rightarrow f_{i}=800 \mathrm{kHz}$
$V_{D}=30 \mathrm{~V} \rightarrow \mathrm{f}_{\mathrm{i}}=1620 \mathrm{kHz}$

CONVERSION CONDUCTANCE vs OSCILLATOR VOLTAGE


## RF STAGE CONTROL



The input is not power matched and can be driven with a higher resistance, $\mathrm{V}_{\mathrm{i}}$ is chosen so that a constant $\mathrm{V}_{15}$ is obtained $\left(50 \mathrm{mV} \mathrm{V}_{\mathrm{pp}}\right)$.

TYPICAL APPLICATIONS

## IF CONTROL


$V_{\text {IF }}\left(469 \mathrm{kHz} ; m=80 \% ; f_{\text {mod }}=1 \mathrm{kHz}\right)$ is chosen so that always a constant $V_{\text {AF }}$ is obtained ( $200 \mathrm{~m} \mathrm{~V}_{\text {RMS }}$ )

## TYPICAL PERFORMANCE CHARACTERISTICS

## AF OUTPUT VOLTAGE AND NOISE

 FIGURE vs RF INPUT VOLTAGE (switching position 1)

SIGNAL TO NOISE DISTANCE vs RF INPUT VOLTAGE (switching position 2)


SIGNAL TO NOISE DISTANCE vs RF INPUT VOLTAGE
(parameter is generator impedance) (switching position 1)


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## TEST CIRCUITS



## DESCRIPTION

The $\mu \mathrm{A} 758$ is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The $\mu \mathrm{A} 758$ operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

## FEATURES

- 45dB channel separation
- Automatic stereo/mono switching
- 70dB SCA rejection
- 10 V to 16 V supply range
- High impedance input-low impedance output

PIN CONFIGURATION


## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Supply voltage | +18 | V |
| Supply voltage $\leq 15$ seconds) | +22 | V |
| Voltage at lamp driver terminal |  |  |
| (Lamp OFF) | +22 | V |
| Internal power dissipation | 730 | mW |
| Operating temperature range | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Lead temperature (60sec) | 300 |  |

EQUIVALENT SCHEMATIC


DC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=+12 \mathrm{~V}, 19 \mathrm{kHz}$ pilot level $=30 \mathrm{mV}$ RMs, multiplex signal
( $\mathrm{L}=\mathrm{R}$, pilot OFF) $=300 \mathrm{~m} V_{\text {RMs }}$, modulation frequency $=400 \mathrm{~Hz}$ or 1 Hz , test circuit 1 , unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | $\mu$ A758 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Icc $\mathrm{IL}$ | Supply current <br> Maximum available lamp current |  | Lamp OFF | 75 | $\begin{gathered} 26 \\ 150 \end{gathered}$ | 35 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\mathrm{V}_{7}$ | Voltage at lamp driver terminal | Lamp $=50 \mathrm{~mA}$ |  | 1.3 | 1.8 | V |
| ri ro | Input resistance Output resistance |  | $\begin{aligned} & 20 \\ & 0.9 \end{aligned}$ | $\begin{aligned} & \hline 35 \\ & 1.3 \end{aligned}$ | 2.0 | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |

## AC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | $\mu \mathrm{A} 758$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\Delta\left(\mathrm{V}_{4} \& \mathrm{~V}_{5}\right)$ DC voltage shift at either output terminal | Stereo to mono operation |  | 30 | 150 | mV |
| PS.R.R. Power supply ripple rejection <br> Channel separation <br> SEP  <br> BAL. Channel balance | $200 \mathrm{~Hz}, 200 \mathrm{mV}$ RMS 100 Hz 400 Hz 10 kHz | $\begin{aligned} & 35 \\ & 30 \end{aligned}$ | $\begin{aligned} & 40 \\ & 45 \\ & 45 \\ & 0.3 \\ & \hline \end{aligned}$ | 1.5 | $\begin{aligned} & \hline \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \hline \end{aligned}$ |
| $A_{V} \quad$ Voltage gain | 1 kHz | 0.5 | 0.9 | 1.4 | V/V |
| Pilot input level | Lamp turn-on Lamp turn-off | 2.0 | $\begin{aligned} & 15 \\ & 7.0 \\ & \hline \end{aligned}$ | 22 | $m V_{\text {RMS }}$ mVRMS |
| Pilot input level hysteresis | Lamp turn-off to turn-on | 3.0 | 7.0 |  | dB |
| Capture range <br> T.H.D. Total harmonic distortion | Multiplex level $=600 \mathrm{mV}$ RMs pilot OFF | 2.0 | $\begin{aligned} & 4.0 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \hline 6.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \% \\ & \% \\ & \% \end{aligned}$ |
| 19 kHz rejection 38 kHz rejection SCA rejection ${ }^{1}$ |  | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ | $\begin{aligned} & 35 \\ & 45 \\ & 70 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |
| VCO Tuning resistance ${ }^{2}$ |  | 21.0 | 23.3 | 25.5 | k $\Omega$ |
| VCO Frequency drift | $\begin{gathered} 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C} \\ 25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & +0.1 \\ & -0.4 \end{aligned}$ | $\begin{aligned} & \pm 2 \\ & \pm 2 \end{aligned}$ | $\begin{aligned} & \hline \% \\ & \% \end{aligned}$ |

NOTES

1. Measured with a stereo composite signal consistency of $80 \%$ stereo, $10 \%$ pilot and $10 \%$ SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit, required to set reference frequency at pin 11 to $19 \mathrm{kHz} \pm 10 \mathrm{hz}$.

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


## TEST CIRCUIT AND TYPICAL APPLICATION



## sECTION IA TV CIRCUITS

## DESCRIPTION

Dual doubly balanced chroma demodulator with RGB matrix, PAL switch, and chroma driver stages. A monolithic device designed for use in solid-state color television receivers.

## FEATURES

- Good chroma sensitivity-0.28Vp-p input typical for $5.0 \mathrm{Vp}-\mathrm{p}$ output
- Low differential output dc offiset voltage- 0.6 V maximum
- Differential dc temperature stability$0.7 \mathrm{mV} /{ }^{\circ} \mathrm{C}$
- High blue output voltage swing-10Vp-p typical
- Blanking input provided
- Luminance bandwidth greater than 5.0 MHz


## PIN CONFIGURATION



## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $T_{A}=+25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Power supply voltage | 30 | Vdc |
| Chroma signal input voltage | 5.0 | Vpk |
| Reference signal input voltage | 5.0 | Vpk |
| Minimum load resistance | 3.0 | kohms |
| Luminance input voltage | 12 | $\mathrm{VP}_{\mathrm{P}-\mathrm{P}}$ |
| Blanking input voltage | 7.0 | $\mathrm{VP-P}$ |
| Power dissipation (package limitation) | 625 | mW |
| Plastic packages | 5.0 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Derate above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -20 to +75 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range (ambient) | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range |  |  |

DC ELECTRICAL CHARACTERISTICS $T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=24 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=3.3 \mathrm{k}$ unless otherwise specified. 1,2

| PARAMETER | TEST CONDITIONS | MC1327 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Quiescent output voltage ${ }^{2}$ |  | 13.2 | 14.5 | 15.8 | Vdc |
| Quiescent input current from supply ${ }^{2}$ | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=\infty \\ \mathrm{R}_{\mathrm{L}}=3.3 \mathrm{k} \Omega \end{gathered}$ | 16 | $\begin{aligned} & 7.5 \\ & 19 \end{aligned}$ | 26 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Reference input dc voltage ${ }^{2}$ Chroma reference input dc voltage |  |  | $\begin{aligned} & \hline 6.2 \\ & 3.4 \end{aligned}$ |  | $\begin{aligned} & \mathrm{Vdc} \\ & \mathrm{Vdc} \end{aligned}$ |
| Differential output voltage 1,2 | Temperature coefficient ( $+25^{\circ} \mathrm{C}$ to $+65^{\circ} \mathrm{C}$ ) |  | $\begin{aligned} & 0.3 \\ & 0.7 \end{aligned}$ | 0.6 | $\begin{gathered} \mathrm{Vdc} \\ \mathrm{mV} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Output voltage 1,2 | Temperature coefficient ( $+25^{\circ} \mathrm{C}$ to $+65^{\circ} \mathrm{C}$ ) |  | +0.5 | $\pm 5.0$ | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

## NOTES

[^8]AC ELECTRICAL CHARACTERISTICS $T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=24 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=3.3 \mathrm{~K}$, reference input voltage $=1.0 \mathrm{Vp}-\mathrm{p}$, unless otherwise specified. 1,2,3,4

| PARAMETER | TEST CONDITIONS | MC1327 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Blue output voltage swing 1,4 Chroma input voltage 2,4 | B output $=5.0 \mathrm{Vp}-\mathrm{p}$ | 8.0 | $\begin{gathered} 10 \\ 280 \end{gathered}$ | 550 | $\begin{gathered} \mathrm{Vp-p} \\ \mathrm{mVp}-\mathrm{p} \end{gathered}$ |
| Luminance input resistance |  | 100 |  |  | k $\Omega$ |
| Luminance gain from pin 3 to outputs <br> Differential luminance gain, RGB outputs | @ 5.0 MHz , reference at 100 kHz <br> @ 5.0 MHz |  | $\begin{gathered} \hline 0.95 \\ -1.8 \\ 0.3 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Blanking input resistance | 1.0 Vdc OVdc |  | $\begin{aligned} & 1.1 \\ & 75 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \\ & \hline \end{aligned}$ |
| Detected output voltage (Adjust B output to $5.0 \mathrm{Vp}-\mathrm{p}$, luminance voltage $=23 \mathrm{~V} / 4$ <br> PAL switch operating voltage range | G output R output 7.8 kHz square wave | $\begin{aligned} & \hline 1.4 \\ & 2.5 \\ & 0.3 \\ & \hline \end{aligned}$ | 1.8 2.9 | $\begin{aligned} & 2.2 \\ & 3.3 \\ & 3.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \mathrm{Vp-p} \\ & \mathrm{Vp-p} \\ & \mathrm{Vp-p} \\ & \hline \end{aligned}$ |
| R-Y output dc offset with PAL switch operation |  |  |  | 100 | mVdc |
| Demodulator unbalance voltage | No chroma input voltage and normal reference signal input voltage |  | 200 | 300 | mVp-p |
| Residual carrier and harmonic output voltage | With input signal voltage, normal reference signal voltage and B output $=5.0 \mathrm{Vp}-\mathrm{p}$ |  | 0.6 | 1.0 | Vp-p |
| Reference input resistance Reference input capacitance | Chroma input $=0$ <br> Chroma input $=0$ |  | $\begin{aligned} & 2.0 \\ & 6.0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{K} \Omega \\ & \mathrm{pF} \end{aligned}$ |
| Chroma input resistance Chroma input capacitance |  |  | $\begin{aligned} & \hline 2.0 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \end{aligned}$ |

NOTE

1. With normal reference input signal voltage, adjust chroma input signal voltage to $1.2 \mathrm{Vp}-\mathrm{p}$.
2. With normal reference input signal voltage, adjust chroma input signal voltage until the blue output voltage $=5.0 \mathrm{Vp}-\mathrm{p}$.
3. With normal reference input signal voltage, adjust chroma input signal voltage until the blue output voltage $=5.0 \mathrm{Vp}-\mathrm{p}$. At this point, the red and green voltages will fall within the specified limits.
4. Reference Figure 3.

## TYPICAL APPLICATIONS



Figure 1

## TEST CIRCUITS


$\left(V_{C C}=24 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=3.3\right.$ kilohms, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise specified.)
Figure 2


## DESCRIPTION

An eight stage amplifier with balanced demodulator for amplifying, limiting and the demodulation of FM signals, specially designed for the sound-IF in TV and RF-IF amplifier in radios. An electronic Volume Control for the audio outputsignal is also provided.

## Groups:

TBA 120 S is delivered in groups:
An attenuation of -30 dB of the audio outputsignal requires a resistor from pin 5 to ground as indicated in the table.

| Group | 2 | 3 | 4 | 5 |
| :--- | :---: | :---: | :---: | :---: |
| Value (k $\Omega)$ | 1.9 to 2.2 | 2.1 to 2.5 | 2.4 to 2.9 | 2.8 to 3.3 |

For example, devices marked TBA120S-3 indicate group 3.

## PIN CONFIGURATION



## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | 18 | V |
| Operating temperature range | -15 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation | 400 | mW |
| max 1 minute | 500 | mW |
| Supply current | 15 | mA |
| max 1 minute | 20 | mA |
| Current 13 | 1 | mA |
| 14 | 1 | mA |
| Operating supply voltage | 6 to 18 | V |
| Frequency range | 0 to 12 | MHz |

DC ELECTRICAL CHARACTERISTICS $\quad\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}\right)$

| PARAMETER |  | TEST CONDITIONS | TBA120S |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| ICC | Total current requirement |  | $\begin{aligned} & R_{5}=\infty \\ & R_{5}=0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & 14 \\ & 16 \end{aligned}$ | $\begin{aligned} & 18 \\ & 20 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\begin{aligned} & \mathrm{V}_{8} \\ & \mathrm{~V}_{5} \end{aligned}$ | dc-portion of the output signal Voltage | $\begin{gathered} V_{1}=0 \\ -1 \mathrm{~dB} \text { down } \\ -70 \mathrm{~dB} \text { down } \end{gathered}$ |  | $\begin{aligned} & 7.3 \\ & 2.4 \\ & 1.3 \end{aligned}$ | 2.6 | $\begin{aligned} & V \\ & V \\ & V \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TBA120S |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Gv | IF-voltage gain $\mathrm{V}_{6} / \mathrm{V}_{14}$ |  | $\mathrm{f}=5.5 \mathrm{MHz}$ |  | 68 |  | dB |
| V QPP | IF-output voltage at limiting; each output |  |  | 250 |  | mV |
| VAFrms | AF-output voltage | $\begin{gathered} f=5.5 \mathrm{MHz} ; \Delta f= \pm 50 \mathrm{kHz} ; \\ \mathrm{V}_{\mathrm{I}}=10 \mathrm{mV} ; f_{\bmod }=1 \mathrm{kHz} ; \\ \mathrm{Q}=45 ; \mathrm{k}=4 \% \\ f=5.5 \mathrm{MHz} ; \Delta f= \pm 50 \mathrm{kHz} \\ V_{I}=10 \mathrm{mV} ; f_{\bmod }=1 \mathrm{kHz} \\ \mathrm{Q}=20 ; \mathrm{k}=1 \% \end{gathered}$ |  | $\begin{gathered} 1.1 \\ 0.55 \end{gathered}$ |  | V <br> V |
| $\begin{aligned} & \mathrm{V}_{\mathrm{lim}} \\ & \mathrm{Z}_{\mathrm{I}} \\ & \mathrm{R}_{\mathrm{Q}} \end{aligned}$ | Input voltage starting limiting <br> Input impedance <br> Output resistance | $\begin{gathered} f=5.5 \mathrm{MHz} ; f=50 \mathrm{kHz} \\ \mathrm{f}_{\mathrm{mod}}=1 \mathrm{kHz} ; Q=45 \\ \mathrm{f}=5.5 \mathrm{MHz} \\ \operatorname{Pin} 8 \end{gathered}$ | 15/6 | $\begin{gathered} 30 \\ 40 / 4.5 \\ 2.6 \end{gathered}$ | 60 | $\begin{gathered} \mu V \\ \mathrm{k} \Omega / \mathrm{pf} \\ \mathrm{k} \Omega \end{gathered}$ |
| $V_{\text {AFmax }}$ <br> $V_{\text {AFmin }}$ <br> aAM | Range of volume control <br> AM-suppression | $\begin{gathered} f=5.5 \mathrm{MHz} ; f=+50 \mathrm{~Hz} \\ \mathrm{~V}_{\mathrm{I}}=500 \mu \mathrm{~V} ; \mathrm{f}_{\text {mod }}=1 \mathrm{kHz} ; \\ \mathrm{m}=30 \% \end{gathered}$ | 45 | $70$ $55$ |  | dB <br> $d B$ |
| R5 | Potentiometer resistance | -1dB down <br> -70dB down | 1.0 | $\begin{aligned} & 3.7 \\ & 1.4 \end{aligned}$ | 4.7 | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| CHARACTERISTICS OF THE AUXILIARY CIRCUIT <br> $\mathrm{V}_{12} \quad$ Z-voltage <br> Rz Z-resistance |  | $\mathrm{I}_{12}=5 \mathrm{~mA}$ | 11.2 | $\begin{aligned} & 12 \\ & 30 \end{aligned}$ | 13.2 | $\begin{aligned} & V \\ & \Omega \end{aligned}$ |
| $\begin{aligned} & \text { VCEO T43 } \\ & \text { hFE } \end{aligned}$ | Breakdown voltage Current gain | $\begin{gathered} I_{4}=0 ; I_{3}=500 \mu A \\ I_{3}=1 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & 13 \\ & 30 \end{aligned}$ | 120 |  | V |

## TYPICAL PERFORMANCE CHARACTERISTICS



VOLUME CONTROL
SIGNETICS TBA120S


## TEST CIRCUIT



## FEATURES

TBA120T

- Input and demondulator are designed for use with ceramic resonators
- Additional output before volume control (constant audio signal) for the connection of headphones and video recorders
- Additional audio input for connection of video recorders (playback)
- Constant audio output voltage between 10 to 18 V supply voltage of the same level as TBA120S operating at 15 V supply voltage
- Insensitive against hum from the supply voltage therefore very little need for
smoothing capacitors
- As there is very little residual IF voltage on the audio output, there is no interference of the video-IF due to harmonics of the sound-IF
- No selection for volume control characteristics is necessary

TBA120U

- This circuit incorporates all the advantages of TBA120T but input and demodulator are designed for use in connection with standard LC-circuits

PIN CONFIGURATION


## BLOCK DIAGRAM



NOTES

1. Only TBA120T
2. Only TBA120U

## ABSOLUTE MAXIMUM RATINGS

|  | PARAMETER | RATING | UNIT |
| :--- | :--- | :---: | :---: |
| $V_{C C}$ | Supply voltage | 18 | V |
| $\mathrm{~T}_{\text {A }}$ | Ambient temperature in operation | -15 to +70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{S}$ | Storage temperature | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{P}_{\text {TOT }}$ | Total power dissipation | 400 | mW |
| $\mathrm{~V}_{\mathrm{S}}$ | Voltage | 6 | V |
| $\mathrm{I}_{4}$ | Current | 5 | mA |
| $\mathrm{R}_{13-14}$ | Ohmic resistance (TBA120U) | $\leq 1$ | $\mathrm{k} \Omega$ |
| $R_{\text {THSA }}$ | Thermal resistance (system-air) | $\leq 120$ | $\mathrm{~K} / \mathrm{W}$ |
| V $_{\text {CC }}$ | Range of operation | 10 to 18 | V |
| f | Frequency range | 0 to 12 | MHz |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TBA120T/120U |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Icc | Total current consumption |  |  | 9.5 | 13.5 | 17.5 | mA |
| $\mathrm{V}_{8}$ | DC level of output signal | $\mathrm{V}_{\mathrm{i}}=0$ |  | 4 |  | V |
| $\mathrm{V}_{12}$ |  | $\mathrm{V}_{\mathrm{i}}=0$ |  | 4.9 |  | V |
| $\mathrm{V}_{4}$ | Stabilized voltage |  | 4.2 | 4.8 | 5.3 | V |

AC ELECTRICAL CHARACTERISTICS $\quad T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=12 \mathrm{~V}$ unless otherwise specified.*

|  | PARAMETER | TEST CONDITIONS | TBA120/120U |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| $\begin{aligned} & \mathrm{G}_{\mathrm{v}} \\ & \mathrm{~V}_{\mathrm{qpp}} \end{aligned}$ | IF voltage gain Output voltage with limiting at each output | $\mathrm{V}_{6} / \mathrm{V}_{14}(\mathrm{ffiF}=5.5 \mathrm{MHz})$ |  | $\begin{gathered} 68 \\ 250 \end{gathered}$ |  | $\begin{gathered} \mathrm{dB} \\ \mathrm{mV} \end{gathered}$ |
| $\begin{aligned} & \hline \mathrm{R}_{\mathrm{q} 8} \\ & \mathrm{Rq}_{12} \\ & \mathrm{R}_{13} \\ & \hline \end{aligned}$ | Output impedance Input impedance | $\begin{gathered} \text { Pin } 8 \\ \text { Pin } 12 \end{gathered}$ |  | $\begin{gathered} \hline 1.1 \\ 1.1 \\ 2 \\ \hline \end{gathered}$ |  | $\begin{aligned} & \hline \mathrm{k} \Omega \\ & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \\ & \hline \end{aligned}$ |
| $\mathrm{R}_{14}$ | Internal impedance |  |  | 12 |  | $\Omega$ |
| $\begin{aligned} & \hline V_{8} \\ & V_{12} \end{aligned}$ | Residual IF voltage without deemphasis |  |  | $\begin{aligned} & 20 \\ & 30 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| $\mathrm{V}_{8} / \mathrm{V}_{3}$ | AF gain | AF not regulated |  | 7.5 |  |  |
| $\mathrm{V}_{\mathrm{AF} / 8}$ | Regulation at certain ratio of divider | $\mathrm{R}_{4-5}=5 \mathrm{k} \Omega, \mathrm{R}_{5-1}=13 \mathrm{k} \Omega$ | 20 | 28 | 36 | dB |
| $\frac{V_{\text {AFMAX }}}{V_{\text {AFMIN }}}$ | Range of volume control | Referred to pin 8 | 70 | 85 |  | dB |
| $\begin{aligned} & \mathrm{R}_{4-5^{*}} \\ & \mathrm{~V}_{\text {ilim }} \end{aligned}$ | Resistance Input voltage for limitation | $\begin{gathered} \mathrm{f}_{\mathrm{IF}}=5.5 \mathrm{MHz}, \mathrm{f}= \pm 50 \mathrm{kHz}, \\ \mathrm{f}_{\mathrm{MOD}}=1 \mathrm{kHz} \end{gathered}$ | 1 | 30 | $\begin{aligned} & \hline 10 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{k} \Omega \\ & \mu \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{8} / \mathrm{V}_{11}$ | Hum suppression | 。 |  | 35 |  | dB |
| $\mathrm{V}_{12} / \mathrm{V}_{11}$ |  |  |  | 30 |  | dB |

*NOTE
If dc volume control is not used, pin 4 has to be connected directly to pin 5.

AC ELECTRICAL CHARACTERISTICS TBA120T $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TBA120T ONLY |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $Z_{\text {IN }}$ | Input impedance |  | $\mathrm{f}_{\mathrm{IF}}=5.5 \mathrm{MHz}$ |  | 800/5 |  | $\Omega / \mathrm{pF}$ |
| afm | AM suppression | $\begin{gathered} \mathrm{f}_{\mathrm{IF}}=5.5 \mathrm{MHz}, \mathrm{f}= \pm 50 \mathrm{kHz} \\ \mathrm{~V}_{\mathrm{I}}=500 \mu \mathrm{~V}, \mathrm{f}_{\mathrm{MOD}}=1 \mathrm{kHz} \\ \mathrm{~m}=30 \% \end{gathered}$ | 50 | 60 |  | dB |
| $\begin{aligned} & V_{8} \\ & V_{12} \end{aligned}$ | AF output voltage | $\begin{gathered} \mathrm{f}_{\mathrm{IF}}=5.5 \mathrm{MHz}, \mathrm{f}=+50 \mathrm{kHz} \\ \mathrm{f}_{\mathrm{MOD}}=1 \mathrm{kHz} \end{gathered}$ | 650 400 | $\begin{aligned} & 900 \\ & 650 \end{aligned}$ |  | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |

*NOTE
If dc volume control is not used, pin 4 has to be connected directly to pin 5 .

AC ELECTRICAL CHARACTERISTICS TBA120V $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{VCC}=12 \mathrm{~V}$ unless otherwise specified.

|  | PARAMETER | TEST CONDITIONS | TBA120U ONLY |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| $Z_{1}$ | Input impedance | $\mathrm{f}_{\mathrm{IF}}=5.5 \mathrm{MHz}$ | 15/6 | 40/4.5 |  | $\mathrm{k} \Omega / \mathrm{pF}$ |
| aAM | AM suppression | $\begin{gathered} \mathrm{f}_{\mathrm{IF}}=5.5 \mathrm{MHz}, \mathrm{f}= \pm 50 \mathrm{kHz} \\ \mathrm{~V}_{\mathrm{i}}=500 \mu \mathrm{~V}, \mathrm{f}_{\mathrm{MOD}}=1 \mathrm{kHz} \\ \mathrm{~m}=30 \% \end{gathered}$ | 50 | 60 |  | dB |
| $V_{8 \text { eff }}$ $V_{12 e f f}$ | AF output voltage | $\begin{gathered} f_{\mathrm{IF}}=5.5 \mathrm{MHz}, \mathrm{f}= \pm 50 \mathrm{kHz}, \\ \mathrm{~V}_{\mathrm{i}}=500 \mu \mathrm{~V}, \mathrm{f}_{\mathrm{MOD}}=1 \mathrm{kHz}, \\ \mathrm{Q}_{8} \approx 45, \mathrm{k}=4 \% \end{gathered}$ | $850$ | $1200$ $1000$ |  | $\mathrm{mV}$ |
| k | Harmonic distortion | $\begin{gathered} f_{\mathrm{lF}}=5.5 \mathrm{MHz}, f=+50 \mathrm{kHz} \\ V_{i}=10 \mathrm{mV}, f_{M O D}=1 \mathrm{kHz} \\ Q_{8} \approx 20 \end{gathered}$ |  | 1 |  | \% |

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)

## HARMONIC DISTORTION

vs VOLUME CONTROL

AF OUTPUT VOLTAGE (PIN 8) vs POTENTIOMETER RESISTANCE AND vs RATIO OF RESISTANCES

AF OUTPUT VOLTAGE (PIN 8) vs VOLTAGE FEEDING INTO PIN 5



With electrolytic capacitor $47 \mu \mathrm{~F}$ from pin 11 to ground.

$V_{\text {IRF }}=60 \mathrm{mV} \mathrm{V}_{\text {EFF }}, \mathrm{f}_{\text {IF }}=5.5 \mathrm{MHz}, .1 \mathrm{f}= \pm 50 \mathrm{kHz}$, $\mathrm{f}_{\mathrm{MOD}}=1 \mathrm{kHz}, \mathrm{V}_{\mathrm{CC}}=18 \mathrm{~V}$

## TEST CIRCUITS

CIRCUIT FOR DIRECT CONNECTION TO VIDEO RECORDERS VIDEO RECORDER


SOCKET (1): Switching voltage: at playback +12 V
at input free

SOCKET (4): Simultaneous in and output for AF
FUNCTION:
When switching voltage applied the emitter follower, BC238, on the output is blocked and the buffer stage, BC308, is switched on. It includes a pre-emphasis to balance the de-emphasis at the AF output. The IF amplifier is put out of the operation by the diode, BA127, and the 47kohm resistor. The remote controllable volume regulator in the TBA120 T/U is used for recording and playback.

## TEST CIRCUITS (Con't)



## DESCRIPTION

Chrominance combination circuit for use in PAL television receivers.

## FEATURES

- Internal supply line stabilization
- 20dB ACC range-14dB + 6dB
- Low external component count
- Designed to be used in conjunction with TBA396 and TBA327/MC1327


## PIN CONFIGURATION



## SYSTEM BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Power supply current | 60 | mA |
| dc current capability of | 4.0 | mA |
| reference output | 1.2 | $\mathrm{VD}-\mathrm{p}$ |
| Chrominance input voltage | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | 625 | mW |
| Power dissipation (package |  |  |
| limitation) | 5.0 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Derate above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range |  |  |

EQUIVALENT SCHEMATIC


DC ELECTRICAL CHARACTERISTICS $T_{A}=+25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | TBA395 |  | UNIT |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ |  |  |
| Supply voltage |  | 7.5 | 8.4 | 9.5 | Vdc |
| Burst gate operating voltage |  | 2.0 |  | V |  |
| Chrominance output dc current | Color killer operating <br> Color killer off | 200 |  | 4.0 | $\mu \mathrm{~A}$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=+25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LIMITS |  | UNIT |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ |  |  |
| Forward transconductance | Chrominance output <br> load $=560 \Omega$ |  |  |  |  |
| fiN $=4.43 \mathrm{MHz}$ | 6.4 |  |  | mmho |  |
| Chrominance input resistance |  | 2.4 | 3.1 | 4.3 | $\mathrm{k} \Omega$ |
| Reference oscillator pull-in range |  | 4250 |  | Hz |  |
| Reference output |  | 1.3 | 700 |  | mV |
| H/2 bistable output |  | 1.6 | 2.2 | $\mathrm{Vp}-\mathrm{p}$ |  |

## TYPICAL CIRCUIT CONFIGURATION



## SETTING-UP NOTES

For subcarrier oscillator adjustment the chrominance input must be bypassed to ground via a 1 nf capacitor. The ACC potentiometer is then set to 1.2 volts below pin 2 voltage using a high input impedance oscilloscope or Voltmeter ( $>10 \mathrm{~m} \Omega$ ). While the adjustment is made burst gate pulses must be applied to pin 5.
The oscillator free-running frequency can then be adjusted to sub-carrier value $\pm 10 \mathrm{~Hz}$.

The loop will lock if a chrominance signal is re-connected.
With a peak to peak signal of 250 mV (100\% bars) the output on pin 1 should be adjusted to 400 mV peak to peak using the ACC control potentiometer.

## APPLICATION NOTES

1. Normal decoupling precautions must be taken. For example pin 2 ( 8.4 volt circuit supply point) must be decoupled closely to
pin 6 (ground) thus preventing sub-carrier components leaking into sensitive areas of the circuit.
2. To prevent the radiation of sub-carrier harmonics, the connection from pin 9 (reference output) and pin 8 (crystal feedback) must be kept as short as possible.
3. The connection from pin 1 (chroma output) should be also as short as possible to prevent capacitive loading of the $1.8 \mathrm{k} \Omega$ output resistor.

## DESCRIPTION

Luminance and chrominance combination circuit designed for use in PAL television receivers.

## FEATURES

- DC control of brightness, contrast and saturation
- Tracking of saturation with contrast control changes
- Beam current limiting
- Black level clamping
- Designed to be used in conjunction with TBA395 and TBA327/MC1327

PIN CONFIGURATION


SYSTEM BLOCK DIAGRAM


ABSOLUTE MAXIMUM RATINGS $T_{A}=+25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | 20 | V |
| Luminance output collector voltage | 30 | V |
| Luminance output emitter current | 7.0 | mA |
| Chrominance output emitter current | 5.0 | mA |
| Operating temperature range | 0 to +70 | mW |
| Power dissipation (package | 625 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| limitation) | 5.0 | ${ }^{\circ} \mathrm{C}$ |
| Derate above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -65 to +150 |  |
| Storage temperature range |  |  |

## EQUIVALENT SCHEMATIC



GENERAL ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | TBA396 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Luminance input resistance |  | 100 |  |  | k $\Omega$ |
| Luminance gain |  | 0.6 | 1.0 | 1.2 |  |
| Change of black level with contrast and signal changes Black level clamp gating pulse | Black to white $4 \mu$ s gating | 50 |  | $\begin{gathered} 3.0 \\ 1000 \\ \hline \end{gathered}$ | $\begin{gathered} \% \\ \mu \mathrm{~A} \\ \hline \end{gathered}$ |
| Contrast control range Saturation control range |  | $\begin{aligned} & 35 \\ & 35 \end{aligned}$ |  |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| 3dB luminance bandwidth | Resistive load |  | 7.5 |  | MHz |
| Video input aperture |  | 1.4 |  | 3.4 | $\mathrm{V}_{\mathrm{p}-\mathrm{p}}$ |
| Chrominance input resistance Chrominance voltage gain | Resistive load | $\begin{aligned} & 5.0 \\ & 2.5 \end{aligned}$ | 3.0 | 5.0 | k $\Omega$ |
| Chrominance phase shift with saturation control <br> Chrominance phase shift with contrast control |  |  |  | $\pm 3$ $\pm 3$ | \% |
| Chrominance/Luminance tracking error with contrast control Threshold of beam limiter |  | 1.8 | 2.0 | $\pm 2$ 2.2 | dB V |

## TYPICAL CIRCUIT CONFIGURATION



## APPLICATION NOTES

- The dc controls are relatively insensitive to interference if the decoupling associated with these lines is close to the IC.
- Good decoupling is required close to the "cold" end of the PAL delay line driving coil to prevent spurious subcarrier components reaching the IC supply line.


## SETTING UP PROCEDURE

The pre-set brilliance control must be adjusted to give the correct black level of +16.5 V at pin 7 . If the color demodulator IC TBA327/MC1327 is used to complete the system a voltage of +7.5 V at the chroma outputs can be set using the same procedure.

This operation must be performed with the brilliance control at the center of its range.

## DESCRIPTION

The circuit is a TV-video amplifierdemodulator and consists of:

Three symmetrical IF-broadbandamplifiers with AGC on the first and second stage,
A video balanced-carrier demodulator, A video pre-amplifier with lowpasscharacteristic,
Gated AGC-section for IF-amplifier and a Delayed tuner-AGC-current TBA1440 is for PNP-type tuner The AGC-current is high enough to drive pin-diodes

## FEATURES

- High gain-high stability-low noise
- Constant input impedance
- Output independent of supply-voltage over the operating range
- Minimum IF at video-outputs
- Fast AGC
- Low intermodulation products
- Low impedance outputs for positive and negative going video
- DC-levels temperature compensated
- Adjustable black and white level, each independent from the other
- High tuner-AGC current
- Adjustable tuner-AGC threshold

PIN CONFIGURATION


## BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Power supply voltage | 10.5 to 16 | V |
| Voltage at pin 4 | 5 | V |
| Voltage at pin 5 | 16 | V |
| Voltage at pin 14 | 5 | V |
| Ohmic resistance between | 0 to 20 | $\Omega$ |
| pin 8 and pin 9 |  |  |
| Power dissipation | 1100 | mW |
| $25^{\circ} \mathrm{C}$ | 700 | mW |
| $70^{\circ} \mathrm{C}$ | 110 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal resistance junction to ambient | -25 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range |  |  |

## DC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | TBA1440 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Vcc |  | 10.5 | 15 | 16.5 | V |
| Icc | $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$ |  | 40 | 45 | mA |
| $\mathrm{V}_{110}$ | $\mathrm{V}_{11}-\mathrm{DC} / \mathrm{R}_{14}=0$ | 7.9 | 8.2 | 8.5 | V |
| $\mathrm{V}_{11}$ | $\mathrm{V}_{11}-\mathrm{DC} / \mathrm{R}_{14}=\infty$ | 5.4 | 5.8 | 6.2 | V |
| $\mathrm{V}_{120}$ | $V_{12}-\mathrm{DC} / \mathrm{R}_{14}=0$ | 2.4 | 2.8 | 3.0 | v |
| $\mathrm{V}_{12}$ | $\mathrm{V}_{12}-\mathrm{DC} / \mathrm{R}_{14}=\infty$ | 1.25 | 1.6 | 1.8 | v |
| THRESHOLD FOR SYNC. LEVEL $-\mathrm{V}_{10}$ | $\mathrm{R}_{10-11}=0$ | 0.7 | 1.0 | 1.3 | V |
| $-\mathrm{V}_{7}$ | Negative gating pulse | 0.25 | 1 | 7 | v |
| GAIN CONTROL VOLTAGE |  |  |  |  |  |
| $V_{4 \text { max }}$ | Gain max |  | 0.5 |  | v |
| $V_{4 \text { min }}$ | Gain min |  | 1.6 | 2 | V |

AC ELECTRICAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | TBA1440 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| MINIMUM INPUT VOLTAGE$\mathrm{V}_{1 / 16}$$\mathrm{~V}_{11}$ |  |  |  |  |  |
|  | $\mathrm{V}_{11}=3 \mathrm{Vpp}$ |  | 500 | 750 | $\mu \mathrm{V}$ |
|  | Videoband width ( -3 dB ) | 5.5 | 6 | 7 | MHz |
| ACC range |  | 50 | 55 |  | dB |
| Maximum IF voltage level present at video outputs |  |  | 60 | 70 | mV |
| Input impedance | Gain max |  | 1.8 |  | $k \Omega$ |
|  |  |  | 2.0 |  | pF |
|  | Gain min |  | 1.9 |  | $\mathrm{k} \Omega$ |
|  |  |  | 1.9 |  | $\mathrm{pF} \Omega$ |

TYPICAL PERFORMANCE CHARACTERISTICS


TEST CIRCUIT


## DESCRIPTION

The TBA1440G (for pnp tuner pre-stages) and TBA1441 (for npn tuner pre-stages) have been developed from the TBA440P/N. Their improvements are as follows:

- Reduced residual IF at outputs 11 and 12
- Reduced residual IF at pin 13
- Considerably improved intermodulation distance
- Excellent tuning attitude even with lowohmic tank circuit at demodulator

The IC's contain a high-amplifying controllable video IF amplifier, a controlled demodulator and two low-resistance video outputs
with positive- and negative-going signals as well as the complete keyed control and delayed tuner control.

- Large control range with low noise and wide dynamic range
- High sensitivity
- Controlled demodulator, so minimum 1.07 MHz disturbances
- Internal temperature stabilization
- The white levels of the video signals at the positive and negative video output are independent of the operating voltage
- The white and black levels can be adjusted separately


## ABSOLUTE MAXIMUM RATINGS



| PARAMETER | RATING | UNIT |  |
| :--- | :--- | :---: | :---: |
| $\mathrm{V}_{13}$ | Supply voltage | $15^{*}$ | V |
| $\mathrm{~V}_{4}$ | Voltages | 5 | V |
| $\mathrm{~V}_{5}$ |  | 20 | V |
| $\mathrm{~V}_{14}$ |  | 5 | V |
| $\mathrm{R}_{8-9}$ | Ohmic resistance between pins 8 and 9 | $\leq 20$ | $\Omega$ |
| $\mathrm{R}_{\text {THSA }}$ | Thermal resistance (system-air) | 100 | $\mathrm{~K} / \mathrm{W}$ |
| $\mathrm{T}_{\mathrm{J}}$ | Junction temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathbf{S}}$ | Storage temperature | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{13}$ | Supply voltage range | 10.5 to 15 | V |
| $\mathrm{~T}_{\mathbf{A}}$ | Ambient temperature in operation | -25 to +60 | ${ }^{\circ} \mathrm{C}$ |

*NOTE
Briefly 16.5 V

DC ELECTRICAL CHARACTERISTICS $\quad \mathrm{V}_{13}=13 \mathrm{~V}, \mathrm{f}_{\| \mathrm{F}}=38.9 \mathrm{MHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$; all data with reference to ground, unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TBA1440G/1441 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| 113 | Current consumption |  | $\mathrm{V}_{13}=15 \mathrm{~V}$ | 34 | 47 | 60 | mA |
| $\mathrm{V}_{11}$ | DC voltage at output 11 | $\begin{gathered} \hline \mathrm{V}_{13}=15 \mathrm{~V} ; \mathrm{V}_{1}=0 \\ R_{14-3}=\infty \\ R_{14-3}=0 \end{gathered}$ |  | $\begin{aligned} & 5.5 \\ & 9.6 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{12}$ | DC voltage at output 12 | $\begin{gathered} \hline \mathrm{V}_{13}=15 \mathrm{~V} ; \mathrm{V}_{1}=0 \\ \mathrm{R}_{14-3}=\infty \\ \mathrm{R}_{14-3}=0 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 1.9 \\ & 3.5 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & V_{10}=V_{11} \\ & V_{11 \text { sync }} \end{aligned}$ | AGC threshold <br> Sync pulse level with async or without gating pulses | $\mathrm{V}_{10}=$ sync pulse level for $R_{10-11}=0$ <br> Peak level control |  | $\begin{aligned} & 1.9 \\ & .5 \end{aligned}$ |  | $\mathrm{V}$ $\mathrm{V}$ |
| $\mathrm{V}_{4}$ | IF control voltage | For max. gain For min. gain | $\begin{gathered} 0 \\ 2.5 \end{gathered}$ |  | $\begin{gathered} .5 \\ 5 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $-V_{7}$ | Gating pulse voltage |  | 2 |  | 5 | V |
| $I_{11} ; I_{12}$ | Output current | To ground $\mathrm{TO}+\mathrm{V}_{13}$ |  |  | $\begin{gathered} 5 \\ -1 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

## NOTES

1. According to test circuit; $\mathrm{V}_{1}=$ effective sync pulse level at $60 \Omega$.
2. Test level $\mathrm{a}_{\mathrm{cc}}=-3 \mathrm{~dB}$

$$
\mathrm{a}_{\mathrm{sc}}=-20 \mathrm{~dB} \text { referring to picture carrier. }
$$



AC ELECTRICAL CHARACTERISTICS $\quad\left(V_{13}=13 \mathrm{~V} ; f_{\| F}=38.9 \mathrm{MHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$; all data with reference to ground, unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TBA1440G/1441 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\begin{aligned} & \Delta \mathrm{V}_{11} / \Delta \mathrm{V}_{13} \\ & \Delta \mathrm{~V}_{12} / \Delta \mathrm{V}_{13} \end{aligned}$ | White level deviation |  |  |  | $\begin{aligned} & 100 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & \mathrm{mV} / \mathrm{V} \\ & \mathrm{mV} / \mathrm{V} \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{R}_{14-3} \\ & \mathrm{R}_{10-11} \end{aligned}$ | Resistance for $\Delta \mathrm{V}_{11}=1 \mathrm{~V}$ Resistance for sync pulse level deviation of 1 V |  |  | $\begin{aligned} & 8.5 \\ & 2.4 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| 15 | Control current for tuner prestage | $V_{5}>2 V$ <br> TBA1440G: 10 dB after AGC TBA1441: 10dB previous to AGC | 10 | 15 |  | mA |
| $\mathrm{V}_{11} ; \mathrm{V}_{12}$ | Residual IF (basic frequency) |  |  | 10 |  | mV |
| $\mathrm{Z}_{1-16}$ | Input impedance | At max. gain At min. gain |  | $\begin{aligned} & \hline 1.8 / 2 \\ & 1.9 / 0 \end{aligned}$ |  | k $\Omega / \mathrm{pF}$ $\mathrm{k} \Omega / \mathrm{pF}$ |
| $\overline{V_{1}}$ | Input voltage ${ }^{1}$ Video band width | $\begin{gathered} \hline \mathrm{V}_{11}=3 \mathrm{~V}_{\mathrm{PP}} \\ -3 \mathrm{~dB} \\ \hline \end{gathered}$ | $\begin{gathered} 70 \\ 6 \\ \hline \end{gathered}$ | $\begin{gathered} 100 \\ 7 \\ \hline \end{gathered}$ | 300 | $\begin{gathered} \mu \mathrm{V} \\ \mathrm{MHz} \\ \hline \end{gathered}$ |
| $\begin{aligned} & \Delta G_{v} \\ & \mathrm{a} \\ & \mathrm{Z}_{\mathrm{q} 8-9} \end{aligned}$ | AGC range <br> Intermodulation with reference <br> color carrier ${ }^{2}$ <br> Output impedance |  |  | $\begin{gathered} 55 \\ 45 \\ 2 / 2.5 \end{gathered}$ |  | dB <br> dB <br> $\mathrm{k} \Omega / \mathrm{pF}$ |

NOTES

1. According to test circuit; $\mathrm{V}_{1}=$ effective sync pulse level at $60 \Omega$.
2. Test level $a_{c c}=-3 d B$

$$
\mathrm{a}_{\mathrm{sc}}=-20 \mathrm{~dB} \text { referring to picture carrier. }
$$

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS


TEST CIRCUIT


## FEATURES

- Performs all video IF functions
- Provides 63dB IF AGC range
- Tuner AGC output
- Black and white noise inverting circuits
- AFC output
- High input sensitivity $-100 \mu \mathrm{~V}$ typical
- $53 \mathrm{~dB} \mathrm{~S} / \mathrm{N}$ ratio at 40dB gain control
- Minimal external components and adjustments required
- Switch disabling of video to allow direct video interface with VTR

PIN CONFIGURATION


## SIMPLIFIED BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage $\mathrm{V}_{\mathrm{CC}}$ | 14 | V |
| Supply current $(\mathrm{V} \mathrm{CC}=14 \mathrm{~V})$ | 75 | mA |
| Power dissipation $(\mathrm{V} \mathrm{CC}=14 \mathrm{~V})$ | 1.0 | W |
| Operating temperature | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | TDA 2541 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Icc | Supply current |  |  | 37 |  | 67 | mA |
| $\begin{aligned} & V_{\operatorname{tn}(\mathrm{AFC})} \\ & \mathrm{I}_{5} \end{aligned}$ | AFC switched off below AFC symmetry | $\mathrm{V}_{\mathrm{i}}=0, \mathrm{~V}_{14}=0$ | -40 | 2.5 | +40 | $\begin{aligned} & \mathrm{V} \\ & \mu \mathrm{~A} \end{aligned}$ |
| $V_{\text {th }}$ (VTR) | VTR switch switches off below |  |  | 1.1 |  | V |
| Vws $V_{D(W S)}$ | White spot inverter threshold level White spot inversion clamping level |  |  | $\begin{aligned} & 6.6 \\ & 4.6 \end{aligned}$ |  | $\begin{aligned} & \text { v } \\ & \text { v } \end{aligned}$ |
| $\begin{aligned} & \hline \mathrm{V}_{\mathrm{N}} \\ & \mathrm{~V}_{0(\mathrm{~N})} \end{aligned}$ | Noise inverter threshold level Noise inversion clamping level |  |  | $\begin{aligned} & 1.8 \\ & 3.8 \end{aligned}$ |  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{v} \end{aligned}$ |
| $\begin{aligned} & \mathrm{I}_{4} \\ & \mathrm{~V}_{4(\mathrm{SAT})} \\ & \mathrm{I}_{4} \end{aligned}$ | Tuner AGC output ON current Tuner AGC output voltage Tuner AGC output OFF current | $\mathrm{I}_{4}=10 \mathrm{~mA}$ | 10 |  | $\begin{gathered} 300 \\ 10 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{mV} \\ & \mu \mathrm{~A} \end{aligned}$ |

AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | TDA 2541 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| IF input voltage for onset $\mathrm{V}_{\mathrm{i}} \quad$ of $\mathrm{AGC}(f=45.75 \mathrm{MHz})$ |  | 70 | 100 | 140 | $\mu \mathrm{V}$ |
| $\mathrm{V}_{\mathrm{O}(\mathrm{Z})}$ Zero signal output level <br> $\mathrm{V}_{\mathrm{O}(\mathrm{TS})}$ Top sync level |  | $\begin{aligned} & \hline 5.7 \\ & 2.9 \end{aligned}$ | $\begin{aligned} & 6 \\ & 3 \end{aligned}$ | $\begin{aligned} & 6.3 \\ & 3.2 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{5}$ AFC output voltage swing <br> $\Delta V_{i}$ IF gain control range <br> $\mathrm{S} / \mathrm{N}$ $\mathrm{S} / \mathrm{N}$ at $\mathrm{V}_{\mathrm{i}}=10 \mathrm{mV} 1$ <br> B 3dB bandwidth of video amplifier |  | 50 | $\begin{gathered} 10 \\ 63 \\ 58 \\ 6 \end{gathered}$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~dB} \\ \mathrm{~dB} \\ \mathrm{MHz} \end{gathered}$ |
| dG Differential gain2 <br> d0 Differential phase ${ }^{2}$ |  |  | $\begin{gathered} 4 \\ 3^{\circ} \end{gathered}$ | $\begin{aligned} & 10 \\ & 10^{\circ} \end{aligned}$ | \% |
| Intermodulation (1.1MHz)3 <br> Intermodulation (3.3MHz)4 | 1.1 MHz blue 1.1 MHz yellow 3.3 MHz | $\begin{aligned} & 46 \\ & 46 \\ & 46 \end{aligned}$ | $\begin{aligned} & 60 \\ & 50 \\ & 54 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Carrier signal at video output 2nd harmonic of carrier at video output |  |  | $\begin{gathered} 4 \\ 20 \end{gathered}$ | 30 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Change of frequency for 10V AFC swing |  |  | 100 | 200 | kHz |

## NOTES

1. $S / N=\frac{V_{0} \text { black to white }}{V \text { noise r.m.s. } B=5 \mathrm{MHz}}$
2. Measured with the VZM-2 test set-up of Wandel \& Goltermann or equivalent. Measured between 10 and $75 \%$ of topsync level.
3. Intermodulation $1.1 \mathrm{MHz}=20 \log \left(\frac{V_{0} B-W}{V_{0} p-p 1.1 M H z}\right) d B=20 \log \left(\frac{V_{0} 4.4 \mathrm{MHz}}{V_{0} 1.1 \mathrm{MHz}}\right.$
4. Intermodulation $3.3 \mathrm{MHz}=20 \log \left(\frac{V_{0} 4.4 \mathrm{MHz}}{V_{0} 3.3 \mathrm{MHz}}\right) d \mathrm{~dB}$

## TYPICAL APPLICATION



## DESCRIPTION

The ULN2211 contains a limiting amplifier, an FM quadrature detector, an electronic gain control stage and a 2-watt audio output stage. It can be used to detect and amplify any FM modulated signal having a $0.1-20 \mathrm{MHz}$ carrier frequency.
It is especially recommended as a complete TV sound channel requiring few external components and only one tuning adjustment for the 4.5 MHz tank circuit. Provision is made for 6 dB /octave de-emphasis and tone control.

## FEATURES

- 2-watt output
- DC volume control attenuation, 70 dB typ
- Limiter gain of 70 dB
- Limiting threshold typically less than $200 \mu \mathrm{~V}$
- Automatic thermal shutdown
- Over-current limiting
- 20dB ripple rejection
- Single supply operation (18-30V)
- No crossover distortion


## PIN CONFIGURATION



NOTE: Internal power dissipation in watts.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage, VCC | +30 | V |
| Input voltage (pin 10) | +4.0 | Vrms |
| Power consumption (internal) | See Figure 1 |  |
| Operating temperature |  |  |
| Storage temperature | -65 to +70 | ${ }^{\circ} \mathrm{C}$ |

## AC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+24 \mathrm{~V} ; \mathrm{f}_{\mathrm{o}}=4.5 \mathrm{MHz}, \Delta \mathrm{f}=25 \mathrm{kHz}, \mathrm{f}_{\mathrm{m}}=400 \mathrm{~Hz}$

 unless otherwise specified.| PARAMETER |  | TEST CONDITIONS | ULN2211 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $V_{\text {TH }}$ | Recovered audio limiting threshold1 |  | $\begin{gathered} \text { Adjust } \mathrm{V}_{1} \text { for } \mathrm{V}_{0}=5.6 \mathrm{~V}\left(\mathrm{PO}_{\mathrm{O}}=2 \mathrm{~W}\right) \\ \text { Adjust } \mathrm{V}_{1} \text { for } 2 \mathrm{~W}, \mathrm{~V}_{\mathrm{IN}}=10 \mathrm{mV} \\ \mathrm{~V}_{\text {IN }}=10 \mathrm{mV}, \mathrm{f}=25 \mathrm{kHz} \\ \hline \end{gathered}$ | $\begin{gathered} 30 \\ 500 \end{gathered}$ | 150 | 350 | $\begin{gathered} \mu \mathrm{V} \\ \mathrm{~dB} \\ \mathrm{mVrms} \end{gathered}$ |
| AMR Vo | AM rejection ${ }^{2}$ <br> Recovered AF voltage (pin 16) | $\begin{gathered} 55 \\ 800 \end{gathered}$ |  |  |  |  |
| $\begin{aligned} & \text { THDD } \\ & \text { THDO } \end{aligned}$ | Detector output distortion Output distortion | $\begin{gathered} \mathrm{V}_{\mathrm{IN}}=10 \mathrm{mV}, \mathrm{f}=25 \mathrm{kHz} \\ \mathrm{PO}_{\mathrm{O}}=2 \mathrm{~W}, \mathrm{R}_{\mathrm{L}}=16 \end{gathered}$ |  | $\begin{gathered} 1.0 \\ 2 \end{gathered}$ | $\begin{aligned} & 2.0 \\ & 10 \end{aligned}$ | $\begin{aligned} & \hline \% \\ & \% \end{aligned}$ |  |
|  | Playthrough | $\mathrm{V}_{1}=0$ |  | 10 | 15 | mVrms |  |
| $\begin{aligned} & \hline \operatorname{lmax} \\ & \mathrm{V}_{\mathrm{N}} \\ & \hline \end{aligned}$ | Current limit Noise | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=0 \\ \mathrm{~V}_{\mathrm{IN}}=0, \mathrm{~V}_{1}=+15 \mathrm{~V} \\ \hline \end{gathered}$ |  | $\begin{gathered} \hline 800 \\ 15 \\ \hline \end{gathered}$ | 20 | mA mVrms |  |
| Av $\mathrm{V}_{\mathrm{O}} / \mathrm{V}_{\mathrm{CC}}$ | Power AMP voltage gain ${ }^{3}$ Output tracking ( $\mathrm{V}_{6} / \mathrm{V}_{7}$ ) | $\mathrm{V}_{\mathrm{CC}}=18$ to 27 V | 25 | 27 0.5 | 29 | dB |  |
| Zin | Audio amp input impedance | $\mathrm{f}=1 \mathrm{kHz}$ | 40 | 50 | 60 | k $\Omega$ |  |

NOTES

1. Measured with output at -3 dB , reference $\mathrm{V}_{\mathrm{IN}}=10 \mathrm{mV}, \Delta \mathrm{f}=25 \mathrm{kHz}$
2. $A M R=20 \log \frac{V_{0}(F M, \Delta f=7.5 \mathrm{kHz})}{V_{0}(A M, 30 \%)}$
3. Set $\mathrm{V}_{0}=1 \mathrm{Vrms} . \mathrm{A}_{\mathrm{V}}=20 \log \frac{1}{(\mathrm{~V} 3 \mathrm{rms})}$

DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+24 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | ULN2211 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Icc | Standby current |  | $\mathrm{V}_{\text {IN }}=0$ | 25 | 45 | 60 | mA |
| $\mathrm{V}_{6}$ | Terminal voltage |  | 10.5 | 12.5 | 14.5 | V |
| $\mathrm{V}_{10}$ |  |  |  | 1.4 |  | V |
| $\mathrm{V}_{11}$ |  |  |  | 1.4 |  | V |
| $\mathrm{V}_{14}, \mathrm{~V}_{15}$ |  |  |  | 4.0 |  | v |
| $\mathrm{V}_{16}$ |  |  |  | 8.0 |  | v |
| $\mathrm{V}_{8}$ |  |  | 14 | 14.5 | 16 | V |
| $\mathrm{V}_{2}$ |  |  |  | 10 |  | v |
| $V_{3}$ |  |  |  | 2.6 |  | V |

TYPICAL PERFORMANCE CHARACTERISTICS


## MAXIMUM ALLOWABLE POWER DISSIPATION



Figure 1

## TYPICAL APPLICATION



## sECTION IS General consumer

## DESCRIPTION

The NE543 is a servo amplifier and pulsewidth demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications.

## FEATURES

- 450mA load current capability without external power transistors
- Bidirectional bridge output with single power supply
- Low standby power drain


## PIN CONFIGURATION



## EQUIVALENT SCHEMATIC



NOTE
All resistor values are shown in ohms.

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Supply voltage | 6 | V |
| Power dissipation $\left(T_{A}=+25^{\circ} \mathrm{C}\right)$ | 830 | mW |
| Output current $\left(T_{A}=+25^{\circ} \mathrm{C}\right)$ | 450 | mA |

## BLOCK DIAGRAM AND TYPICAL CONNECTION



## NE543 SERVO

## DRIVER CONNECTION

The servo driver receives a nominal 1.5 ms pulse from the receiver-decoder. The length of the input pulse is compared with an internally generated pulse. If the pulse durations differ by more than an allowed amount (the deadband), a pulse derived from the difference is stretched and applied to the output stage. If the input pulse is shorter, the motor is driven so as to reduce the value of $\mathrm{R}_{3}$ and, hence, the internal pulse width. If the input pulse is longer, the motor is driven the other way so that $R_{3}$ increases and the internal pulse is lengthened. In this way, the control surface position can be made to follow the input pulse. The servo output
moves over 100 degrees for pulses between 1 and 2 ms . The pulses occur at 16 ms intervals.

The internal pulse generator pulse width is determined by $C_{2}$ and $R_{2}$ in series with $R_{3}$. Capacitor $\mathrm{C}_{4}$ decouples the pulse generator from the supply.
Deadband is controlled by Rd-1 and Rd-2. The 33ohm resistor sets deadband at about 4-5 microseconds (that is, the circuit will not drive the motor until the input pulse is 4 to 5 microseconds different from the internally generated pulse.)
Resistors RS-1 and RS-2 determine the
amount of pulse stretching. Capacitors CS1 and CS-2 are the pulse stretching capacitors. The value is not critical, but if changed RS-1 and RS-2 will have to be changed proportionately.

Resistors $\mathrm{R}_{8}$ and $\mathrm{R}_{9}$ are feedback resistors which prevent overshoot by adjusting the closed-loop damping

Capacitor $\mathrm{C}_{1}$ is the input coupling capacitor. Resistor $R_{1}$ can be any value in the range shown, but noise immunity is improved if it is at the low end of the range. Capacitor $\mathrm{C}_{3}$ bypasses the power supply at the device.

DC ELECTRICAL CHARACTERISTICS
$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}^{+}=4.8 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Supply voltage |  | 3.6 | 4.8 | 6.0 | V |
| Idle current |  |  | 8.0 | 10.0 | mA |
| Input bias current |  |  | 24 | 50 | $\mu \mathrm{~A}$ |
| Input impedance | Pin 4 or pin 6 to ground | 1.9 | 2.4 | 2.8 | $\mathrm{k} \Omega$ |
| Output voltage | $\mathrm{V}_{\mathrm{S}}=4.8 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=35 \Omega$ | 3.30 | 3.75 |  | V |
| Output current | $\mathrm{V}=6.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=11.5 \Omega$ | 340 | 385 |  | mA |
|  | $\mathrm{~V}=4.8 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=11.5 \Omega$ | 270 | 280 |  | mA |
|  | $\mathrm{~V}_{\mathrm{S}}=3.6 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=11.5 \Omega$ | 185 | 200 |  | mA |
| Output impedance | Quiescent, $\mathrm{RL}=\infty$ | 4.0 | 4.8 | 5.4 | $\Omega$ |
| Power dissipation | R |  | 39 | 48 | mW |
|  |  |  | 350 |  | mW |

TYPICAL PERFORMANCE CHARACTERISTICS


## TYPICAL APPLICATIONS



## DESCRIPTION

The NE544 is a servo amplifier and pulsewidth demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

## FEATURES

- 500 mA load current capability
- Bidirectional bridge output with single power supply
- Low standby power drain
- Adjustable deadband and trigger thresholds
- High linearity, 0.5\% maximum error
- Output drive for external PNP transistors (optional)
- Wide supply voltage range


## BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

|  | PARAMETER | RATING | UNIT |
| :--- | :--- | :---: | :---: |
| V+ | Supply voltage | 6.0 | V |
| $\mathrm{I}_{\mathrm{O}}$ | Output current | 500 | mA |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating temperature | -20 to +75 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {stg }}$ | Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## PIN CONFIGURATIONS



EQUIVALENT CIRCUIT SCHEMATIC


DC ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}=4.8 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | Limits |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\mathrm{v}_{\text {CC }}$ | Supply voltage |  |  | 3.2 | 4.8 | 6 | V |
| ${ }^{1} \mathrm{CC}$ | Supply current | Quiescent | 4.2 | 5.5 | 7.3 | mA |
| $\mathrm{V}_{\mathrm{TH}}$ | Input threshold On Off |  |  | 1.5 <br> 1.4 |  | $\bar{v}$ |
| $\mathrm{Z}_{\text {IN }}$ | Input resistance |  |  | 18 |  | k $\Omega$ |
| $\mathrm{V}_{\mathrm{OL}}$ <br> $V_{\mathrm{OH}}$ | Output voltage Low High | Pin 9 or $13, \mathrm{I}_{\mathrm{L}}=400 \mathrm{~mA}$ | 2.4 | $\begin{aligned} & 0.3 \\ & 3.9 \end{aligned}$ | 2.7 |  |
| $\mathrm{V}_{\mathrm{R}}$ | Reference voltage |  |  | 2.5 |  | v |
| PSRR | Power supply rejection <br> Minimum dead band <br> One shot temperature coefficient | $\begin{gathered} 3.5 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{S}} \leqslant 6 \mathrm{~V} \\ R D B=0 \end{gathered}$ |  | $\begin{gathered} .01 \\ 1 \\ .01 \end{gathered}$ |  | $\begin{gathered} \% / \mathrm{V} \\ \mu \mathrm{~s} \\ \% /{ }^{\circ} \mathrm{C} \\ \hline \end{gathered}$ |
|  | Standby power PNP drive current | Pin 10 and 12 |  | $\begin{aligned} & 27 \\ & 20 \end{aligned}$ |  | $\begin{gathered} \mathrm{mW} \\ \mathrm{~mA} \end{gathered}$ |




TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


PC BOARD-W PACKAGE


PC Board Layout Bottom View-4X

Parts Layout Top View

## sECTION 16 PHASE IOCHED LOOPS

## DESCRIPTION

The NE560 Phase Locked Loop (PLL) is a monolithic signal conditioner and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency ( $f_{0}$ ) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional potentiometer. The low pass filter, which determines the capture characteristics of the loop, is formed by the two capacitors and two resistors at the Phase Comparator output.
The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output, in differential form, is available for signal conditioning, frequency synchronization, multiplication and division applications. Terminals are provided for optional extended control of the tracking range, VCO frequency, and output dc level.

The monolithic signal conditionerdemodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of $\pm 1 \%$ to $\pm 15 \%$.

## FEATURES

- FM demodulation without tuned circuits
- Narrow bandpass: $\pm 14 \%$ adjustable
- Exact frequency duplication in high noise environment
- Wide tracking range : $\pm 15 \%$
- High linearity: $1 \%$ distortion max
- Frequency multiplication and division


## APPLICATIONS

- Tone decoders
- FM IF strips
- Telemetry decoders
- Data synchronizers
- Signal reconstitution
- Signal generators
- Modems
- Tracking filters
- SCA receivers
- FSK receivers
- Wide band high linearity detectors


## PIN CONFIGURATION



## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Maximum operating voltage | 26 | V |
| Input voltage | 1 | Vrms |
| Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation | 300 | mW |

NOTE
Limiting values above which serviceability may be impaired.

GENERAL ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified. 1

| PARAMETER | TEST CONDITIONS | NE560 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Lowest practical operating frequency Maximum operating frequency | Measured at 2 MHz , with both inputs ac grounded. Measured at 2 MHz | 15 | 0.1 30 |  | $\mathrm{Hz}$ <br> MHz |
| Supply current |  | 7 | 9 | 12 | mA |
| Minimum input signal for lock |  |  | 100 |  | $\mu \mathrm{V}$ |
| Dynamic range |  |  | 60 |  | dB |
| VCO Temp. coefficient ${ }^{2}$ |  |  | $\pm 0.06$ | $\pm 0.12$ | \%/ ${ }^{\circ} \mathrm{C}$ |
| VCO Supply voltage regulation |  |  | $\pm 0.3$ | $\pm 2$ | \%/V |
| Input resistance |  |  | 2 |  | $\mathrm{k} \Omega$. |
| Input capacitance |  |  | 4 |  | pF |
| dc level (pins 14 \& 15) |  | +10.6 | +12 | +13.4 | V |
| Input dc level (pins 12 \& 13) |  | +2.8 | +4 | +6.2 | V |
| Output dc level (pin 10) |  | +12.5 | +14 | +17 | V |
| (pin 9) |  | +12 | +14 | +16 | V |
| Available output swing | Measured at pin 9 (see Figure 1) | 30 | 4 |  | $V_{p-p}$ |
| AM rejection ${ }^{2}$ |  |  | 40 |  | dB |
| De-emphasis resistance |  |  | 8 |  | $\mathrm{k} \Omega$ |

NOTES

1. $15 \mathrm{~K} \Omega$ Pin 9 to GND; input Pin 12 or Pin 13 (ac ground unused input); optional controls not connected; $\mathrm{V}+=18 \mathrm{~V}$ unless otherwise specified.
2. Acceptance Test Sub Group C.

ELECTRICAL CHARACTERISTICS FM Applications (see Figure 2) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}+=18 \mathrm{~V}$ unless otherwise specified. 1


ELECTRICAL CHARACTERISTICS (Cont'd) Tracking Filter (see Figure 3)
$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}+=18 \mathrm{~V}$ unless otherwise specified. 1

| PARAMETER | TEST CONDITIONS | NE560 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Tracking range <br> Minimum signal to sustain lock | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{mVrms}$ <br> Seetypical performance characteristics | $\pm 5$ | $\begin{array}{r}  \pm 15 \\ 0.8 \end{array}$ |  | $\%$ of $f_{0}$ mVrms |
| VCO Output impedance <br> VCO Output swing <br> VCO Output dc level | Measured with high impedance probe with less than 10 pF capacitance with 100 kHz sideband separation and 3 kHz low pass filter. $\mathrm{C}_{1}=.001 \mu \mathrm{~F}, \mathrm{R}_{1}=50 \Omega$ | 0.4 | $\begin{gathered} 1 \\ 0.6 \\ +6.5 \end{gathered}$ |  | $\begin{gathered} k \Omega \\ V_{p-p} \\ V \end{gathered}$ |
| Side band suppression | Input $=1 \mathrm{mV}$ peak for carrier and each sideband. |  | 35 |  | dB |

NOTES

1. $15 \mathrm{~K} \Omega$ Pin 9 to GND; input Pin 12 or 13 (AC ground unused input); optional controls not connected.
2. Acceptance Test Sub Group C.

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

## FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF vCO TIMING CAPACITANCE




ORMALIZED TRACKING RANGE CONTROL CURRENT

## EXTERNAL CONTROLS

1. Loop Low Pass Filter (Pins 14 and 15)

The equivalent circuit for the loop lowpass filter can be represented as:

where $R_{A}(6 K \Omega)$ is the effective resistance seen looking into pin 14 or pin 15.
The corresponding filter transfer characteristics are:

$$
\frac{V_{2}}{V_{1}}(S)=\frac{1+S R_{1} C_{1}}{1+S\left(R_{1}+R_{A}\right) C_{1}}
$$

where $S$ is the complex frequency variable.
2. Loop Gain (Threshold) Control

The overall phase locked loop gain can be reduced by connecting a feedback resistor, Rf, across the low-pass filter terminals, pins 14 and 15. This causes the loop gain and the detection sensitivity to decrease by a factor $\propto$, $(\propto<1)$
where:

$$
\propto=\frac{R_{F}}{2 R_{A}+R_{F}}
$$

Reduction of loop gain may be desirable at high input signal levels ( $\mathrm{V}_{\mathrm{IN}}>30 \mathrm{mV}$ ) and at high frequencies ( $f_{0}>5 \mathrm{MHz}$ ) where excessively high loop gain may cause instability.
3. Tracking Range Control (Pin 7)

Any bias current, $\mathrm{I}_{\mathrm{b}}$, injected into the tracking range control reduces the tracking range of the PLL by decreasing the output of the limiter. The variations of the tracking range and the center frequency, as a function of $I_{b}$, are shown in the characteristic curves with $\mathrm{I}_{\mathrm{b}}$ defined positive going into the tracking range control terminal. This terminal is normally at a dc level of +0.6 volts and presents an impedance of $600 \Omega$.

## 4. External Fine Tuning (Pin 6)

Any bias current injected into the fine tuning terminal increases the frequency of oscillation, $\mathrm{f}_{\mathrm{o}}$, as shown in the characteristic curves. This current is defined positive into the fine tuning terminal. This terminal is at a typical dc level of +1.3 volts and has a dynamic impedance of $100 \Omega$ to ground.
5. Offset Adjustment (Pin 11)

Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier, setting the dc level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.
Nominally this terminal is at +4 Vdc and has an input impedance of $3 \mathrm{k} \Omega$. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.
6. De-emphasis Filter (Pin 10)

The de-emphasis terminal is normally used when the PLL is used to demodulate frequency modulated audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3 dB bandwidth of the output amplifier (see Figure 2) is related to the de-emphasis capacitor, $C_{D}$, as:

$$
\mathrm{f}_{3 \mathrm{~dB}}=\frac{1}{2 \pi R_{D} C_{D}}
$$

where $R_{D}$ is the 8000 ohm resistance seen looking into the de-emphasis terminal.

When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, the de-emphasis terminal should be ac grounded.

## TEST CIRCUITS



## DESCRIPTION

The NE561 Phase Locked Loop (PLL) is a monolithic signal conditioner, and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency ( $f_{0}$ ) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional potentiometer. The low pass filter, which determines the capture characteristics of the loop is formed by the two capacitors and two resistors at the Phase Comparator output.
The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output is available for signal conditioning, frequency synchronization, multiplication and division applications. Terminals are provided for optional external control of the tracking range, VCO frequency, and output dc level. An analog multiplier block is incorporated into the PLL system to provide frequency selective synchronous AM detection capability.
The monolithic signal conditionerdemodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of $\pm 1 \%$ to $\pm 15 \%$.

## FEATURES

- FM demodulation without tuned circuits
- Synchronous AM detection
- Narrow band pass to $\pm 1 \%$
- Exact frequency duplication in high noise environment
- Adjustable tracking range
- Wide tracking range to $\pm 15 \%$
- High linearity: 1\% distortion max
- Frequency multiplication and division through harmonic locking


## APPLICATIONS

- Tone decoders AM-FM-IF strips
- Telemetry decoders data synchronizers
- Signal reconstitution
- Signal generators
- Modems
- Tracking filters
- SCA receivers
- FSK receivers
- Wide bank high linearity detectors
- Synchronous detectors
- AM receiver


## PIN CONFIGURATION



## BLOCK DIAGRAM

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Maximum operating voltage | 26 | V |
| Input voltage | 1 | Vrms |
| Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation | 300 | mW |



Maximum operating voltage

Power dissipation
mW
-

GENERAL ELECTRICAL CHARACTERISTICS $15 \mathrm{k} \Omega$ pin 9 to GND; input pin 12 or pin 13 (AC ground unused input); optional controls not connected; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}+=18 \mathrm{~V}$ unless otherwise specified.

| PARAMETER |  | TEST CONDITIONS | NE561 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\begin{aligned} & \text { vco } \\ & \text { vco } \end{aligned}$ | Lowest practical operating frequency Maximum operating frequency |  | Measured at 2 MHz , with both inputs AC grounded Measured at 2 MHz | 158 | 0.1 30 | 13 | $\begin{gathered} \mathrm{Hz} \\ \mathrm{MHz} \end{gathered}$ |
|  | Supply current <br> Minimum input signal for lock Dynamic range | $\begin{gathered} 10 \\ 100 \\ 60 \end{gathered}$ |  |  | mA $\mu \mathrm{V}$ dB |  |
|  | Supply voltage regulation | $\begin{gathered} \pm 0.06 \\ \pm 0.3 \end{gathered}$ |  |  | $\begin{gathered} \pm 0.12 \\ \pm 2 \end{gathered}$ | $\begin{aligned} & \% /{ }^{\circ} \mathrm{C} \\ & \% / \mathrm{V} \end{aligned}$ |
|  |  |  |  |  |  |  |
|  | Input resistance Input capacitance | 2 |  |  |  | k $\mathrm{pF}^{\text {P }}$ |
|  | Input dc level | Measured at pins 12 and 13 | $\begin{gathered} +2.8 \\ +10.6 \\ +13 \end{gathered}$ | +4 | $\begin{gathered} +6.0 \\ +13.4 \\ +17 \end{gathered}$ | V |
|  |  | Measured at pins 14 and 15 |  | +12 |  | V |
|  |  | Measured at pin 10 |  | +15 |  | V |
|  | Output dc level Available output swing AM rejection* De-emphasis resistance | Measured at pin 9 Measured at pin 9 See Figure 3 | +12 | +14 | +16 | $\begin{gathered} \mathrm{V} \\ \mathrm{Vp-p} \\ \mathrm{~dB} \\ \mathrm{k} \Omega \end{gathered}$ |
|  |  |  | 30 | $\begin{gathered} 4 \\ 40 \\ 8 \end{gathered}$ |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

*NOTE
Acceptance Test Sub Group C.

ELECTRICAL CHARACTERISTICS (for tracking filter, Figure 1). $15 \mathrm{k} \Omega$ pin 9 to GND; input pin 12 or pin 13 (AC ground unused input); optional controls not connected; $T_{A}=25^{\circ} \mathrm{C}$, $\mathrm{V}+=18 \mathrm{~V}$ unless otherwise specified.


ELECTRICAL CHARACTERISTICS (for FM applications, Figure 2) $15 \mathrm{k} \Omega$ pin 9 to GND; input pin 12 or 13 (AC ground unused input); optional controls not connected; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, $\mathrm{V}+=18 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE561 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| 10.7MHz OPERATION- <br> DEVIATION $=75 \mathrm{kHz}$, SOURCE IMPEDANCE $=50 \Omega$ |  |  |  |  |  |
| Detection threshold Demodulated output amplitude | $\mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}, \underset{1 \mathrm{kHz}}{\text { modulation frequency }}$ | 30 | $\begin{gathered} 120 \\ 60 \end{gathered}$ | 300 | $\begin{gathered} \mu V \\ m V \end{gathered}$ |
| Distortion* <br> Signal to noise ratio ( $\frac{S+N}{N}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}, \text { modulation frequency } \\ & \mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVZ} \mathrm{mVms}, \begin{array}{c} \text { modulation frequency } \\ 1 \mathrm{kHz} \end{array} \end{aligned}$ |  | $\begin{gathered} .3 \\ 35 \end{gathered}$ | 1 | \%T.H.D. dB |
| 4.5MHz OPERATION- <br> DEVIATION $=25 \mathrm{kHz}$; SOURCE IMPEDANCE $=50 \Omega$ |  |  |  |  |  |
| Detection threshold Demodulation output amplitude | $\mathrm{VIN}=1 \mathrm{mVrms}, \underset{1 \mathrm{kHz}}{\text { modulation frequency }}$ | 30 | $\begin{gathered} 120 \\ 60 \end{gathered}$ | 300 | $\begin{aligned} & \mu V \\ & \mathrm{mV} \end{aligned}$ |
| Distortion* <br> Signal to noise ratio ( $\frac{S+N}{N}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}, \begin{array}{c} \text { modulation frequency } \\ 1 \mathrm{kHz} \\ \mathrm{~V}_{\mathrm{IN}}=1 \mathrm{mVrms}, \text { modulation frequency } \\ 1 \mathrm{kHz} \end{array} \end{aligned}$ |  | $\begin{gathered} 0.3 \\ 35 \end{gathered}$ | 1.0 | \%T.H.D. dB |
| WIDE DEVIATION- <br> $\Delta \mathrm{f} / \mathrm{f}_{\mathrm{o}}=5 \%, \mathrm{f}_{\mathrm{o}}=4.5 \mathrm{MHz}$, DEVIATION $=$ <br> $225 \mathrm{kHz} @ 1 \mathrm{kHz}$ MODULATION RATE |  |  |  |  |  |
| Detection threshold Demodulated output <br> Distortion* <br> Signal to noise ratio $\left(\frac{S+N}{N}\right)$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=5 \mathrm{mV} \mathrm{rms} \\ & \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{mVrms} \\ & \mathrm{~V}_{\mathrm{IN}}=5 \mathrm{mVrms} \end{aligned}$ | 0.2 | $\begin{gathered} \hline 1 \\ 0.5 \\ 0.8 \\ 50 \end{gathered}$ | 5 | $\begin{array}{\|c\|} \hline \mathrm{mV} \\ \mathrm{Vrms} \\ \% \mathrm{~T} . \mathrm{H} . \mathrm{D} . \\ \mathrm{dB} \end{array}$ |

*NOTE
Acceptance Test Sub Group C.

ELECTRICAL CHARACTERISTICS (for AM synchronous detector, Figure 4). $15 \mathrm{k} \Omega$ pin 9 to GND; input pin 12 or pin 13 (AC ground unused input); optional controls not connected; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$; $\mathrm{V}+=18 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | NE561 |  |  | UNIT |
| :--- | :---: | :---: | :---: | :---: |
|  | Min | Typ | Max |  |
| Input impedance |  | 3 |  | $\mathrm{k} \Omega$ |
| Output impedance |  | 8 |  | $\mathrm{k} \Omega$ |
| Output dc level | +10 | +14 | +17 | V |
| AM conversion gain | 3 | 12 |  | dB |
| Out of band rejection |  | 30 |  | dB |
| Distortion |  | 1 |  | $\%$ T.H.D. |

## TYPICAL PERFORMANCE CHARACTERISTICS

MINIMUM INPUT SIGNAL
AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $\mathbf{f}_{\text {in }}=\mathbf{f o}=2.0 \mathrm{MHz}$


TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL


AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL


CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT


THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (fo)


CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CURRENT


FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE


NORMALIZED TRACKING RANGE
AS A FUNCTION OF RANGE CONTROL CURRENT


## EXTERNAL CONTROLS Loop Low Pass Filter (Pins 14 and 15)

The equivalent circuit for the loop low-pass filter can be represented as:

where $R_{A}(6 K \Omega)$ is the effective resistance seen looking into pin 14 or pin 15.
The corresponding filter transfer characteristics are:

$$
\frac{V_{2}}{V_{1}}(S)=\frac{1+S R_{1} C_{1}}{1+S\left(R_{1}+R_{A}\right) C_{1}}
$$

where $S$ is the complex frequency variable.

## Loop Gain (Threshold) Control

The overall phase lock loop gain can be reduced by connecting a feedback resistor, $R_{f}$ across the low-pass filter terminals, pins 14 and 15. This causes the loop gain and the detection sensitivity to decrease by a factor $\propto$, ( $\propto<1$ ), where:

$$
\propto=\frac{R_{f}}{2 R_{A}+R_{f}}
$$

Reduction of loop gain may be desirable at high input signal levels $\left(\mathrm{V}_{\mathrm{IN}}>30 \mathrm{mV}\right)$ and at high frequencies (fo $>5 \mathrm{MHz}$ ) where excessively high PLL loop gain may cause instability.

## Tracking Range Control (Pin 7)

Any bias current, $\mathrm{I}_{\mathrm{b}}$, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of $\mathrm{I}_{\mathrm{b}}$, are shown in the characteristics curves with $\mathrm{I}_{\mathrm{b}}$ defined positive going into the tracking range control terminal. This terminal is normally at a dc level of +0.6 volts and presents an impedance of $600 \Omega$.

## External Fine Tuning (Pin 6)

Any bias current injected into the fine tuning terminal increases the frequency of oscillation, fo, as shown in the characteristic curves. This current is defined positive into the fine tuning terminal. This terminal is at a typical dc level of +1.3 volts and has a dynamic impedance of $100 \Omega$ to ground.

## Offset Adjustment (Pin 11)

Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the dc level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.

Nominally this terminal is at +4 Vdc and has an input impedance of $3 \mathrm{k} \Omega$. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

## De-emphasis Filter (Pin 10)

The de-emphasis terminal is normally used when the PLL is used to demodulate frequency modulated audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3dB bandwidth of the output amplifier (see Figure 2) is related to the de-emphasis capacitor, $C_{D}$, as:

$$
f_{3 \mathrm{~dB}}=\frac{1}{2 \pi R_{D} C_{D}}
$$

where $R_{D}$ is the 8000 ohm resistance seen looking into the de-emphasis terminal.

When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, the de-emphasis terminal should be AC grounded.

## AM Post-Detection Filter (Pin 1)

The capacitor $C x$ connected between Pin 1 and ground serves as low-pass filter for synchronous AM detection with a transfer characteristic, $\mathrm{F}_{2}(\mathrm{~S})$, given as:

$$
F_{2}(S)=\frac{1}{1+S R_{x} C_{x}}
$$

where $R_{x}=8 k \Omega$ is the resistance seen looking into Pin 1.

## TYPICAL TEST CIRCUITS

## TEST CIRCUIT FOR TRACKING FILTER


$\mathrm{Cc}=$ Coupling capacitors
$C_{B}=$ Bypass capacitor
$C_{1}=$ Low pass filter capacitor
$\mathrm{C}_{0}=$ VCO frequency set capacitor

## TEST CIRCUIT FOR FM DEMODULATION



Figure 2

Figure 1

## TYPICAL TEST CIRCUITS (Cont'd)

## test circuit for am rejection


$G_{1}=F M$ generator with $f_{C}=f 0 \approx 4 \mathrm{MHz}$ $\Delta f=40 \mathrm{kHz}, f_{\text {mod }}=1 \mathrm{kHz}$
$\mathrm{G}_{2}=$ Audio generator with $\mathrm{f}_{\mathrm{A}}=400 \mathrm{kHz}$
$M_{1}=$ Balanced modulator carrier supplied by $G_{1}$ AM modulation provided by $\mathrm{G}_{2}$
$A_{1}=50 \Omega$ attenuator pad with signal level into pin 12 adjusted to 1 mVrms .
$F_{1}=1 \mathrm{kHz}$ bandpass filter. $\mathrm{Q}=20$
$F_{2}=400 \mathrm{~Hz}$ bandpass filter with $Q=50$, with 1 kHz trap.
$A M R=\frac{V_{1}}{V_{2}}$ in $d B V_{1}$ and $V_{2}$ are rms voltmeter readings.
Figure 3

## TEST CIRCUIT FOR AM SYNCHRONOUS DETECTOR



Figure 4

## DESCRIPTION

The NE562 Phase Locked Loop (PLL) is a monolithic signal conditioner and demodulator system comprising a VCO, phase comparator, amplifier and low pass filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency ( $\mathrm{f}_{\mathrm{o}}$ ) of the VCO. This VCO frequency is set by an external capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by 2 capacitors and 2 resistors at the phase comparator output.

This PLL has 2 sets of differential inputs, one for the FM/RF input and one for the phase comparator local oscillator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are selfbiased. An internally regulated voltage source is provided to bias the phase comparator local oscillator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits in signa conditioning and synchronization, frequency multiplication and division applications. Terminals are also provided for the optional extension of the tracking range.

The monolithic signal conditionerdemodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of $\pm 1 \%$ to $\pm 15 \%$.

## FEATURES

- Frequency multiplication and division
- Signal conditioning and side-band suppression
- FM demodulation without tuned circuits
- Narrow bandpass to $\pm 1 \%$
- Adjustable tracking range to $\pm 15 \%$
- Exact frequency duplication in high noise environment
- High linearity: $1 \%$ distortion maximum at 1\% deviation


## APPLICATIONS

- Frequency synthesizers
- Data synchronizers
- Signal conditioning
- Tracking filters
- Telemetry decoders
- Modems
- FM IF strips and demodulators
- Tone decoders
- FSK receivers
- Wideband high linearity FM demodulators

PIN CONFIGURATION


## BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
(Limiting values above which serviceability may be impaired)

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Maximum operating voltage | 30 | V |
| Input voltage | 3 | Vrms |
| Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation | 300 | mW |

EQUIVALENT SCHEMATIC


GENERAL ELECTRICAL CHARACTERISTICS 15,000 ohms pin 9 to ground; 12,000 ohms pins 3 and 4 to ground; pins 2 and 15 to pin 1 through 1,000 ohms; input to pin 11 or 12 with unused input at AC ground; range control not connected; $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=18$ volts unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE562 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Lowest practical operating frequency Maximum operating frequency |  | 15 | $\begin{aligned} & 0.1 \\ & 30 \end{aligned}$ |  | $\begin{gathered} \mathrm{Hz} \\ \mathrm{MHz} \end{gathered}$ |
| Supply current <br> Minimum input signal for lock Dynamic range |  | 10 | $\begin{gathered} 12 \\ 200 \\ 80 \end{gathered}$ | 15 | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~V} \\ & \mathrm{~dB} \end{aligned}$ |
| VCO temp. coefficient* <br> VCO supply voltage regulation | Measured at 2 MHz Measured at 2 MHz |  | $\begin{gathered} \pm 0.06 \\ \pm 0.3 \end{gathered}$ | $\pm 0.15$ $\pm 2$ | $\begin{aligned} & \% /{ }^{\circ} \mathrm{C} \\ & \% / \mathrm{V} \end{aligned}$ |
| Input resistance Input capacitance |  |  | $\begin{aligned} & 2 \\ & 4 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \end{aligned}$ |
| Input DC level DC level | Measured at pins 11 and 12 Measured at pins 13 and 14 | +3 +11 +10 | +4 +13 +12 | +6 +16 +15 | v |
| Output DC level | Measured at pin 9 | +10 | +12.5 | +15 | V |
| Available output swing AM rejection* De-emphasis resistance | Measured at pin 9 | 30 | 4 40 8 |  | $\begin{aligned} & \mathrm{Vp}-\mathrm{p} \\ & \mathrm{~dB} \\ & \mathrm{k} \Omega \end{aligned}$ |
| De-emphasis DC level Bias reference | Measured at pin 10 Measured at pin 1 | $\begin{aligned} & +11 \\ & +6.5 \end{aligned}$ | $\begin{aligned} & +14 \\ & +7.5 \end{aligned}$ | $\begin{aligned} & +16 \\ & +8.5 \end{aligned}$ | $\begin{aligned} & \text { v } \\ & \text { v } \end{aligned}$ |

*NOTE
Acceptance test Sub Group C.

## ELECTRICAL CHARACTERISTICS FOR FM APPLICATIONS

15,000 ohms pin 9 to ground; input to pin 11 or pin 12 (AC ground unused input); range control not connected; $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}+=18$ volts unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE562 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| 10.7 MHz OPERATION-DEVIATION $=75 \mathrm{kHz}$, SOURCE IMPEDANCE $=50 \Omega$ |  |  |  |  |  |
| Detection tnreshold <br> Demodulated output amplitude <br> Distortion* <br> Signal to noise ratio $\left(\frac{S+N}{N}\right)$ | $\mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}$, modulation frequency 1 kHz <br> $\mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}$, modulation frequency 1 kHz <br> $\mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}$, modulation frequency 1 kHz | 30 | $\begin{gathered} 200 \\ 70 \\ 0.5 \\ 35 \end{gathered}$ | 500 | $\mu \mathrm{V}$ mVrms \%T.H.D. dB |
| 4.5 MHz OPERATION-DEVIATION $=25 \mathrm{kHz}$, SOURCE IMPEDANCE $=50 \Omega$ |  |  |  |  |  |
| Detection threshold Demodulated output amplitude Distortion* Signal to noise ratio $\left(\frac{\mathrm{S}+\mathrm{N}}{\mathrm{N}}\right)$ | $\mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}$, modulation frequency 1 kHz <br> $\mathrm{V} / \mathrm{N}=1 \mathrm{mVrms}$, modulation frequency 1 kHz <br> $\mathrm{V}_{\mathrm{IN}}=1 \mathrm{mVrms}$, modulation frequency 1 kHz | 30 | $\begin{gathered} \hline 200 \\ 60 \\ 0.5 \\ 35 \end{gathered}$ | 500 | $\mu V$ <br> $m V r m s$ <br> $\%$ T.H.D. <br> $d B$ |
| WIDE DEVIATION $-\Delta f / f_{0}=5 \%$, INPUT $=4.5 \mathrm{MHz}$, DEVIATION $=225 \mathrm{kHz} @ 1 \mathrm{kHz}$ MODULATIONRATE |  |  |  |  |  |
| Detection threshold Demodulated output Distortion* Signal to noise ratio $\left(\frac{S+N}{N}\right)$ | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{mVrms}$ <br> $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{mVrms}$ <br> $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{mVrms}$ | 0.3 | 1 1 1 0.8 50 | 5 | $\mu \mathrm{V}$ mVrms \%T.H.D. dB |

*NOTE
Acceptance test Sub Group C.
ELECTRICAL CHARACTERISTICS FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS
APPLICATIONS Input to pin 11 or pin 12; AC ground unused input; range control not connected; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}+=18$ volts unless otherwise specified.

| PARAMETER | TEST CONDITIONS | NE562 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Tracking range | 200 mVp -p square wave input | $\pm 5$ | $\pm 15$ |  | $\%$ of $\mathrm{f}_{\mathrm{o}}$ |
| Input resistance Input capacitance Input DC level |  |  | $\begin{aligned} & 2 \\ & 4 \\ & 4 \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \\ & \mathrm{~V} \end{aligned}$ |
| VCO output impedance <br> VCO output swing |  | 3 | $\begin{aligned} & 1.3 \\ & 4.5 \end{aligned}$ | 2.5 | $\begin{gathered} k \Omega \\ V p-p \end{gathered}$ |
| VCO output DC level VCO signal/noise ratio | Inputs at AC ground |  | $\begin{aligned} & 12 \\ & 60 \end{aligned}$ |  | $\begin{gathered} \mathrm{V} \\ \mathrm{~dB} \end{gathered}$ |

TYPICAL PERFORMANCE CHARACTERISTICS



## TEST CIRCUITS

## TEST CIRCUIT FOR FM DEMODULATION


$\mathrm{C}_{\mathrm{B}}=$ Bypass Capacitor $\mathrm{C}_{\mathrm{C}}=$ Coupling Capacitor $\mathrm{C}_{1}=$ Low Pass Filter Capacitor
Figure 1

TEST CIRCUIT FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS

$\mathrm{C}_{B}=$ Bypass Capacitor $\mathrm{C}_{\mathrm{C}}=$ Coupling Capacitor $C_{1}=$ Low Pass Filter Capacitor
Figure 2

## 562 APPLICATIONS INFORMATION

## Bias Reference

Pin 1 of the 562 is an internally regulated bias reference voltage supply which should be used as a source of bias current for the phase comparator input terminals, pins 2 and 15. Biasing may be achieved as shown in Figure 3.


Figure 3

## Phase Comparator Loop Inputs

The 562 has an open loop between the VCO and the phase comparator. Once biasing of the comparator is accomplished, as described in Bias Reference above, loop closure can be accomplished by capacitive coupling between either one or both inputs of the phase comparator and the VCO output. A divider or counter may be enclosed in the loop at this point for frequency synthesis applications or a flip-flop may be used to ensure that the output waveform has a $50 \%$ duty cycle. If large signal swings, greater than 2 volts, are to be applied to the phase comparator inputs, a limiting resistor should be used in series with the coupling capacitors to ensure that the maximum input voltage rating is not exceeded.

## VCO Output

Square wave VCO outputs of both polarities ( $0^{\circ}$ and $180^{\circ}$ ) buffered by an amplifier are available at pins 3 and 4. For proper operation of the buffer amplifier, pins 3 and 4 must be returned to ground (or the negative supply) through resistors, typically 12,000 ohms. The value of these resistors may be reduced provided that total power dissipated in the 562 does not exceed 300 milliwatts or the total average current in each emitter does not exceed 4 mA . The output amplitude is typically 4.5 volts positive with respect to pin $8(\mathrm{~V}+=12$ volts $)$.

## VCO Tuning

Setting the free-running frequency of the VCO is accomplished easily with one timing capacitor connected between pins 5 and 6. For the 562 Phase Locked Loop, fine tuning of the free-running frequency may be accomplished in either or both of two ways. The first method uses a trimmer capacitor connected in parallel with the VCO timing capacitor. This is the simplest technique and requires the smallest number of extra
components but at the lower frequencies may be difficult to implement. The second technique incorporates two resistors and a voltage source. The resistors are connected between each of the timing capacitor terminals and a voltage source as shown in Figure 4.


The percent change in the VCO freerunning frequency, fo, as a function of the voltage applied to point (A) is shown in the curves of Figure 5. Note that with this fine tuning technique, it is possible to increase the VCO free-running frequency to a value greater than possible with just a trimmer capacitor alone. A formula for the approximation of the VCO frequency as a function of the voltage at point (A), the resistance values and the starting frequency, is given below:

$$
f=f_{0}\left[1-\frac{V_{A}-6.4}{1300 R}\right]
$$

The recommended resistance range of $R$ is 20,000 to 60,000 ohms.


## Loop Gain Characteristics

The overall open loop gain of the 562 PLL can be expressed as:

$$
\mathrm{K}_{0}=\mathrm{K}_{1} \mathrm{~K}_{2}
$$

where:
$\mathrm{K}_{0}=$ total open loop gain
$\mathrm{K}_{1}=$ phase comparator and amplifier conversion gain
$\mathrm{K}_{2}=\mathrm{VCO}$ conversion gain

The VCO conversion gain, $\mathrm{K}_{2}$, is the change of VCO frequency per unit of error voltage. In this particular design, it is numerically equal to the VCO frequency, i.e.,

$$
\begin{aligned}
& \mathrm{K}_{2}=\mathrm{f}_{\mathrm{o}} \mathrm{~Hz} / \text { Volt } \\
& \text { or } \\
& \mathrm{K}_{2}=2 \pi \mathrm{f}_{\mathrm{o}} \text { radians/Volt-second }
\end{aligned}
$$

The phase comparator and amplifier conversion gain, $\mathrm{K}_{1}$, is proportional to input signal amplitude for low input levels, $\mathrm{V}_{\mathrm{S}} \leq$ 40 mVrms , and is constant and equal to about 1.5 volts/radian for higher amplitudes. Therefore, $\mathrm{K}_{1}$ can be approximated as:

$$
\mathrm{K}_{1} \cong \frac{.04 \mathrm{~V}_{\mathrm{s}}}{\sqrt{1+\left(\frac{\mathrm{V}_{\mathrm{s}}}{40}\right)^{2}}}
$$

where
$V_{S}=$ input signal in $m V r m s$.

## Signal Input

The input structure is basically differential and may be used in this manner. Biasing is supplied to the input terminals from an internal regulated supply so signal inputs must be capacitively coupled. In most applications where the input is single-ended, the unused input should be AC grounded.

## Demodulated Output

Pin 9 is a low impedance output terminal for the loop error voltage. It is at this point that the demodulated FM output is obtained. When used, it must be biased by a resistor to ground (or negative supply), and the resistor value may be adjusted downward provided that the output current does not exceed 5 mA or the dissipation in the 562 does not exceed the absolute maximum ratings. When not used, pin 9 may be left open.

## De-emphasis Filter

The de-emphasis terminal, pin 10, is normally utilized when the PLL is used to demodulate frequency modulated audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications it may be used to shape the output response. The 3dB bandwidth of the output amplifier is related to the de-emphasis capacitor, $C_{D}$, as:

$$
f_{3 d B}=\frac{1}{2 \pi R_{D} C_{D}}
$$

where $R_{D}$ is the 8000 ohms resistance seen looking into the de-emphasis terminal.
When the PLL system is utilized for applications not requiring the use of the output amplifier, pin 10 should be AC grounded.

## 562 APPLICATIONS INFORMATION (Cont'd)

## Tracking Range Control (Pin 7)

Any bias current, $\mathrm{l}_{\mathrm{b}}$, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of $\mathrm{I}_{\mathrm{b}}$, are shown in the characteristic curves with $l_{b}$ defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 volts and presents an impedance of $600 \Omega$.

## Low Pass Filter

In most applications, a loop low-pass filter should be connected between pins 13 and 14 and ground. It is used to set the loop response time, controlling the capture range and the rejection of out-of-band information. Four filter configurations and their transfer functions are shown in Figures 6 through 9. For VCO operating frequencies below 5 MHz , configurations shown in Figures 6 and 7 may be used. At higher frequencies, configurations shown in Figures 8 and 9 should be used to ensure loop stability. R is the internal resistance seen looking into


Figure 6


Figure 8


Figure 7


Figure 9
the low pass filter terminals, Pins 13 and 14 and is nominally 6000 ohms.

## Loop Gain (Threshold) Control

The overall phase locked loop gain can be reduced by connecting a resistor, RF, across the low-pass filter terminals, pins 13 and 14. This causes the loop gain and the detection sensitivity to decrease by a factor $\alpha,(\alpha<1)$ where:

$$
\alpha=\frac{R_{F}}{12,000+R_{F}}
$$

Reduction of loop gain may be desirable at operating frequencies greater than 5 MHz because, at these frequencies, high loop gain may cause instability.

## Static Loop Phase-Error

When the PLL is in lock, the VCO outputs have a nominal $\pm 90^{\circ}$ phase shift with respect to the input signal. Due to internal offsets, this nominal angle at perfect lock condition may shift a few degrees, typically $\pm 5^{\circ}$.

## DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50 MHz . As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

## APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators


## FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Operation to 50 MHz
- Operates as a modulator
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications

PIN CONFIGURATION


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER |  | RATING | UNIT |
| :---: | :---: | :---: | :---: |
| V+ | Supply voltage Pin 1 Pin 10 | $\begin{gathered} 14 \\ 6 \end{gathered}$ | V |
| $P_{D}$ | Power dissipation | 400 | mW |
| $\mathrm{T}_{\text {A }}$ | Operating temperature | 0 to 70 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ stg | Storage temperature | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to 50 MHz . In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

Equation 1

$$
v_{o}=\frac{\left(f_{\text {in }}-f_{o}\right)}{k_{v c o}}
$$

$\mathrm{K}_{\mathrm{vco}}=$ conversion gain of the VCO
$f_{\text {in }}=$ frequency of the input signal
$f_{o}=$ free running frequency of the VCO
The process of recovering FSK signals involves the conversion of the PLL output into digital, logic compatible signals. For high data rates, a considerable amount of carrier

DC ELECTRICAL CHARACTERISTICS $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| PARAMETER |  | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\mathrm{f}_{0}$ | Lock range <br> Frequency of operation of VCO <br> Frequency drift with temperature <br> Frequency change with supply voltage |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{2}=400 \mu \mathrm{~A} \\ \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C}, \mathrm{f}_{\mathrm{O}}=5 \mathrm{MHz} \\ \mathrm{~V}+=4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & 25 \\ & 45 \end{aligned}$ | $\begin{gathered} 40 \\ 50 \\ 400 \\ 3 \end{gathered}$ | $\begin{gathered} 850 \\ 6 \end{gathered}$ | $\begin{gathered} \% \\ \mathrm{MHz} \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |
|  | Demodulated output voltage | $\pm 1 \%$ input deviation <br> $\pm 10 \%$ input deviation, $\mathrm{f}_{\mathrm{O}}=5 \mathrm{MHz}$ | $\begin{gathered} 10 \\ 100 \end{gathered}$ | $\begin{gathered} \hline 14 \\ 140 \end{gathered}$ |  | mVrms |
|  | Output voltage linearity Signal to noise ratio AM rejection |  |  | $\begin{gathered} 3 \\ 40 \\ 35 \end{gathered}$ |  | \% <br> dB <br> dB |
| $\begin{aligned} & \mathrm{I}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{LC}} \end{aligned}$ | Supply current <br> Leakage current <br> Output current | $\begin{gathered} 5 \mathrm{~V} \\ \text { Pin } 9 \\ \text { Pin } 9 \end{gathered}$ |  | $\begin{gathered} 30 \\ 1 \end{gathered}$ | $\begin{gathered} 40 \\ 10 \\ 6 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \\ & \mathrm{~mA} \end{aligned}$ |
| V+ | Supply voltage | $\begin{array}{lr} \hline \text { Pin } 1 \\ \operatorname{Pin} 10 \end{array}$ | $\begin{aligned} & 4.5 \\ & 4.5 \end{aligned}$ |  | $\begin{aligned} & 12 \\ & 5.5 \end{aligned}$ | V |

will be present at the output due to the the use of complicated filters, a comparator with hysterisis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of $f_{\text {in }}$ from $f_{0}$. Since this differs from system to system, it is necessary that the hysterisis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysterisis of the Schmitt trigger.
For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in $f_{\text {in }}$ itself may be less than the change in $f_{O}$ due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

## VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors $Q_{21}$ and $Q_{23}$ with current sources $Q_{25}-Q_{26}$ form the basic oscillator. The free running frequency
of the oscillator is shown in the following equation:

Equation 2

$$
\begin{aligned}
f_{O} & =\frac{1}{16 R_{C} C_{1}} \\
R_{C} & =R_{19}=R_{20} \\
C_{1} & =\text { frequency setting external capacitor }
\end{aligned}
$$

Variation of $V_{d}$ changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current $I_{R}$ with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

## Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied changing the current in $Q_{4}$ and $Q_{15}$ which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

## Post Detection Processor

## Section

The post detection processor consisits of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear

FM demodulation. The comparator has adjustable hysterisis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transconductance amplifier $Q_{42}-Q_{43}$ with a capacitor at the output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

## Equation 3

$$
\mathrm{v}_{0}=\frac{\mathrm{g}_{\mathrm{m}}}{\mathrm{C}_{2}} \int \mathrm{v}_{\text {in }} \mathrm{dt}
$$

$\mathrm{g}_{\mathrm{m}}=$ transconductance of the amplifier
$\mathrm{C}_{2}=$ capacitor at the output (pin 14)
$\mathrm{V}_{\text {in }}=$ signal voltage at amplifier input
With proper selection of $\mathrm{C}_{2}$, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysterisis is made up of $Q_{49}-Q_{50}$ with positive feedback being provided by $Q_{47}-Q_{48}$. The hysterisis is varied by changing the current in $Q_{52}$ with a resulting variation in the loop gain of the comparator. This method of hysterisis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula
Free running frequency of VCO is shown by the following equation:

## Equation 4

$$
f_{O}=\frac{1}{16 R_{C} C_{1}} \text { in } \mathrm{Hz}
$$

$$
R_{C}=100 \Omega
$$

$\mathrm{C}_{1}=$ external cap in farads

## LOOP FILTER



## EQUIVALENT SCHEMATIC



## DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500 kHz . The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

## FEATURES

- Highly stable center frequency (200ppm $/{ }^{\circ} \mathrm{C}$ typ.)
- Wide operating voltage range ( $\pm 6$ to $\pm 12$ volts)
- Highly linear demodulated output (0.2\% typ.)
- Center frequency programming by means of a resistor or capacitor, voltage or current
- TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider
- Highly linear triangle wave output
- Reference output for connection of comparator in frequency discriminator
- Bandwidth adjustable from $< \pm 1 \%$ to $> \pm 60 \%$
- Frequency adjustable over 10 to 1 range with same capacitor


## APPLICATIONS

- Frequency shift keying
- Modems
- Telemetry receivers
- Tone decoders
- SCA receivers
- Wideband FM discriminators
- Data synchronizers
- Tracking filters
- Signal restoration
- Frequency multiplication \& division


## PIN CONFIGURATIONS



## BLOCK DIAGRAM



## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $T_{A}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Maximum operating voltage | 26 | V |
| Input voltage | 3 | $\mathrm{Vp-p}$ |
| Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE565 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE565 | 300 | mW |

ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{C C}= \pm 6 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | TEST CONDITIONS | SE565 |  |  | NE565 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| SUPPLY REQUIREMENTS <br> Supply voltage Supply current |  | $\pm 6$ | 8 | $\begin{aligned} & \pm 12 \\ & 12.5 \end{aligned}$ | $\pm 6$ | 8 | $\begin{aligned} & \pm 12 \\ & 12.5 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| INPUT CHARACTERISTICS <br> Input impedance ${ }^{1}$ Input level required for tracking | $\mathrm{f}_{\mathrm{O}}=50 \mathrm{kHz}, \pm 10 \%$ <br> frequency deviation | $\begin{gathered} 7 \\ 10 \end{gathered}$ | $\begin{gathered} 10 \\ 1 \end{gathered}$ |  | $\begin{gathered} 5 \\ 10 \end{gathered}$ | $\begin{gathered} 10 \\ 1 \end{gathered}$ |  | $\begin{gathered} \mathrm{k} \Omega \\ \mathrm{mVrms} \end{gathered}$ |
| VCO CHARACTERISTICS <br> Center frequency Maximum value Distribution² | $\begin{gathered} C_{1}=2.7 \mathrm{pF} \\ \text { Distribution taken about } \\ \mathrm{f}_{\mathrm{O}}=50 \mathrm{kHz}, \mathrm{R}_{1}=5.0 \mathrm{k} \Omega, \mathrm{C}_{1}=1200 \mathrm{pF} \end{gathered}$ | $\begin{aligned} & 300 \\ & -10 \end{aligned}$ | $\begin{gathered} 500 \\ 0 \\ \hline \end{gathered}$ | +10 | -30 | $\begin{gathered} 500 \\ 0 \end{gathered}$ | +30 | $\begin{gathered} \mathrm{kHz} \\ \% \end{gathered}$ |
| Drift with temperature Drift with supply voltage | $\begin{gathered} \mathrm{f}_{\mathrm{O}}=50 \mathrm{kHz} \\ \mathrm{f}_{\mathrm{o}}=50 \mathrm{kHz}, \mathrm{VCC}_{\mathrm{cc}}= \pm 6 \text { to } \pm 7 \text { volts } \end{gathered}$ |  | $\begin{array}{r} 200 \\ 0.1 \\ \hline \end{array}$ | $\begin{array}{r} 525 \\ 1.0 \\ \hline \end{array}$ |  | $\begin{gathered} 300 \\ 0.2 \end{gathered}$ | 1.5 | $\begin{gathered} \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \end{gathered}$ |
| Triangle wave Output voltage level Amplitude Linearity |  | 1.9 | $\begin{gathered} 0 \\ 2.4 \\ 0.2 \\ \hline \end{gathered}$ | 3 | 1.9 | $\begin{gathered} 0 \\ 2.4 \\ 0.5 \end{gathered}$ | 3 | $\begin{gathered} \text { V } \\ \text { Vp-p } \\ \% \\ \hline \end{gathered}$ |
| Square wave <br> Logical "1" output voltage Logical "0" output voltage | $\begin{aligned} f_{0} & =50 \mathrm{kHz} \\ \mathrm{f}_{\mathrm{O}} & =50 \mathrm{kHz} \end{aligned}$ | +4.9 | $\begin{aligned} & +5.2 \\ & -0.2 \end{aligned}$ | +0.2 | +4.9 | $\begin{aligned} & +5.2 \\ & -0.2 \end{aligned}$ | +0.2 | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Duty cycle | $\mathrm{fo}_{0}=50 \mathrm{kHz}$ | 45 | 50 | 55 | 40 | 50 | 60 | \% |
| Rise time Fall time |  |  | $\begin{aligned} & 20 \\ & 50 \end{aligned}$ | $\begin{aligned} & 100 \\ & 200 \end{aligned}$ |  | $\begin{aligned} & 20 \\ & 50 \end{aligned}$ |  | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ |
| Output current (sink) <br> Output current (source) |  | $\begin{gathered} 0.6 \\ 5 \end{gathered}$ | $\begin{gathered} 1 \\ 10 \end{gathered}$ |  | $\begin{gathered} 0.6 \\ 5 \\ \hline \end{gathered}$ | $\begin{gathered} 1 \\ 10 \end{gathered}$ |  | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| DEMODULATED OUTPUT CHARACTERISTICS <br> Output voltage level <br> Maximum voltage swing ${ }^{3}$ <br> Output voltage swing <br> Total harmonic distortion <br> Output impedance ${ }^{4}$ <br> Offset voltage (V6-V7) <br> Offset voltage vs temperature (drift) <br> AM rejection | Measured at pin 7 <br> $\pm 10 \%$ frequency deviation | 4.25 <br> 250 <br> 30 | $\begin{gathered} 4.5 \\ 2 \\ 300 \\ 0.2 \\ 3.6 \\ 30 \\ 50 \\ 40 \end{gathered}$ | $4.75$ <br> 0.75 <br> 100 | $\begin{array}{r} 4.0 \\ 200 \end{array}$ | $\begin{gathered} 4.5 \\ 2 \\ 300 \\ 0.4 \\ 3.6 \\ 50 \\ 100 \\ 40 \end{gathered}$ | 5.0 <br> 1.5 <br> 200 | $\begin{gathered} \mathrm{V} \\ \mathrm{Vp}-\mathrm{p} \\ \mathrm{mVp}-\mathrm{p} \\ \% \\ \mathrm{k} \Omega \\ \mathrm{mV} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \mathrm{~dB} \end{gathered}$ |

NOTES

1. Both input terminals (pins 2 and 3 ) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between $2 \mathrm{k} \Omega$ and $20 \mathrm{k} \Omega$.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

## TYPICAL PERFORMANCE CHARACTERISTICS

## POWER SUPPLY CURRENT <br> AS A FUNCTION OF SUPPLY VOLTAGE



LOCK RANGE AS A FUNCTION OF gain setting resistance (PIN 6-7)


## DESIGN FORMULAS

## (See Figure 1)

Free-running frequency of $V C O$ : $f_{0} \simeq \frac{1.2}{4 R_{1} C_{1}}$ in Hz
Lock-range: $f_{L}= \pm \frac{8 f_{o}}{V_{C C}}$ in Hz
Capture-range: $\mathrm{fc} \simeq \pm \frac{1}{2 \pi} \sqrt{\frac{2 \pi \mathrm{f}_{\mathrm{L}}}{\tau}}$
where $\tau=(3.6 \times 103) \mathrm{X} \mathrm{C}_{2}$

## TYPICAL APPLICATIONS <br> FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically $\pm 60 \%$ ) with very high linearity (typically, within 0.5\%).
A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by
$\mathrm{f}_{\mathrm{o}}=\frac{1.2}{4 \mathrm{R}_{1} \mathrm{C}_{1}}$ and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7 , the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be
decreased with little change in the freerunning frequency. In this manner the lock range can be decreased from $\pm 60 \%$ of $f_{o}$ to approximately $\pm 20 \%$ of $f_{0}$ (at $\pm 6 \mathrm{~V}$ ).

A small capacitor (typically $0.001 \mu \mathrm{~F}$ ) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.


Figure 1

## Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the " 0 " and " 1 " states (commonly called space and mark) of the binary data signal.
A simple scheme using the 565 to receive FSK signals of 1070 Hz and 1270 Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.
The loop filter capacitor C 2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150 Hz ) and twice the input frequency (approximately 2200 Hz ). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with $\mathrm{fiN}_{\mathrm{I}}=1070 \mathrm{~Hz}$.
The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600ohm input impedance).

## Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.
The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be

a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.
A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The freerunning frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency ( $f(\mathbb{N})$ as long as the loop is in lock.

## SCA (Background Music) Decoder

 Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commerical use. To do this a frequency modulated subcarrier of 67 kHz is used. The frequency is chosen soas not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only $10 \%$ of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.
A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3 ). The demodulated (multiplex) FM signal is fed to the input through a two-stage highpass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80 mV and 300 mV , is required at the input. Its source should have an impedance of less than 10,000 ohms.
The Phase Locked Loop is tuned to 67 kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.
The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50 mV and the frequency response extends to 7 kHz .


## DESCRIPTION

The SE/NE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

## FEATURES

- Wide range of operating voltage (up to 24 volts)
- High linearity of modulation
- Highly stable center frequency (200 ppm/ ${ }^{\circ} \mathbf{C}$ typical)
- Highly linear triangle wave output
- Frequency programming by means of a resistor or capacitor, voltage or current
- Frequency adjustable over 10 to 1 range with same capacitor


## APPLICATIONS

- Tone generators
- Frequency shift keying
- FM modulators
- Clock generators
- Signal generators
- Function generators


## BLOCK DIAGRAM



## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :--- | :---: | :---: |
| Maximum operating voltage | 26 | V |
| Input voltage | 3 | $\mathrm{VP}_{\mathrm{P}} \mathrm{P}$ |
| Storage temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature range | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| NE566 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| SE566 | 300 | mW |

PIN CONFIGURATIONS


ELECTRICAL CHARACTERISTICS $T_{A}=25^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ unless otherwise specified.

| PARAMETER | SE566 |  |  | NE566 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min | Typ | Max | Min | Typ | Max |  |
| GENERAL <br> Operating temperature range <br> Operating supply voltage Operating supply current | -55 | 7 | $\begin{gathered} 125 \\ 24 \\ 12.5 \end{gathered}$ | 0 | 7 | $\begin{gathered} 70 \\ 24 \\ 12.5 \end{gathered}$ | $\begin{gathered} { }^{\circ} \mathrm{C} \\ \mathrm{~V} \\ \mathrm{~mA} \end{gathered}$ |
| $\mathrm{VCO}^{1}$ <br> Maximum operating frequency <br> Frequency drift with temperature Frequency drift with supply voltage <br> Control terminal input impedance ${ }^{2}$ FM distortion ( $\pm 10 \%$ deviation) <br> Maximum sweep rate Sweep range |  | $\begin{gathered} 1 \\ 200 \\ 1 \\ 1 \\ 0.2 \\ 1 \\ 10: 1 \end{gathered}$ | 0.75 |  | $\begin{gathered} 1 \\ 300 \\ 2 \\ 1 \\ 0.4 \\ 1 \\ 10: 1 \end{gathered}$ | 1.5 | $\begin{gathered} \mathrm{MHz} \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \\ \mathrm{M} \Omega \\ \% \\ \mathrm{MHz} \end{gathered}$ |
| OUTPUT <br> Triangle wave output Impedance <br> Voltage Linearity <br> Square wave input Impedance <br> Voltage <br> Duty Cycle <br> Rise time Fall Time | 1.9 <br> 5 <br> 45 | $\begin{aligned} & 50 \\ & 2.4 \\ & 0.2 \\ & 50 \\ & 5.4 \\ & 50 \\ & 20 \\ & 50 \end{aligned}$ | 55 | 1.9 $\begin{gathered} 5 \\ 40 \end{gathered}$ | $\begin{array}{r} 50 \\ 2.4 \\ 0.5 \\ \\ 50 \\ 5.4 \\ 50 \\ 20 \\ 50 \end{array}$ | 60 | $\begin{gathered} \Omega \\ \mathrm{Vpp} \\ \% \\ \\ \Omega \\ \text { Vpp } \\ \% \\ \text { ns } \\ \text { ns } \end{gathered}$ |

NOTES

1. The external resistance for frequency adjustment $\left(R_{1}\right)$ must have a value between $2 \mathrm{k} \Omega$ and $20 \mathrm{~K} \Omega$.
2. The bias voltage $\left(V_{c}\right)$ applied to the control terminal ( $\operatorname{pin} 5$ ) should be in the range $3 / 4 \mathrm{~V}^{+} \leq \mathrm{V}_{\mathrm{c}} \leq \mathrm{V}^{+}$.

## TYPICAL PERFORMANCE CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE


FREQUENCY AS A FUNCTION OF CAPACITANCE (C1)


VCO OUTPUT WAVEFORMS


## OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1 MHz . A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage ( $\mathrm{V}_{C}$ ) in the range

$$
3 / 4 \mathrm{~V}^{+} \leq \mathrm{V}_{\mathrm{c}} \leq \mathrm{V}^{+}
$$

where $V_{c c}$ is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with $R_{2}$ and $R_{3}$. The modulating signal is then ac coupled with
the capacitor $\mathrm{C}_{2}$. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$
f_{0} \simeq \frac{2\left[\left(V^{+}\right)-\left(V_{C}\right)\right]}{R_{1} C_{1} V^{+}}
$$

and $R_{1}$ should be in the range $2 k \Omega<R_{1}<$ $20 \mathrm{k} \Omega$.

A small capacitor (typically $0.001 \mu f$ ) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.
If the VCO is to be used to drive standard
logic circuitry, it may be desirable to use a dual supply of $\pm 5$ volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T2L gates, which require a current sink of more than 1 mA , it is usually necessary to connect a $5 k \Omega$ resistor between pin 3 and negative supply. This increases the current sinking capability to 2 mA . The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T2L circuitry which requires a fast fall time ( $<50 \mathrm{~ns}$ ) and a large current sinking capability.


FIGURE 1


FIGURE 2

## DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

FEATURES

- Wide frequency range $(.01 \mathrm{~Hz}$ to 500 kHz$)$
- High stability of center frequency
- Independently controllable bandwidth (up to 14 percent)
- High out-band signal and noise rejection
- Logic-compatible output with 100 mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20 to 1 range with an external resistor
- Military processing available


## APPLICATIONS

- Touch Tone ${ }^{\circledR}$ decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

BLOCK DIAGRAM


## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
| :---: | :---: | :---: |
| Operating temperature |  |  |
| NE567 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| SE567 | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating voltage | 10 | V |
| Positive voltage at input | $0.5+\mathrm{Vs}$ | V |
| Negative voltage at input | -10 | Vdc |
| Output voltage (collector | 15 | ${ }^{\circ}$ |
| of output transistor) | -65 to +150 | mW |
| Storage temperature | 300 |  |

PIN CONFIGURATIONS



DC ELECTRICAL CHARACTERISTICS ( $\mathrm{V}+=5.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.)

| PARAMETER | TEST CONDITIONS | SE567 |  |  | NE567 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| CENTER FREQUENCY1 <br> Highest center frequency ( $f_{0}$ ) <br> Center frequency stability2 <br> Center frequency shift with supply voltage | $\begin{gathered} -55 \text { to }+125^{\circ} \mathrm{C} \\ 0 \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{fo}_{\mathrm{o}}=100 \mathrm{kHz} \\ \hline \end{gathered}$ | 100 | $\begin{array}{\|c\|} 500 \\ 35 \pm 140 \\ 35 \pm 60 \\ 0.5 \\ \hline \end{array}$ | 1 | 100 | $\begin{array}{\|c\|} \hline 500 \\ 35 \pm 140 \\ 35 \pm 60 \\ 0.7 \\ \hline \end{array}$ | 2 | $\begin{gathered} \mathrm{kHz} \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \% / \mathrm{V} \\ \hline \end{gathered}$ |
| DETECTION BANDWIDTH <br> Largest detection bandwidth Largest detection bandwidth skew Largest detection bandwidthvariation with temperature Largest detection bandwidthvariation with supply voltage | $\begin{aligned} \mathrm{f}_{\mathrm{o}} & =100 \mathrm{kHz} \\ \mathrm{v}_{\mathrm{i}} & =300 \mathrm{mVrms} \\ \mathrm{v}_{\mathrm{i}} & =300 \mathrm{mVrms} \end{aligned}$ | 12 | $\begin{gathered} 14 \\ 1 \\ \pm 0.1 \\ \pm 2 \end{gathered}$ | $\begin{gathered} 16 \\ 2 \end{gathered}$ | 10 | $\begin{gathered} 14 \\ 2 \\ \pm 0.1 \\ \pm 2 \end{gathered}$ | $\begin{gathered} 18 \\ 3 \end{gathered}$ | $\%$ of $f_{0}$ $\%$ of $f_{0}$ $\% /{ }^{\circ} \mathrm{C}$ \%/V |
| INPUT <br> Input resistance <br> Smallest detectable input voltage ( $\mathrm{V}_{\mathrm{i}}$ ) Largest no-output input voltage <br> Greatest simultaneous outband signal to inband signal ratio Minimum input signal to wideband noise ratio | $\begin{aligned} & \mathrm{I}_{\mathrm{L}}=100 \mathrm{~mA}, \mathrm{f}_{\mathrm{i}}=\mathrm{f}_{0} \\ & \mathrm{I}_{\mathrm{L}}=100 \mathrm{~mA}, \mathrm{f}_{\mathrm{i}}=\mathrm{f}_{0} \end{aligned}$ $B_{n}=140 \mathrm{kHz}$ | 10 | $\begin{aligned} & 20 \\ & 20 \\ & 15 \\ & +6 \\ & -6 \end{aligned}$ | 25 | 10 | $\begin{aligned} & 20 \\ & 20 \\ & 15 \\ & +6 \\ & -6 \end{aligned}$ | 25 | $k \Omega$ <br> mVrms mVrms dB dB |
| OUTPUT <br> Fastest on-off cycling rate <br> "1" output leakage current <br> "0" output voltage <br> Output fall time ${ }^{3}$ <br> Output rise time ${ }^{3}$ | $\begin{gathered} \mathrm{IL}_{\mathrm{L}}=30 \mathrm{~mA} \\ \mathrm{~L}_{\mathrm{L}}=100 \mathrm{~mA} \\ R_{\mathrm{L}}=50 \Omega \\ \mathrm{R}_{\mathrm{L}}=50 \Omega \end{gathered}$ |  | $f_{0} / 20$ 0.01 0.2 0.6 30 150 | $\begin{aligned} & 25 \\ & 0.4 \\ & 1.0 \end{aligned}$ |  | $\begin{gathered} \mathrm{f}_{\mathrm{o}} / 20 \\ 0.01 \\ 0.2 \\ 0.6 \\ 30 \\ 150 \\ \hline \end{gathered}$ | $\begin{aligned} & 25 \\ & 0.4 \\ & 1.0 \end{aligned}$ | $\begin{gathered} A \\ \mathrm{~V} \\ \mathrm{~V} \\ \mathrm{~ns} \\ \mathrm{~ns} \end{gathered}$ |
| GENERAL <br> Operating voltage range <br> Supply current quiescent Supply current-activated <br> Quiescent power dissipation | $\mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$ | 4.75 | $\begin{gathered} 6 \\ 11 \\ 30 \end{gathered}$ | $\begin{gathered} 9.0 \\ 8 \\ 13 \end{gathered}$ | 4.75 | $\begin{gathered} 7 \\ 12 \\ 35 \end{gathered}$ | 9.0 10 15 | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \\ \mathrm{~mA} \\ \mathrm{~mW} \end{gathered}$ |

## notes

1. Frequency determining resistor $R_{1}$ should be between 1 and $20 \mathrm{k} \Omega$.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback $R_{L}$ network selected to eliminate pulsing during turn-on and turn-off.

## TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS
(Cont'd)


## DESIGN FORMULAS

$\mathrm{f}_{0} \simeq \frac{1.1}{\mathrm{R}_{1} \mathrm{C}_{1}}$
$B W \simeq 1070 \sqrt{\frac{V_{1}}{f_{0} C_{2}}}$ in $\%$ of $f_{0}, V_{i} \leq 200 \mathrm{mVrms}$

## Where

$V_{i}=$ Input Voltage (Vrms)
$\mathrm{C}_{2}=$ Low-Pass Filter Capacitor ( $\mu \mathrm{F}$ )

## PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (fo)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

## Detection Bandwidth (BW)

The frequency range, centered about $\mathrm{f}_{\mathrm{o}}$, within which an input signal above the threshold voltage (typically 20 mVrms ) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

## Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

## Detection Band Skew

A measure of how well the detection band is centered about the center frequency, $\mathrm{fo}_{0}$. The skew is defined as $\left(f_{\text {max }}+f_{\text {min }}-2 f_{0}\right) / 2 f_{o}$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

## OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567 . For most applications, the following three-step procedure will be sufficient for choosing the external components $R_{1}, C_{1}, C_{2}$ and $C_{3}$.

1. Select $R_{1}$ and $C_{1}$ for the desired center frequency. For best temperature stability, $\mathrm{R}_{1}$ should be between 2 K and 20 K ohm, and the combined temperature coefficient of the $\mathrm{R}_{1} \mathrm{C}_{1}$ product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low pass capacitor, $\mathrm{C}_{2}$, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of $\mathrm{f}_{\mathrm{o}} \mathrm{C}_{2}$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and $\mathrm{C}_{2}$ may be adjusted accordingly. For example, con-

## TYPICAL RESPONSE



Response to 100 mVrms tone burst. $R_{L}=100$ ohms.


Response to same input tone burst with wideband noise.

$$
\begin{array}{ll}
\frac{S}{N}=-6 \mathrm{db} & R_{\mathrm{L}}=100 \text { ohms } \\
& \text { Noise Bandwidth }=140 \mathrm{~Hz} \\
\hline
\end{array}
$$

stant bandwidth operation requires that input amplitude be above 200 mVrms . The bandwidth, as noted on the graph, is then controlled solely by the $f_{0} C_{2}$ product ( $f_{0}$ $(\mathrm{Hz}), \mathrm{C}_{2}(\mu \mathrm{fd})$ ).
3. The value of $C_{3}$ is generally non-critical. $\mathrm{C}_{3}$ sets the band edge of a low pass filter which attenuates frequencies outside the detection band to elminate spurious outputs. If $\mathrm{C}_{3}$ is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If $\mathrm{C}_{3}$ is too large, turn-on and turn-off of the output stage will be delayed until the voltage on $\mathrm{C}_{3}$ passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to translent frequencies.) A typical minimum value for $\mathrm{C}_{3}$ is $2 \mathrm{C}_{2}$.

AVAILABLE OUTPUTS (Figure 2)
The primary output is the uncommitted output transistor collector, pin 8 . When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6 V ) at full output current $(100 \mathrm{~mA})$. The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to $1.05 \mathrm{f}_{0}$ with a slope of about 20 mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave


Figure 1
output of magnitude $\left(+\mathrm{V}-2 \mathrm{~V}_{\text {be }}\right) \approx(+\mathrm{V}-1.4 \mathrm{~V})$ having a dc average of $+V / 2$. $A 1 \mathrm{k} \Omega$ load may be driven from pin 5 . Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of $+V / 2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

## OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200 mV ) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_{0} / 3, f_{0} / 5$, etc.
2. The 567 will lock onto signals near $(2 n+$ 1) $f_{o}$, and will give an output for signals near $(4 n+1) f_{0}$ where $n=0,1,2$, etc. Thus, signals at $5 f_{o}$ and $9 f_{o}$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and outband signals is afforded in the low input level (below 200 mVrms ) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lockup time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a $0.01 \mu \mathrm{~F}$ or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and
unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

## SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when $\mathrm{C}_{2}$ is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.
The following expressions give the values of $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$ which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $\mathrm{f}_{\mathrm{o}} / 10$ baud.

$$
\begin{aligned}
& \mathrm{C}_{2}=\frac{130}{\mathrm{f}_{\mathrm{o}}} \mu \mathrm{~F} \\
& \mathrm{C}_{3}=\frac{260}{\mathrm{f}_{\mathrm{o}}} \mu \mathrm{~F}
\end{aligned}
$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent $\mathrm{C}_{3}$ voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

## OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is


Figure 2


Figure 3
taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same
temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmiter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

## SENSITIVITY ADJUSTMENT

(Figure 3)
When operated as a very narrow band detector (less than 8 percent), both $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$ are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals ( 10 mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$ are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

## CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when $\mathrm{C}_{3}$ is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making $\mathrm{C}_{3}$ large, the feedback circuit will enable faster operation of the 567 by allowing $\mathrm{C}_{3}$ to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

## DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

## (Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the


Figure 5
circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since $R_{B}$ also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

## ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)
Although a large value of $C_{2}$ will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger
value of $\mathrm{C}_{2}$ be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of $R_{B}$ and $R_{C}$ can be eliminated and the $R_{A}$ resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

## OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

## REDUCTION OF C1 VALUE

(Figure 8)
For precision very low-frequency applications, where the value of $C_{1}$ becomes large, an overall cost savings may be achieved by inserting a voltage follower between the $\mathrm{R}_{1}$ $C_{1}$ junction and pin 6, so as to allow a higher value of $R_{1}$ and a lower value of $C_{1}$ for a given frequency.

## PROGRAMMING

To change the center frequency, the value of $R_{1}$ can be changed with a mechanical or solid state switch, or additional $\mathrm{C}_{1}$ capacitors may be added by grounding them through saturating npn transistors.
$\frac{130}{f_{0}}\left(\frac{10 K+R}{R}\right)<C_{2}<\frac{1300}{f_{0}}\left(\frac{10 K+R}{R}\right)$
NOTE

Adjust control for symmetry of detection band edges about $f_{0}$.

Figure 6

TYPICAL APPLICATIONS



PRECISION VLF


Figure 8

TYPICAL APPLICATIONS
(Cont'd)

| CARRIER-CURRENT REMOTE CONTROL OR INTERCOM |
| :---: |
|  |



24\% BANDWIDTH TONE DECODER


## TYPICAL APPLICATIONS (Cont'd)



NOTE
Application information available on request.

## sECTION 17 new products

## HIGH SLEW RATE OPERATIONAL AMPLIFIER

## DESCRIPTION

The NE/SE530 and NE/SE5530 are new generation high slew rate operational amplifiers featuring 3 MHz bandwidths and improved input parameters. The 530 is a single amplifier while the 5530 is a dual configuration. Both products will have industry standard pinouts.

## FEATURES

- Output swing ( $\pm 5 \mathrm{v}$ supplies) 8 volts $\mathrm{p}-\mathrm{p}$ typical
- High slew rate $35 \mathrm{~V} / \mu \mathrm{s} @$ unity gain inverting typical
- Settling time (to 0.1\%) $1 \mu \mathrm{~s}$ typical
- Low offset voltage $2 m$ Vmax
- Low bias current 60nAmax
- Wide bandwidth 3 MHz typical
- Low current drain 2mA typical/amplifier

PIN CONFIGURATIONS (530)



PIN CONFIGURATIONS (5530)


## DESCRIPTION

The NE586 and 587 are latch/decoder/drivers for 7 -segment LED displays. Both devices have constant current outputs, the NE586 being a fixed $25 \mathrm{~mA} /$ segment drive capability, and the NE587, variable between 5 and $50 \mathrm{~mA} /$ segment. On the NE587 the current is set with a single external resistor. The data (BCD) inputs and $\overline{\mathrm{LE}}$ (latch enable) function are low loading so that the devices are compatible with any data bus system.

PIN CONFIGURATION


## DESCRIPTION

The NE590/NE591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 darlington power outputs, each capable of 250 mA load current. The outputs are turned on or off by respectively loading a logic " 1 " or logic " 0 " into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{C E}$ input line which also serves the function of further address decoding. A common clear input, CLR, turns all outputs off when a logic " 0 " is applied.

The NE590 has 8 open collector darlington outputs which sink current to ground. The device is packaged in a 16 pin molded or cerdip package.

The NE591 has 8 open emitter darlington outputs which source current to an external load from a common collector line, $\mathrm{V}_{\mathrm{s}}$. The $V_{S}$ line need not necessarily be the same as the 5 volt Vcc supply. The device is packaged in an 18 pin molded or cerdip package.

## FEATURES

- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 9334.


## APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver


## PIN CONFIGURATIONS



## DESCRIPTION

The NE5030 is an 8-bit A-to-D converter employing the triple-slope technique of conversion. The device includes a voltage reference and clock generator and so constitutes the total conversion system with a minimum of components. Conversion time is approximately 10 mS ; voltage requirement is a single 5 V supply and the data outputs are tri-state bus compatible.

PIN CONFIGURATION


## applications

## sECTION 18 AnAlOG IC PROCESSING

## INTRODUCTION

Integrated circuits are divided into three general categories: (1) linear, (2) digital, and (3) MOS. Distinctly different design and process techniques are used for each type. The main difference between linear processes and other IC processes is their diversity. While digital circuits are commonly restricted to low voltage switching, linear circuits may be fabricated with anything from switching to linear characteristics, high or low voltages, high or low frequency, or any combination of these properties. To cope with this range of applications, the following processes are frequently used:
Epitaxial - 0.25 ohm-cm gold doped and non-gold doped 0.5 ohm-cm gold doped 1.0 ohm-cm Schottky and nonSchottky
2.5 ohm-cm
5.0 ohm-cm

Dielectric- 2 to 15 ohm-cm
All epitaxial processes are similar. The main difference is the resistivity of the deposited epitaxial layer in which the components are formed. This provides the means of selecting higher breakdown voltages or lower saturations by merely selecting an epitaxial resistivity.

For instance, the 5 ohm-cm process is used for operational amplifiers and regulators because it gives the 50 V LV ceo transistor breakdowns required. Since the phase lock loops need only 20 V , and lower saturation voltages are desirable, the 2.5 ohm-cm process is used for their fabrication.


Figure 1-1a



Transistor breakdown is not the only consideration in choosing a process. In products where fast switching is required, either the gold doped or Schottky processes are used. Gold doping is used where medium and high current operation is involved. Schottky technology is desired where lower currents or high transistor breakdowns are needed in addition to speed. Dielectric isolation is used where breakdown voltages must be in excess of 50 volts.

## COMPONENTS

The components commonly formed in linear integrated circuits by junction isolation are drawn in cross section in Figure 1-1. Parasitic components are also shown in the equivalent schematics. These parasitics can occasionally cause "sneak" paths or fault conditions in the circuit.

## TRANSISTORS

It is instructive to compare, in a general manner, discrete transistors with those manufactured in integrated circuits. The most important differences for npn transistors are the parasitic substrate transistor and the top contact collector, as seen in Figure 1-2.

The magnitude of the parasitic pnp beta depends upon the process and geometry used, but it ranges from about five for highresistivity processes to very much less than one for gold doped processes. The parasitic pnp only becomes active when the npn transistor goes into saturation. Normally such effects are not important, but in some circuit configurations latching effects may be observed. That is, a positive feedback path may be established which is selfsustaining. Alternately, or perhaps coincidentally, this path may cause high currents to flow. These potential problems are easily avoided with judicious layout procedures.

The effect of the top contact is to increase the saturation resistance. In small signal devices this is not significant, but at higher currents (around $50 . \mathrm{mA}$ ) this becomes an economic factor as the die arc must be increased and yields drop. This resistance is lowered by means of the $\mathrm{N}+$ buried layer seen in the cross sections of Figure 1-1.

The normal npn transistor beta for linear devices ranges up to 250. Occasionally "super beta" transistors are needed with betas as high as 2000. The processing steps involved are the same as for regular transistors except for a longer emitter diffusion time which gives a very narrow base width and high beta. Care must be exercised in this sequence to make super beta and regular npn devices at the same time.


The pnp transistors in monolithic form, both lateral and vertical, differ from discrete pnps. The names 'lateral' and 'vertical' are derived from the mode of transistor action that occurs in the two components. Referring to Figure $1-1 B$ it can be seen that current flows laterally from emitter to collector through the N-epitaxial area. The presence of the buried layer diffusion reduces to a comparatively low level, the collection by the isolation area. It is not eliminated entirely, however, which gives
rise to the parasitic diode shown in Figure 1-3.

The vertical pnp is similarly constructed but in this case the buried layer diffusion is omitted resulting in the isolation diffusion acting as the collector. The vertical current flow in this device gives rise to its name.
Frequency response is the primary difference between these devices. The lateral pnp is restricted to frequencies below 1 to 2 MHz while the vertical pnp upper range is around


## NPN TRANSISTOR PARASITIC COMPONENTS



Figure 1-2

## LATERAL PNP WITH PARASITIC DIODE



Figure 1-3

## MULTIPLE COLLECTOR PNP TRANSISTOR



Figure 1-4

10 to 20 MHz . Another important feature of the lateral pnp is its comparatively low beta range and the low current at which beta peaks. In addition, the lateral pnp collector can be split to give multiple collector devices as shown in Figure 1-4.

This configuration can be used to give fairly precise values of beta by tying one of the collectors to the base. Figure 1-5 illustrates the tie back method used.

Recent process development allows the addition of Schottky barrier devices to monolithic design (see Figure 1-6). The advantage is very fast switching circuits without gold doping. With this technique, the properties of non-gold doped devices are main-
tained while switching speeds are greatly improved. This is very desirable in devices containing both analog and digital circuitry such as voltage comparators.

## RESISTORS

Resistors can be made from any of the norp type layers. In practice the base and emitter diffusions are generally used. At times the "epilayer" (the bulk material) in the dielectric isolation process is also used. The required characteristics of the resistor determine the material or processes used. The most commonly used is the base diffused resistor. Size is scaled for the value desired. Base pinch resistors are used where high values are required and the limitations of accuracy and breakdown are not a problem.

LATERAL PNP WITH COLLECTOR TIE-BACK


Figure 1-5

Emitter resistors are useful where low value, temperature insensitive resistors are needed. This diffusion is also often used as a "cross-under," that is, a low resistance connecting path. This can simplify layout design considerably.

A new development in resistors that will offer great flexibility in design is the use of ion implantation. With this technique, resistivities orders of magnitude higher and temperature coefficients orders of magnitude lower than base diffused resistors are possible. We can expect to see this technology used extensively in high voltage circuits, low power circuits and in complex linear functions where die areas would otherwise be excessive.

## JUNCTION FIELD EFFECT TRANSISTORS

The n-channel FET is fabricated in the epitaxial layers and is obtained by pinchingoff the epi with isolation diffusion. Because of this construction, the nomenclature FET is something of a misnomer since the gate is not available as an input. Its usefulness is as a bias circuit starting element. It is much smaller in area than an equivalent value resistor and has a sufficiently high breakdown voltage for this purpose.

The $p$-channel FET is a more useful general purpose device. Its most important limitation is the breakdown voltage which is restricted to about 5 volts. Processing of both field effect and super beta transistors is similar. Changes in the regular process flows is necessary for both devices.

## CAPACITORS

Capacitors are made by using the capacitance associated with the various junctions or by forming a thin silicon dioxide layer between two plates. The plates are formed by alumirum metalization and low resistivity emitter diffusion.
A number of problems are associated with junction capacitors. They have low breakdowns for reasonable capacitance per unit area, the capacitors formed are polarized,
SCHOTTKY DIODE
and they have high leakage currents. Oxide capacitors are free from these problems but the capacitance per unit area is comparatively low. Junction capacitors are used primarily where decoupling capacitors are needed, while oxide capacitors are used where high quality is needed.

## OTHER DEVICES

There are a number of other components such as SCR, SCS and Zener diodes that are available coincidentally with the components discussed above. The Zener diodes available are the emitter base junction and the emitter-isolation junction. Other junctions have breakdowns that are high and variable so they are seldom used.


## OXIDE CAPACITOR CONSTRUCTION



Figure 1-7

## sECTION 19 AnAlOG IC DESIGn TECHIOUES

## INTRODUCTION

The components available for linear ICs were reviewed in Section 1. From that discussion it was clear that many differences exist between IC components and those available to discrete circuit design. These differences may be conveniently summarized as:
A. Limited resistor accuracy and values
B. Lack of integrated inductance
C. Small integrated capacitance values
D. Poor PNP transistor performance
E. Limited power dissipation

On the other hand, linear IC designs have the advantages of excellent component matching, both active and passive; and the accessibility of a great number of active components.

To cope with the limitations of monolithic circuitry, designers have evolved special techniques and practices, a number of which are detailed in this section.

## BIAS CIRCUITRY

In discrete designs the bias circuitry is accomplished by high value resistor networks. In linear designs this is impractical because of the die area required. The alternative is to use an n-channel FET as shown in Figure 2-1.

## SIMPLE BIAS CIRCUIT



Figure 2-1

Zener $V_{z}$ is fed current by FET Q1. The required bias voltage is then developed by the resistor divider R1 and R2. This simple technique can be elaborated upon if temperature compensation is required. By adding transistor Q2 shown in Figure 2-2, the positive temperature coefficient of the zener diode is offset by the negative one of the forward biased emitter-base diode.

More elaborate schemes, which include the maintenance of constant currents in the

TEMPERATURE COMPENSATED BIAS NETWORK


Figure 2-2
diodes, buffering the load from the source, and adjusting the composite temperature coefficient to zero, are commonly found where accurate references are required.
Current sources as well as voltage sources can be easily obtained using similar circuitry. Both npn and pnp type current sources are depicted by Figure 2-3.

## NPN AND PNP CURRENT SOURCES



Figure 2-3

Assuming Q1-Q2 and Q4-Q5 are well matched and of the same geometries it can be shown that :
$I_{N P N}=\frac{V_{B}-V_{B E}}{R 2}$ and IPNP $=\left[\frac{V_{B}-V_{B E}}{R 1}\right] \begin{aligned} & R 3 \\ & R 4\end{aligned}$
These equations demonstrate that the circuit currents can be made independent of external supply voltages and temperature fluctuations. Circuits such as these are used extensively in modern operational amplifiers such as the 531 and 536, where their
presence assures that such parameters as voltage gain and offset voltage remain constant with temperature and supply voltage variations.

The preceding circuits are valuable for high and medium values of current. Low current values are better developed by the popular circuit of Figure 2-4.

LOW VALUE CURRENT SOURCE


Figure 2-4

If the geometries of Q1 and Q2 are identical, the following equations hold:

$$
\begin{aligned}
& V_{B E 1}=V_{B E 2}+I_{N} R \\
& V_{B E 1}=\frac{k T}{q} \ln \left(\frac{I_{B}}{I_{S}}\right) \\
& V_{B E 2}=\frac{k T}{q} \ln \left(\frac{I_{N}}{I_{S}}\right) \\
& I_{N} R=\frac{k T}{q} \ln \left(\frac{I_{B}}{I_{N}}\right)
\end{aligned}
$$

Where the subscripts refer to their respective transistors, beta is high, and other symbols have their standard meaning.

This is a transcendental equation which is represented graphically by Figure 2-5.


Figure 2-5

As can be seen, it becomes possible to obtain very low currents with reasonable values of resistance. This circuit is used in the 592 where $\mathrm{I}_{\text {bias }}$ is set by a single resistor and the valve of the operating power supplies.

This principle may be extended to provide a particularly useful voltage reference. The circuit of Figure 2-6 illustrates how this is done.

## NON ZENER VOLTAGE REFERENCE



Figure 2-6

From the same considerations as before, the reference voltage can be shown to be:

$$
V_{\text {Ref }}=K_{2} \frac{k T}{q} I_{n} K_{1}
$$

There are a number of interesting and useful properties of this circuit. Compared with a Zener reference, it is much less noisy and can be used at lower supply voltages. With judicious circuit implementation, the voltage can be controlled to about $\pm 10 \%$ and low temperature coefficients can be achieved.

## CURRENT SOURCE LOADS

Using current sources for load resistors is another technique exploited in linear integrated circuit designs. The schematics of Figure 2-7 show how this may be done. The circuit shown is the simple differential amplifier. Figure 2-7a gives a conventional circuit while Figure 2-7b is an I.C. implementation using pnp current sources.

The value of the current source as a collector load lies in its equivalancy of an extremely high resistance while occupying a very small die area. High stage gains are thus obtained in a minimum of space. Other advantages of the current source include linearity of gain versus output swing (because gain is independent of current), and large output swing capabilities. The active load circuit also has the feature of summing the gain from both output sides. The disad-

vantages of the circuit in Figure 2-7b are that the noise in the pnp's is summed into the npn input noise, and the self-biasing scheme used in Figure 2-7b can introduce some added offset current if the pnp betas are low because pnps run at different current levels. A change in the circuit which avoids this problem is shown in Figure 2-8.

## IMPROVED DIFFERENTIAL AMPLIFIER



Figure 2-8

The current imbalance between Q1 and Q2 is now only:

$$
\mathrm{I}_{\mathrm{B}_{3}}=\frac{2 \mathrm{I}_{\mathrm{C}_{1}}}{\beta_{1} \beta_{3}}
$$

Where $I_{B 3}$ is Q3 base current $I_{C_{1}}$ is Q1 collector current and $\beta_{1}$ and $\beta_{3}$ are betas of Q1 and Q3 respectively. This imbalance is now negligible. Resistors have also been added to the
pnp emitters to increase the output impedance and, therefore, the gain.

Use of the pnp as a collector load can be extended by using multiple collector pnps as indicated in Figure 2-9.


This circuit could give a voltage gain of many millions, which for linear amplification would be generally impractical due to clipping. A practical realization would incorporate feedback to define gain, as shown in Figure 2-10, where the voltage gain is given by the ratio:

$$
A v=\frac{R_{F}}{R_{E}}
$$

## LEVEL SHIFTING

The necessity for level shifting arises from two general requirements:
A. Level interfacing from input to output
B. Maintaining voltages across transistor collector-base junctions to avoid clipping.

The latter situation can be seen in the circuit of Figure 2-10, where the voltage across Q1 is limited to a $V_{B E}$ minus an IR drop which limits the voltage swing at the output. Discrete designers overcome this problem with a liberal use of coupling and decoupling capacitators which are not available to linear I.C. designers, unless incorporated externally.

## AMPLIFIER STAGE WITH FIXED GAIN



Figure 2-10

Resistive level shifting is one method used in integrated circuitry. Figure 2-11 illustrates the actual and equivalent networks.

The DC voltage is level shifted down from point $A$ to point $B$ through resistor R1 by the current of Q2. The circuit AC performance can be analyzed by the equivalent circuit of Figure 2-11b with the gain of the circuit being given by:

$$
A_{1}=\frac{Z_{2}}{Z_{1} Z_{2}}
$$

Where

$$
Z_{1}=\frac{R 1}{1+j \omega R 1 C 1} \text { and } Z 2=\frac{R 2}{1+j \omega R 2 C 2}
$$

Maximum gain and broad bandwidth are dependent upon the following relationships:

R2 >> R1 and C1 >>C2
These conditions can generally be met since the output can be fed into an emitter follower with high input resistance and low input capacitance. R2 and C2 values would be in the 5 megohm and 0.5 pF range respectively. These values place workable values of R1 and C1 at 10-20Kohms and 1530 pF respectively. Lower values of R1 consume excessive current while lower values of C 1 degrade the 50 MHz frequency performance.


The disadvantages of this circuit include:
A. Large die area for R1 and C1
B. Limited voltage range
C. Power consumption without gain

A level shifter which overcomes these problems is the zener diode. A reverse biased transistor emitter base junction, giving a voltage drop of 6 to 7 volts, is commonly used for the zener since the voltage is in the range generally required.

## ZENER DIODE LEVEL SHIFTING



Figure 2-12

Multiples of this value can be gained by cascading more diodes. The benefits of this method are speed and small die area, while disadvantages include inflexibility to power supplies and high noise. These drawbacks restrict the use of this method to switching circuits such as comparators and sense amplifiers.

A combination of these two methods provides a circuit which provides a variable level shift. The zener of Figure 2-13 produces a constant voltage drop which is modified by resistors R1 and R2. Input to output voltage is given by:

$$
v=\left(1+\frac{R 1}{R 2}\right)\left(V_{2}=V_{B E}\right)
$$

VARIABLE LEVEL SHIFT


Figure 2-13

The most universally used level shifting technique however, uses the pnp transistor. The circuit of Figure 2-10 has been redrawn to include pnp level shifters in Figure 2-14.

LEVEL SHIFT WITH PNP TRANSISTORS


Figure 2-14

Transistors Q3 and Q4 are current source loads as described earlier. With the addition of Q2 the level shifting has been accomplished across the gain stage itself. The primary advantages are a large voltage range and power supply insensitivity. Voltage ranges up to the breakdown of the transistor are available with the additional advantage of voltage gain for the current consumed. Although not a problem in audio and low frequency systems, the disadvantage of the pnp level shifter is lack of frequency response above 1 MHz .

## OUTPUT STAGES

The design techniques for driven stages used in linear integrated circuits differ little from those of conventional designs. In cases where the power required is small, the conventional class $A$ emitter follower is generally used as shown in Figure 2-15a.
The integrated form may vary in that $R_{E}$ is generally replaced by a current source in the interest of smaller die size.
Where both sink and source drive capabilities are required, the nnp-pnp arrangement is used. As shown in Figure 2-16a driver Q1 feeds output transistors Q2 and Q3.

Diodes D1 and D2 are used to bias the output transistors into slight quiescent conduction. Temperature variations make current control difficult with this method and thermal runaway can result. The circuit of Figure 2-16b is much better from this standpoint since the current through Q4 and, therefore, the voltage across Q4 and Q5 can be controlled fairly well. By adjusting the value of R2 the current flowing through Q2 and Q3 is likewise controlled. A further advantage of this scheme is that Q4, Q5 and


Figure 2-16a


R2 can be placed in the same isolation tub.
An alternative to the use of the vertical pnp is the compound npn-pnp circuit of Figure 2-17. Keeping in mind the poor frequency and phase response of the lateral pnp, the loop formed from Q3 and Q6 has the potential danger of instability, however.


Transistor Biasing
Figure 2-16b

## OUTPUT PROTECTION

Output stages are commonly protected so that the maximum current available does not damage the device. A circuit achieving this is shown in Figure 2-18.
As the output current increases the voltage drop across R1 rises sufficiently to turn on Q1, which in turn removes some base drive from Q3. The output current is thus limited to the value specified by the IR drop of R1. Currents in the negative direction are likewise limited by R2 and Q2 acting upon Q4.


COMPLEMENTARY OUTPUT STAGE WITH SHORT CIRCUIT PROTECTION


Figure 2-18

Often times the current handled by Q4 is large. If this is the case, the base drive at Q4 must be large to overcome low beta in the pnp. Hence Q2 must handle large currents to effect output protection. For this reason negative current limiting is often installed at earlier stages of a design so that smaller Q2 collector currents are required to control the output.

## REACTIVE COMPONENT SIMULATION

Earlier in this chapter component limitations of linear IC design were discussed. These limitations restricted the values of resistance and capacitance in addition to the non existence of the inductor for linear design. Techniques circumventing the resistor limitations, such as current source loads, have been covered. Methods of multiplying capacitance and simulating inductance have also been developed for use in linear IC design.

In both cases the general method is to incorporate the oxide capacitors available into an active feedback configuration to synthesize the desired impedance.
Capacitive multiplication is done using the circuit of Figure 2-19. The effective capacitance is given by the relationship:

$$
C_{e f f}=C\left(\frac{R 1}{R 3}\right)
$$

Values of resistance for R1 should be as high as possible since the impedance appears in series with the effective capacitance.

## CAPACITANCE MULTIPLIER



Figure 2-19

Virtual inductors can be synthesized from active devices as well. With a constant current excitation, the voltage dropped across an inductance increases with frequency. Thus an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 2-20 yields such a response with the effective inductance being equal to:


The $Q$ of this inductance depends upon R1 being equal to R2. At this point the Q of the inductor is maximum. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of oscillation at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

## LAYOUT CONSIDERATIONS

Of paramount importance to the layout of a linear circuit is the chip size. Every possible effort is made to reduce chip size for economic reasons.

In general, the transition of a circuit design to a layout of its monolithic form is by way of design rules which give the minimum and maximum spacing between oxide openings of both the same and other diffusions. These rules take into account various process parameters and tolerances. Besides these general rules there are some particular considerations.
First is optimization of matching between similar components. This is accomplished by placing components as close as possible so that the differences due to micro-
variations are minimized. In the case of transistors this means placing them in adjacent isolation tubs. For resistors this means running them parallel with identical numbers of corners and with identical endcontacts.

Another consideration is component matching in the presence of thermal transients. This is a common problem with operational amplifiers where thermal transients of the output transistors can reflect back to the input transistors. A layout that could exhibit this effect is shown in Figure 2-21.

As the output drives the load the power dissipation from output transistors Q3 and Q4 cause thermal gradients across the die. Transistors Q1 and Q2 receive a thermally generated voltage difference of 2 mV per degree centigrade. Since operational amplifiers such as the 531 have voltage gains in excess of 100 dB , the voltage need only be $20-200 \mu \mathrm{~V}$ to produce output saturation.

The layout example of Figure 2-21 would generate large offset voltages as well as make accurate gain measurements impossible. The modifications required to eliminate temperature variations have been illustrated in Figure 2-22. Here the power dissipating elements are situated on the die center line. All temperature sensitive elements, such as Q1 and Q2, are placed symmetrically about the center line.

CHIP LAYOUT WITH THERMAL SYMMETRY


Figure 2-22

## POOR THERMAL LAYOUT



Figure 2-21

Die layout is also important with respect to ground current feedback. A good example occurs when both digital and linear circuitry appear on the same chip, as with sense amplifiers.

A functional block diagram of the sense amplifier with parasitic resistances R1 and R2 is shown in Figure 2-23. Resistors R1 and R2 represent the impedance of the die metalization.

## PARASITIC RESISTANCE IN GROUND LINES



Figure 2-23

When the TTL gate output switches large ground currents occur on the gate ground leads. This transient current flows through R1 and R2, raising the voltage at points $A$ and B . These potentials can cause positive (or negative) feedback which can alter the ideal transfer curve of Figure 2-24a to that of Figure 2-24b. Both discontinuities and hysteresis are evident.

The improved method of grounding is illustrated in Figure 2-25. Ground paths have been arranged so that currents sum only at the common ground pad of the die. In addition, ground metalization has been widened to reduce metal resistance.

As stated earlier, minimizing die area is important. One of the ways this can be done is by placing many components in a single isolation area. There are dangers in doing this however, due to the presence of parasitic components. To illustrate, the emitter follower circuit of Figure 2-26 will be used.

To save space both components are diffused in the same isolation tub as shown by Figure 2-27. The transistor collector contact serves the dual role of collector contact and reverse biasing of the resistor as required. Danger arises as the transistor current increases.

The voltage drop in the N -epi region becomes larger, eventually forward biasing part of the resistor. The circuit of Figure 228 applies should forward biasing occur, adding a parasitic pnp transistor between the resistor and the npn transistor base. If the beta is high enough a regenerative loop occurs causing latch up. The solution lies in


HYSTERESIS DUE TO GROUND CURRENTS


Figure 2-24b

## EMITTER FOLLOWER CIRCUIT



Figure 2-26


Figure 2-27
locating the resistor out of the transistor current path.

## Summary:

The preceding two chapters have been devoted to a basic treatise of linear design and processing techniques. Although severely limited in depth, the knowledge presented should provide a great deal of insight into understanding linear circuits, their capabilities and limitations.

EMITTER WITH PARASITIC PNP TRANSISTOR


Figure 2-28

## sECTION 20 OPERATIONAL AmpIIfIERS

## INTRODUCTION

The operational amplifier was first introduced in the early 1940's. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity this chapter will cover the basic op amp as it is defined along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

## THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 3-1.

## IDEAL OPERATIONAL AMPLIFIER



Figure 3-1

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common mode input signals.
Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

## THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. Input bias currents for instance are in the 5pA range for FET input amplifiers while offset voltages have been reduced to less than 1 mV in many cases.
Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak to peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage while output current is internally limited to approximately 25 mA . Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

## DEFINITION OF TERMS

Earlier the ideal operational amplifier was defined. No circuit is ideal of course so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored it would be beneficial to define those parameters commonly referenced.

## INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0 volts out for 0 volts input. But, since the practical case is not perfect, there will appear a small dc voltage at the output even though no differential voltage is applied. This dc voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 3-2.

An operational amplifier's performance is in large part dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage also which determines dc parameters such as offset voltage since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

## DIFFERENTIAL INPUT STAGE



Figure 3-2

$$
E_{O S}=I_{C} 2 R_{L}-I_{C} 1 R_{L}=0
$$

In practice small differences in geometries of the base emitter regions of Q1 and Q2 will cause Eos not to equal 0. Thus, for balance to be restored a small dc voltage must be added to one $\mathrm{V}_{\mathrm{BE}}$ or

$$
V_{O S}=V_{B E 1}-V_{B E} 2
$$

where the $V_{B E}$ of the transistor is found by

$$
V_{B E}=\frac{k T}{q} \ln \left(\frac{I_{E}}{I_{s}}\right)
$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is 'that differential dc voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of Vos. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

## INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is Vos drift with temperature. Present day amplifiers usually possess $V_{\text {O }}$ drift levels in the range of $5 \mu \mathrm{~V}$ to $40 \mu \mathrm{~V}$ per degree C . The magnitude of $V_{\text {OS }}$ drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per degree $C$ will be $3.3 \mu \mathrm{~V}$ for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.


Figure 3-3

## INPUT BIAS CURRENT

Again referring to Figure 3-2, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a dc current path to ground in order for the input to function. Input bias current, then is the dc current required by the inputs of the amplifier to properly drive the first stage.'

The magnitude of $I_{b i a s}$ is calculated as the average of both currents flowing into the inputs and is calculated from

$$
I_{B}=\frac{I_{1}+I_{2}}{2}
$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

## INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little los as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to $l_{\text {os }}$ can be calculated by

$$
V_{\text {out }}=A_{\text {cl }}\left(l_{\mathrm{os}} R_{\mathrm{s}}\right)
$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

## INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current.

Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for los drift with values ranging in the $.5 n \mathrm{n}$ per degree $C$ area. Obviously those applications requiring low input offset currents also require low drift with temperature.

## INPUT IMPEDANCE

Differential and common mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other while common mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

## COMMON MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon both inputs which will not cause the output to misbehave is called the common mode range. Most amplifiers possess common mode ranges of $\pm 12$ volts with supplies of $\pm 15$ volts.

## COMMON MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common mode signals. The classic definition for common mode rejection ratio of an amplifier is the ratio the differential signal gain to the common mode signal gain expressed in dB as shown in equation 3-6a.

$$
C M R R(d B)=20 \log \frac{e_{o} / e_{i}}{e_{o} / e_{c m}}
$$

The measurement CMRR as in 3-6a requires 2 sets of measurements. However note that if $e_{o}$ in equation $3-6 a$ is held constant, CMRR becomes:

$$
\operatorname{CMRR}(\mathrm{dB})=20 \log \frac{e_{\mathrm{cm}}}{e_{\mathrm{i}}} / e_{\mathrm{o}}=\mathrm{K}
$$

A new alternate definition of CMRR based on $3-6 \mathrm{~b}$ is the ratio of the change of input

offset voltage to the input common made voltage change producing it.

Figure 3-4 illustrates the application of the equivalent common mode error generator to the voltage follower circuit. The gain of the voltage follower with error contributions caused by both finite gain and finite common mode rejection ratio is shown in equation 3-7.

$$
\frac{e_{0}}{e_{\text {in }}}=\frac{1 \pm 1 / \text { CMRR }}{1+1 / \mathrm{A}}
$$

## AC PARAMETERS

Parameter definition has up to this point, been dealing primarily with dc quantities of voltages, currents, etc. Several important ac or frequency dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open loop gain with low frequency gains in excess of 100 dB . The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open loop gain the cascading of stages results in the need for frequency compensation in closed loop configurations and reduces the open loop.

## LARGE SIGNAL BANDWIDTH

The large signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$
\mathrm{FPL}_{\mathrm{PL}}=\frac{\text { Slew Rate }}{2 \pi \cdot \mathrm{E}_{\text {out }}}
$$

where FPL is the upper power bandwidth frequency and Eout is the peak output swing of the amplifier.

## SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed a slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease
frequency response. In general, the worst case slew rate is in the unity gain noninverting mode. Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

## AMPLIFIER SLEW RATE LIMITATIONS



Figure 3-5a


Figure 3-5b

## FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each and every gain stage. Monolithic pnp transistors used for level shifting possess poor upper frequency characteristics and cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 3-6 the open loop frequency response of most op amps crosses unity gain at 10 MHz . Closed loop response is unstable without compensation however, so typical unity gain frequencies are readjusted to approximately 1 MHz by the effects of phase compensation.

From Figure 3-6 it is also apparent that an amplifier has a trade off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade off is a constant figure called the gain bandwidth product.

## TEST METHODS

Product testing of all integrated circuits is

## OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



Figure 3-6
very rapid using state of the art automatic test equipment. Large computer controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

A typical simplified op amp test configura-
tion is depicted by Figure 3-9. Units may be classed in several categories according to selected parameters. Even failures may be classified categorically depending upon their mode of failure.

Figures 3-7, 3-8, 3-10, and 3-11 illustrate the general test set ups commonly used to measure CMRR, average bias current, offset voltage and current and open loop gain respectively. In general the following parameters are tested under the following conditions.

## COMMON MODE REJECTION

The test set-up for CMRR is given in Figure 3-7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

The positive common mode input voltage within the range $\mathrm{V}_{\mathrm{CM}}$ is algebraically subtracted from all supply voltages and from $V_{0}$. Then $V_{1}$ is measured. The most negative common mode voltge within the range, $V_{\text {CM2 }}$, is then subtracted from all the supply voltages and $V_{0}$, and $V_{1}$ is again measured. Then
$\mathrm{CMRR}=(\mathrm{R} 1+\mathrm{R} 2) / \mathrm{R} 1 \mid\left(\mathrm{V}_{\mathrm{CM} 1}-\mathrm{V}_{\mathrm{CM}}\right) / \mathrm{V}_{11}-\mathrm{V}_{12}$

CIRCUIT DIAGRAM USED FOR CMRR MEASUREMENT


Figure 3-7

## CIRCUIT DIAGRAM USED FOR <br> AVERAGE BIAS CURRENT MEASUREMENT



Figure 3-8


CIRCUIT DIAGRAM USED FOR OFFSET VOLTAGE AND OFFSET CURRENT


All resistor values are in ohms.
Figure 3-10


Figure 3-11

This operation is equivalent to swinging both inputs over the full common mode range, and holding the output voltage constant, but it makes the $V_{1}$ measurement much simpler.

## BIAS CURRENT

Bias current is measured in the configuration of Figure 3-8.

With switches at position 1 and $\mathrm{V}_{\mathrm{O}}=0$ volts, measure $\mathrm{V}_{1} 1$. Move switches to position 2 and again measure $V_{\mid 2}$. Calculate IBIAS (average), by

$$
\begin{aligned}
& I_{B 1}=\frac{R 1}{R 1+R 2}\left(\frac{V_{1}}{R 3}\right) \\
& I_{B 2}=\frac{R 1}{R 1+R 2}\left(\frac{V_{1}}{R 3}\right) \\
& I_{B 1 A S}(a v g)=\frac{I_{B 1}+I_{B 2}}{2}=\frac{R 1}{R 1+R 2} \frac{V_{11}-V_{B 2}}{2 R 3}
\end{aligned}
$$

## OFFSET VOLTAGE

Figure $3-10$ is used for both offset voltage and current. With $\mathrm{V}_{0}$ at 0 volts and the switches selecting the source impedance, the offset voltage is measured at $V_{I}$ and is equal to

$$
V_{\text {os }}=\frac{R 1 V_{1}}{R 1+R_{2}}
$$

## OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure $\mathrm{V}_{12}$. Calculate the contribution of los by

$$
\mathrm{I}_{\mathrm{os}}=\frac{\mathrm{V}_{12}-V_{11}}{R 3}
$$

## SIGNAL GAIN

The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 3-11. Usually specified under a specific load determined by $R_{L}$, a signal equal to the maximum swing of the output voltage is applied to $V_{o}$ in both positive and negative directions. $V_{11}$ and $V_{12}$ are measured values of $V_{1}$ and and $V_{0}=$ maximum positive and maximum negative signals respectively. The gain of the device under test then becomes

$$
A_{v o}=\left(\frac{R 1+R 2}{R 1}\right)\left(\frac{V_{01}-V_{02}}{V_{11}-V_{12}}\right)
$$

## SLEW RATE

Many other parameters are checked automatically by similar means. Only the most
important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.


Figure 3-12a


Figure 3-12 shows a typical bench set up for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, $\mathrm{V}_{\text {in }}$ must be less than absolute maximum input voltage and the wave form should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$
S_{R}=\frac{V_{\text {out }}}{T} \text { in volts } / \mu \mathrm{s}
$$

## OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Signetics linear devices.
Figure 3-13 shows the transfer characteristic of a typical linear device, the Signetics 531. Note that the unit saturates at approximately +12 and -12 volts and exhibits a linear transfer characteristic between -10
and +10 volts.
From the slope of this linear portion of the transfer characteristic, and from the point

TRANSFER CURVE OF 531


Figure 3-13a


Figure 3-13b
where it crosses the $e_{i n}$ axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (D.U.T.), is 50,000 and its input offset voltage is 1.0 mV .
A simple circuit to display the curves of Figure 3-13 on an oscilloscope is shown in Figure $3-14$. A $60 \mathrm{~Hz}, 44 \mathrm{Vp}-\mathrm{p}$ sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the D.U.T.
The output of the D.U.T. drives the vertical input of the scope. For providing $V+$ and $V-$ to the D.U.T., the tester uses two simple adjustable regulators, both current limited at 25 mA . Input drive to the D.U.T. may be selected by means of S-2 as shown.
To use the curve tracer, first preset the V+ and $V$-supplies with an accurate meter. The supply voltages are somewhat dependent on ac line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak D.U.T. input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 3-13 of course.

## CURVE TRACER SCHEMATIC



Figure 3-14

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

## AMPLIFIER DESIGN

Linear operational amplifier IC's were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three stage approach requiring both input and output stage compensation. In addition the output stage was not short circuit proof and the input stage latched up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these, (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage to current converter, with a small $g_{m}$ and the second stage a current to voltage converter with a high $r_{m}$, the second stage can be rolled off at 6 dB octave with a small value capacitor in the order of 30 pF , which can then be built into the device itself. This concept is shown in Figure 3-15.

The frequency and phase response of the pnp devices in the first stage dictate a roll off in the second stage to give a loop gain of unity at about 1.0 MHz . For the unity gain

feedback configuration, this implies an open loop gain of unity at this frequency. The capacitor $\mathrm{C}_{\mathrm{c}}$ controls this parameter by looking much smaller than $r_{m}$ at frequencies above a few cycles, giving a clean 6dB/octave roll off over 5 decades.
The overall gain at frequencies where the impedance of $\mathrm{C}_{\mathrm{c}}$ dominates $\mathrm{r}_{\mathrm{m}}$ is given by

$$
A_{v}(\omega)=\frac{q l_{s 1}}{4 \mathrm{KT}} \cdot \frac{1}{\omega C_{c}}
$$

Substituting the value given above, we find that a capacitance of $\mathrm{C}_{\mathrm{c}}=30 \mathrm{pF}$ gives a unity

SCHEMATIC OF 536


Figure 3-16
gain frequency of about 1.0 MHz .
First stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the $\mathrm{C}_{\mathrm{c}}$ by the expression

$$
S_{R}=\frac{d V}{d T}=\frac{I L S}{C_{C}}
$$

where ILs is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000 . Bias currents under 2 nA can be achieved in this way. Even
though the Buceo of such transistors can be as low as 1 volt, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

Further reduction in room temperature input bias current can be achieved by the use of FET input devices. A, (slightly simplified), schematic of the 536 FET input op amp is given in Figure 3-16.

The majority of the 741 circuitry is preserved with the appropriate input and bias structural changes made to incorporate the junction FETs. The biasing of Q1 and Q2 is chosen to minimize offset voltage and drift. The voltage across Q1 is controlled by Q28, Q32, and R8 which is the same as that across R6 via Q42 and Q43. The operating points of Q1 and Q2 are closely controlled by the IDss of Q42 via their respective current sources. Offset adjustment is accomplished by trimming the values of R1 and R2 externally to equalize the currents through Q1 and Q2. Figure 3-17 illustrates the technique required.
FET input structures of this type can provide input bias, (gate leakage), currents on the


All resistor values are in ohms.
Figure 3-17
order of 5pA at room temperature. However, unlike the input bias currents of bipolar devices, the input bias current changes rapidly with temperature, doubling in value for every $10^{\circ} \mathrm{C}$ rise in temperature. For high temperatures the bias current of FETs becomes only about 4 times lower than super beta structures.

The 536 offers the advantages of very high input impedance and higher slew rate. The increase in slew rates for the 536 is about 6 times that of a 741.

The second limitation of 101-741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal gm of the first stage as depicted by Figure $3-18$, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source 14 causes the first stage transfer function to change as shown in Figure 3-19. The compensation capacitor is returned to the output of the 531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large signal bandwidths with this input structure will be essentially the same as the small signal response. Full bandwidth possibilities of this configuration are still limited by the beta and $f_{t}$ of the lateral pnp devices used for collector loads in the first stage. Even so, the slew rate of the 531 and 538 is a factor of 40 better than general purpose devices.

## VOLTAGE/CURRENT CURVES OF FIRST STAGE



Figure 3-19

## BASIC FEEDBACK THEORY

At the beginning of this chapter the ideal op amp was defined. The ideal parameters are never fully realized but they present a very convenient method for the preliminary analysis of circuitry. So important are these ideal definitions that they are repeated here. The ideal amplifier possesses:

1. Infinite gain
2. Infinite input impedance
3. Infinite bandwidth
4. Zero output impedance


From these definitions two important theorems are developed:

1. No current flows into or out of the input terminals.
2. When negative feedback is applied the differential input voltage is reduced to zero.

Keeping these rules in mind, the basic concept of feedback can be explored.

## VOLTAGE FOLLOWER

Perhaps the most often used and simplest circuit is that of a voltage follower. The circuit of Figure 3-20 illustrates the simplicity.

## vOLTAGE FOLLOWER



Figure 3-20

Applying the zero differential input theorem the voltages of pins 2 and 3 are equal and since pins 2 and 6 are tied together, their voltage is equal; hence, $\mathrm{E}_{\text {out }}=\mathrm{E}_{\text {in }}$. Trivial to analyze, the circuit nevertheless does illustrate the power of the zero differential voltage theorem. Because the input impedance is multiplied and the output impedance divided by the loop gain the voltage follower is extremely useful for buffering
voltage sources and for impedance transformation.

## NON-INVERTING AMPLIFIER

Only slightly more complicated is the noninverting amplifier of Figure 3-21.

NON-INVERTING AMPLIFIER


Figure 3-21

The voltage appearing at the inverting input is defined by

$$
\mathrm{E} 2=\frac{\mathrm{E}_{\text {out }} \cdot \mathrm{R}_{\text {in }}}{R_{\mathrm{F}}+\mathrm{R}_{\text {in }}}
$$

Since the differential voltage is zero, $\mathrm{E} 2=$ E3, and the output voltage becomes

$$
E_{\text {out }}=E_{\text {s }}\left(1+\frac{R_{F}}{R_{\text {in }}}\right)
$$

It should be noted that as long as the gain of the closed loop is small compared to open loop gain, the output will be accurate, but as the closed loop gain approaches the open loop value more error will be introduced.

The signal source is shown in Figure 3-21 in
series with a resistor equal in size to the parallel combination of $R_{i n}$ and $R_{F}$. This is desirable because the voltage drops due to bias currents to the inputs are equal and cancel out even over temperature. Thus overall performance is much improved.

## INVERTING AMPLIFIER

By slightly rearranging the circuit of Figure $3-21$, the non-inverting amplifier is changed to an inverting amplifier. The circuit gain is found by applying both theorems; hence, the voltage at the inverting input is 0 and no current flows into the input. Thus the following relationships hold.

$$
\frac{E_{\text {in }}}{R_{\text {in }}}+\frac{E_{o}}{R_{F}}=0
$$

Solving for the output $E_{0}$

$$
E_{o}=-E_{\text {in }} \frac{R_{F}}{R_{\text {in }}}
$$

INVERTING AMPLIFIER


Figure 3-22

As opposed to the non-inverting circuits the input impedance of the inverting amplifier is not infinite but becomes essentially equal to $\mathrm{R}_{\text {in }}$. This circuit has found widespread acceptance because of the ease with which input impedance and gain can be controlled to advantage, as in the case of the summing amplifier.

## COMPENSATION

Present day operational amplifiers are comprised of multiple stages, each of which has a 3dB point or pole associated with it. Referring to Figure 3-23, the 3dB break points of a two stage amplifier are approximated by the Bode plot.
As with any feedback loop, the op amp must be protected from phase shifts in excess of $360^{\circ}$. A steady $180^{\circ}$ phase shift is developed by the amplifier from output to inverting input. In addition the sum of all additional shifts due to amplifier poles or feedback component poles will cause the necessary additional $180^{\circ}$ to sustain oscillation if the

FREQUENCY COMPENSATION


Figure 3-23
gain of the amplifier is greater than one for the frequency at which the $180^{\circ}$ phase shift is reached. By adding poles and zeros to the amplifier response externally, the phase shift can be controlled to insure stability.
Many op amps now include internal compensation. These are single capacitors of 30 pF typically and the amplifier will remain stable for all gains. However, since they are unconditionally stable, the compensation is larger than required for most applications. The resultant loss of bandwidth and slew rate may be acceptable in the general case but selection of an externally compensated device can add a great deal to the amplifier response if the compensation is handled properly.

In order to fully develop the point at which instability occurs a fuller understanding of phase response is necessary.
The diagram of Figure 3-24 depicts the phase shift of a single pole. Note that at the pole position the phase shift is $45^{\circ}$ and that phase shift becomes $0^{\circ}$ for a decade below the pole and $-90^{\circ}$ for a decade above the pole location. This is a Bode approximation which possesses a $5.7^{\circ}$ error at $0^{\circ}$ and $90^{\circ}$ but this error is usually considered small enough to be ignored. The single pole produces a maximum of $90^{\circ}$ phase shift and also produces a frequency roll off of 20 dB per decade. The addition of the second pole of Figure 3-25 produces an additional $90^{\circ}$ phase shift and increases the role off slope to -40 dB per decade.
At this point phase shift could exceed $180^{\circ}$ because unity gain is reached causing instability. For gain levels equal to A1 or $|1 / \beta|$, the phase shift is only $90^{\circ}$ and the amplifier is stable. However, the gain of A2 the phase shift is $180^{\circ}$ and the loop is unstable. Gains in between A1 and A2 are



Figure 3-25
marginally stable. However, as shown in Figure 3-26 the phase shift as it approaches $180^{\circ}$ causes increasing frequency peaking and overshoot until sustained oscillations occur.


Figure 3-26

It is generally accepted in the interest of minimized frequency peaking to limit the phase shift of the amplifier to $135^{\circ}$ or a phase margin of $45^{\circ}$. At this margin the second order response of the system is critically damped and oscillation is prevented.

Referring to Figure 3-27, the required compensation can be determined. Given the open loop response of the amplifier, the desired gain is plotted until it intercepts the open loop curve as shown.

## FREQUENCY COMPENSATION



Figure 3-27

The phase shift for minimum peaking is $135^{\circ}$. Remembering that phase shift is $45^{\circ}$ at the frequency pole the example of Figure $3-27$ will be unstable at gains less than 20 dB where phase shift exceeds $180^{\circ}$, and will possess excessive overshoot and ringing at gains less than 60 dB where phase shift exceeds $135^{\circ}$. Thus, the desired compensation will move the second pole of the amplifier out in frequency until the closed loop gain intersects the open loop response before the second break of the amplifier occurs. Selecting only enough compensa-
tion to do the job assures the maximum bandwidths and slew rates of the amplifier. Additional in-depth information on compensation can be found in the reference material.

## FEED FORWARD COMPENSATION

External compensation has been shown to improve amplifier bandwidth over internal compensation in the preceding section. Additional bandwidth can be realized if feed forward compensation is used. Bandwidth is limited in monolithic design by the poor frequency response of the pnp level shifters of the first stage.


Figure 3-28a

FREQUENCY RESPONSE WITH FEED FORWARD COMPENSATION


## FEED FORWARD COMPENSATION OF LM301



Figure 3-28C

The concept of feed forward compensation bypasses the input stage at high frequencies driving the higher frequency second stage directly as pictured by Figure 3-28a. The Bode plot of Figure 3-28b shows the additional response added by the feed forward technique used in Figure $3-28 \mathrm{c}$. The response of the original amplifier requires less compensation at lower frequencies allowing an order of magnitude improvement in bandwidth. The typical feed forward network for the LM301 is shown in Figure 328 c with its Bode plot in Figure 3-28b. Standard compensation and feed forward are both plotted to illustrate the bandwidth improvement. Unfortunately, the use of feed forward compensation is restricted to the inverting amplifier mode.

## REFERENCES

1. OPERATIONAL AMPLIFIERS-Design \& Applications, Jerald Graeme and Gene Tobey, McGraw Hill Book Company.

## APPLICATIONS

Volumes upon volumes have been written describing circuits based on the operational amplifier. Space prohibits a lengthy discussion of each application. Rather the following pages are intended as a reference point from which one can digress to achieve a specific response. The most important things to remember were brought out in the basic feedback theory section. No application of op amps need be terribly difficult if the summing point restraints are remembered and applied.

## VOLTAGE FOLLOWER

The basic configuration in Figure 3-29 has a gain of 1 with extremely high input impedance. Setting the feedback resistor equal to the source impedance will cancel the effects of bias current if desired.


Figure 3-29

However, for most applications a direct connection from output to input will suffice. Errors arise from offset voltage, common mode rejection ratio and gain. The circuit can be used with any op amp with the required unity gain compensation, if it is required.

## INVERTING AMPLIFIER

With the inverting amplifier of Figure 3-30 the gain can be set to any desired value defined by R2 divided by R1. Input impedance is defined by the value of R1, and R3 should equal the parallel combination of R1 and R2 to cancel the effect of bias current. Offset voltage, offset current, and gain contribute most of the errors. The ground may be set anywhere within the common mode range and any op amp will provide satisfactory response.

## NON-INVERTING AMPLIFIER

Gain for the non-inverting amplifier is defined by the sum of R1 and R2 divided by R1.

The amplifier does not phase invert and possesses high input impedance. Again the impedances of the two inputs should be equal to reduce offsets due to bias currents.


Figure 3-30

NON-INVERTING AMPLIFIER


Figure 3-31



## DIFFERENTIAL AMPLIFIER



Figure 3-33

## SUMMING AMPLIFIER



Figure 3-34

## CURRENT TO VOLTAGE CONVERTER

The transfer function of the current to voltage converter is

$$
V_{\text {out }}=R 1 l_{\text {in }}
$$

Evaluation of the circuit depends upon the virtual ground theorem developed earlier. The current flowing into the input must be the same as that flowing across R1, hence, the output voltage is the IR drop of R1.

Limitations of course are output saturation voltage and output current capability. The inputs may be biased anywhere within the common mode range.

## DIFFERENTIAL AMPLIFIER

This circuit of Figure $3-33$ has a gain with respect to differential signals of R2/R1.

The common mode rejection is dominated by the accuracy of the resistors. Other errors arise from the offset voltage, input offset current, gain and common mode rejection. The circuit can be used with any op amp discussed in this chapter with the proper compensation.

## SUMMING AMPLIFIER

The summing amplifier is a variation of the inverting amplifier. The output is the sum of the input voltages, each being weighed by$\mathrm{R}_{\mathrm{F}} / \mathrm{R}_{\mathrm{in}}$.

The value of R4 may be chosen to cancel the effects of bias current and is selected equal
to the parallel combination of RF and all the input resistors.

## INTEGRATOR

Integration can be performed with a variation of the inverting amplifier by replacing the feedback resistor with a capacitance. The transfer function is defined by

$$
V_{\text {out }}=-\frac{1}{R C} \int_{0}^{t} V_{\text {in }} \cdot d t
$$

The gain of the circuit falls at 6 dB per octave over the range in which strays and leakages are small.


Since the gain at dc is very high a method for resetting initial conditions is necessary. Switch S1 removes the charge on the capacitor. A relay of FET may be used in the practical circuit. Bias and offset currents and offset voltage should be low in such an application.

## DIFFERENTIATOR

The differentiator of Figure 3-36 is another variation of the inverting amplifier. The gain increases at 6 dB per octave until it intersects the amplifier open loop gain, then decreases because of the amplifier bandwidth. This characteristic can lead to instability and high frequency noise sensitivity.


A more practical circuit is shown in Figure $3-37$. The gain has been reduced by R3 and the high frequency gain reduced by C 2 allowing better phase control and less high frequency noise. Compensation should be for unity gain.

## PRACTICAL DIFFERENTIATOR



Figure 3-37

## AUDIO CIRCUITS

Many audio circuits involve carefully tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 3-38. Operational amplifiers are well suited to these applications because of their high gain and easily tailored frequency response.

## RIAA PREAMP

The preamplifier for phono equalization is shown in Figure 3-39, along with the theoretical and actual circuit response.


Figure 3-38a


Figure 3-38b


Figure 3-38c



Low frequency boost is provided by the inductance of the magnetic cartridge with the RC network providing the necessary break points to approximate the theoretical RIAA curve.

## RUMBLE FILTER

Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2 pole Butterworth approach and features switchable break points. With the circuit of Figure 3-40 any degree of filtering from fairly sharp to none at all is switch selectable.

## TONE CONTROL

Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones dependent upon listener preference. The

PREAMPLIFIER-RIAA/NAB COMPENSATION

-Select to provide specified transducer loading.
Output Noise $\equiv 0.8 \mathrm{mV} \mathrm{rms}$ (with input shorted) All resistor values are in ohms.

Figure 3-39a


Bode Plot of RIAA Equalization and the
response realized in an actual circuit using
response realized in an actual circuit using
the 531 .
Figure 3-39b


Bode Plot of NAB Equalization and the
response realized in the actual circuit response realized in the actual circuit using
the 531 .

Figure 3-39c


Figure 3-40


All resistor values are in ohms.
NOTES

1. Amplifier A may be a 531 or 301 . Frequency compensation, as for unity gain noninverting amplifiers, must be used.
2. Turn-over frequency -1 kHz .
3. Bass boost +20 dB at 20 Hz , bass cut -20 dB at 20 Hz , treble boost +19 dB at 20 kHz , treble cut -19 dB at 20 kHz .


Figure 3-41

## BALANCE AMPLIFIER WITH LOUDNESS

 CONTROL

All resistor values are in ohms.
Figure 3-42
circuit of Figure 3-41 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

## BALANCE AND LOUDNESS AMPLIFIER

Figure 3-42 shows a combination of balance and loudness controls. Due to the nonlinearity of the human hearing system the low frequencies must be boosted at low listening levels. Balance, level and loudness controls provide all the listening controls to produce the desired music response.

## VOLTMETER

Figure $3-43$ shows a high impedance voltmeter, using the 536 op amp as a noninverting amplifier. The ranges, up to 10 V full scale, have extremely high input impedance, (up to $5 \times 10^{8} \Omega$ ), with a guard terminal available. The 30 V and 100 V scales have 30 and $100 \mathrm{M} \Omega$ input impedance. The input is protected against input overvoltage by the diodes, but the meter cannot be subjected to more than $50 \%$ overload.

## CAPACITANCE MULTIPLIER

The circuit in Figure 3-44 can be used to simulate large capacitances using small value components. With the values shown and $C=10 \mu F$, and effective capacitance of $10,000 \mu \mathrm{~F}$ was obtained. The Q available is limited by the effective series resistance. So R1 should be as large as practical.

## SIMULATED INDUCTOR

With a constant current exitation, the voltage dropped across an inductance increases with frequency. Thus, an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure $3-45$ yields such a response with the effective inductance being equal to:

$$
L=R 1 R 2 C
$$

The Q of this inductance depends upon R1 being equal to R2. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of instability at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

## POWER AMPLIFIER

For most applications, the available power from op amps is sufficient. There are times when more power handling capability is necessary. A simple power booster capable of driving moderate loads is offered in Figure 3-46.

The circuit as shown uses a 741 device. Other amplifiers may be substituted only if


Figure 3-43

R1 values are changed because of the ICC current required by the amplifier. R1 should be calculated from the expression

$$
\mathrm{R} 1=\frac{600 \mathrm{mV}}{1 \mathrm{CC}}
$$

## VOLTAGE-TO-CURRENT CONVERTERS

A simple voltage-to-current converter is shown in Figure 3-47 The current out is lout $\approx V_{\text {in }} / R$. For negative currents, a pnp can be used and for better accuracy, a Darlington pair can be substituted for the transistor. With careful design, this circuit can be used to control currents of many amps. Unity gain compensation is necessary.
The circuit in Figure 3-48 has a different input and will produce either polarity of output current. The main disadvantages are the error current flowing in R2, and the limited current available.

## ACTIVE CLAMP LIMITING AMPLIFIER

The modified inverting amplifier in Figure 349 uses an active clamp to limit the output swing with precision. Allowance must be made for the Vbe of the transistors. The
swing is limited by the base-emitter breakdown of the transistors. A simple circuit uses two back-to-back zener diodes across the feedback resistor, but tends to give less precise limiting and cannot be easily controlled.

## ABSOLUTE VALUE AMPLIFIER

The circuit in Figure 3-50 generates a positive output voltage for either polarity of input. For positive signals, it acts as an noninverting amplifier and for negative signals, as an inverting amplifier. The accuracy is poor for input voltages under 1 V , but for less stringent applications, it can be effective.

## HALF WAVE RECTIFIER

Figure 3-51 provides a circuit for accurate half wave rectification of the incoming signal. For positive signals, the gain is 0 , for negative signals, the gain is -1 . By reversing both diodes, the polarity can be inverted. This circuit provides an accurate output, but the output impedance differs for the two input polarities and buffering may be needed. The output must slew through two diode drops when the input polarity reverses. This limits the accuracy for 741 type devices above 300 Hz . The 535 device will

CAPACITANCE MULTIPLIER


All resistor values are in ohms.
Figure 3-44

VIRTUAL INDUCTOR


Figure 3-45
work up to 10 kHz with less than $5 \%$ distortion.

## PRECISION FULL WAVE RECTIFIER

The circuit in Figure 3-52 provides accurate full wave rectification. The output impedance is low for both input polarities, and the errors are small at all signal levels. Note that the output will not sink heavy currents, except a small amount through the $10 \mathrm{k} \Omega$ resistors. Therefore, the load applied should be referenced to ground or a negative voltage. Reversal of all diode polarities will reverse the polarity of the output. Since the outputs of the amplifiers must slew through two diode drops when the input polarity changes, 741 type devices give $5 \%$ distortion at about 300 Hz . The 535 device will give under 5\% distortion up to 10 kHz in this circuit.

## CYCLIC A TO D CONVERTER

One interesting, but, much ignored $A / D$ converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts $\mathrm{V}_{\text {ref }}$ from the input and doubles the remainder if the polarity


## VOLTAGE TO CURRENT CONVERTERS



Figure 3-47


Figure 3-48


Figure 3-49
was correct. In Figure 3-53 the signal is full wave rectified and the remainder of $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {ref }}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of $\mathrm{V}_{\text {ref. }}$. Possessing high potential accuracy, the circuit using 531 devices settles in $5 \mu \mathrm{~s}$.

## LOGARITHMIC AMPLIFIER

Converting an input voltage to its log equivalent is very useful in computational circuits since two inputs can be multiplied simply by adding their logarithms. The log transfer curve of a $V_{B E}$ junction is used in Figure 3-54 to achieve the transfer function. The 15.7 kohm resistor and 1 kohm thermistor provide a temperature compensated scale factor of 1 volt per decade of input voltage. Low input current devices such as the LF356 should be used for best results.

## TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 3-55 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of the op amp A-1 and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is

$$
f=\frac{1}{4 R C} \cdot \frac{R 2}{R 1}
$$

The square wave will maintain $50 \%$ duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the 531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The 5558 device can be used as well, except for the lower frequency response.

## TWO-PHASE SINE WAVE OSCILLATOR

This circuit uses a 2-pole pass Butterworth filter, followed by a phase shifting single pole stage, fed back through a voltage limiter to achieve sine and cosine outputs. The values shown using 741 amplifiers give about $1.5 \%$ distortion at the sine output and about $3 \%$ distortion at the cosine output. By careful trimming of $\mathrm{C}_{\mathrm{G}}$ and/or the limiting network, better distortion figures are possible. The component values shown give a frequency of oscillation of about 2 kHz . The values can be readily selected for other frequencies. The 531 should be used at higher frequencies to reduce distortion due to slew limiting.

Absolute value AMPLIFIER


Figure 3-50

HALF WAVE RECTIFIER


All resistor values are in ohms.
Figure 3-51

## PRECISION FULL WAVE RECTIFIER



Figure 3-52

## FAST SAMPLE AND HOLD CIRCUIT

This circuit, (referring to Figure 3-57), depends upon the high slew rate of the 531 . The operation begins as a strobe pulse developed from a logic input at IC2 turns on jFET Q1. This completes the feedback loop to IC1 and Q1 and Q2. This forces the capacitor C 1 to charge to a voltage equal to the input voltage plus the gate to source offest voltage of the MOS transistor Q2. At the end of the strobe time, the loop is broken and this voltage is held by capacitor C 1 until the time of the next strobe pulse. Using the MOSFET in this way minimizes greatly any drift or offset and results in a tracking accuracy of better than $.01 \%$. The 536 could be used as a buffer amplifier instead, with some loss of speed.

With the components shown, a $15 \mu$ s strobe pulse was used and the decay of the output voltage between samplings was measured at less than 1 mV per second.

## VOLTAGE COMPARATOR

Inexpensive voltage comparators with only modest parameters are often needed. The op amp is often used in this configuration because the high gain provides good selectivity. Figure $3-58$ shows a circuit usable with most any op amp. The zener is selected for the output voltage required (5.1 volt for TTL), and the resistor provides some current protection to the op amp output structure. $\mathrm{V}_{\text {ref }}$ can be any voltage within the wide common mode range of the amplifier-another advantage of using op amps for comparators. If the LM101A devices is used as depicted by Figure 3-59 the clamp diode may be connected to the compensation point directly. Clamping the voltage at this point does not require a series resistor because of the internal circuitry of the LM101A.

## VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times however, it becomes necessary to select a device not possessing external adjustments. Figures 360, 3-61, and 3-62 suggest some possible arrangements for offset voltage adjust and bias current nulling circuitry. The circuitry of Figure 3-62 provides sufficient current into the input to cancel the bias current requirement. Although more simplified arrangements are possible the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.

## CYCLIC A TO D CONVERTER



Figure 3-53a


Figure 3-53b


TWO-PHASE SINE WAVE OSCILLATOR


Figure 3-56


All resistor values are in ohms.
Figure 3-57

VOLTAGE COMPARATOR
UNIVERSAL OFFSET NULL
FOR INVERTING AMPLIFIERS

All resistor values are in ohms.
Figure 3-60

UNIVERSAL OFFSET NULL FOR NONINVERTING AMPLIFIERS


All resistor values are in ohms.

Figure 3-61


## THE LF 156, IMPROVED FET OP AMP

## Introduction

Advanced analog processing at Signetics has led to the improved jFET input op amp. The LF156 incorporates well-matched, high-voltage jFET's on the same chip with bipolar transistors. The design gives low voltage and current noise and a low $1 / \mathrm{f}$ noise corner. Specific applications which can utilize the advanced characteristics of the LF156 follow:

## Applications

A change in capacitance must cause a change in charge, and that charge is displaced into the summing point, which must be balanced by an equivalent displacement of charge across the feedback capacitor, $\mathrm{C}_{\mathrm{f}}$, caused in turn by a change in the output voltage e. This circuit has the desirable property of being virtually independent of shunt capacitance across the

input, since such capacitance is connected from the summing point to ground, and has across it only the residual null voltage, which should be negligibly low. This independence of input capacitance permits the use of long shielded cables between the transducer and the amp, without significantly affecting accuracy. Leakage resistance in parallel with $\mathrm{C}_{\mathrm{f}}$ must be deliberately sustained, in order to prevent the amplifier output from drifting to saturation. The sensitivity is inversely proportional to the value of $\mathrm{C}_{\mathrm{f}}$.

The smallest value of $\mathrm{C}_{\mathrm{f}}$ that will be large compared to "strays" will yield the highest predictable sensitivity. At the lowest frequency, Xc must be small compared to $R_{L}$ and the op amp's offset current is sufficiently small to prevent saturation with the required value of $R$.

Another application for which the LF156 is well suited is the high frequency, high impedance active filter. An example follows:


FREQUENCY RESPONSE



Other applications for the LF156 include: high impedance buffers, wideband low noise low drift amplifiers, precision high speed integrators, sample and hold circuits and fast $D / A$ and $A / D$ converters.

## SE/NE535, OP AMP APPLICATIONS

## Introduction

The 535 is a new generation monolithic op amp which features improved input characteristics. The device is compensated to unity gain and has a minimum guaranteed unity gain slew rate of $10 \mathrm{~V} / \mu \mathrm{s}$. This is achieved by employing a clamped super beta input stage which has lower input bias current.


## Applications

These improved parameters can be put to good use in applications such as sample and hold circuits which require low input current and in voltage follower circuits which require high slew rates. The circuit that follows will yield maximum small signal transient response and slew rate for the 535 at unity gain.

It is always good practice in designing a system to use dual tracking regulators such as the Signetics 5554 to power the dual supply op amps. This will guarantee the positive and negative supply voltage will be equal during power up. With the 535, it is possible to degrade the input circuit characteristics by not applying the power supplies simultaneously. The 535 is capable of directly replacing the 741 with higher input resistance which will improve such designed as active filters, sample and hold, as well as voltage followers.
The SE/NE535 can be used either with single or split power supplies.


## SE/NE538 APP. NOTE

## Introduction

The Signetics SE/NE538 is the undercompensated version of the SE/NE535. The 538 has a typical slew rate of $50 \mathrm{~V} / \mu \mathrm{s}$ and a gain bandwidth product of 6 MHz .

The internal frequency compensation is designed for a minimum inverting gain of 4 and a minimum non-inverting gain of 5 . Below these gains the 538 will be unstable and the 535 should be used.

The higher slew rate of the 538 has made this device quite appealing for high speed designs and the fact that it has a standard pinout will allow it to be used to upgrade existing sytems that now use the $\mu \mathrm{A} 741$ or $\mu \mathrm{A} 748$.

## Applications

OFFSET ADJUST CIRCUIT



NOTE:
Pins not shown are not connected. All resistor values are typical and in ohms.

## sECTION 21 VOITAGE REGULATORS

## INTRODUCTION

The wide use of integrated circuits in systems has frequently led to the power supply and regulator portions taking a disproportionate share of the volume of the system. The introduction of flexible, high performance regulator ICs such as the 550 has made it possible for a designer to produce a highly regulated power supply in a small space with greatly reduced design effort.

The objective of a voltage regulator is to provide a constant output voltage independent of input supply voltage, output load current, and temperature. In general, it is desirable that the regulator should limit its own dissipation and its output current so that fault conditions and overload will not damage the regulator or the load.

Supply regulators contain four basic elements: a reference source, an error detector, a control device, and protection circuitry. For the devices discussed here, the reference source is a constant voltage, the control device is a pass transistor, and the protection is primarily by current limiting.
Because the application of voltage regulators depends a great deal upon the internal workings of the integrated circuit, a brief discussion of the design is included before actual applications are presented.

A schematic of the 550 is present in Figure 4-1. For the sake of brevity this discussion will deal with the 550 but in most cases will apply also to the $\mu \mathrm{A} 723$ device.

## THE REFERENCE SOURCE

The 550 reference voltage is developed across the zener diode D2. The voltage is temperature compensated by the baseemitter drops in Q4, Q5 and Q6, in combination with the resistance divider R2-R6. The voltage appearing at the emitter of Q5 has a temperature coefficient of approximately $+7 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ while that at the base of Q6 is approximately $-2.3 \mathrm{mV} /{ }^{\circ} \mathrm{C}$. Thus, by choosing the appropriate tap on the resistor R2-R6, it is possible to obtain a zero temperature coeffient. Naturally, the actual value of the temperature coefficient will fluctuate from unit to unit, but accurate compensation is easier to achieve here than with other methods. The effective impedance at this point is predominantly the parallel impedance of R2 and R6, increased by the diode impedances, and is typically $2 k$ ohms.

The reference circuit as it stands is not self starting, necessitating the addition of FET Q1, D1, D4, and D5. When there is no current in D2, Q1 will feed current through D4 and D5 into the base of Q4, thus starting the
current sources. When these are operating, D1 drops approximately the same voltage as D2, so D5 has no voltage across it and it no longer affects the reference circuit. The current through Q1 drives the base of Q17, with D1 and D4 providing the correct bias point for the proper operation of Q4 and Q5.

## ERROR AMPLIFIER

The error amplifier in the 550 is a differential amplifier composed of Q11 and Q12, with biasing provided by Q7, Q8, Q9, Q10 and Q13. Q7 and Q8 act as equal current sources, driven by Q2, with R4 and R5 improving the balance and output impedance characteristics. The current from Q7 is inverted in Q10 and Q13. Q13 has twice the area of Q10, so the current sink Q13 is twice the value of the source Q7 and Q8. Q9 eliminnates the error term caused by the basic currents of Q12 and Q13. Thus, the sum of the emitter currents of Q4 and Q12 is twice the current in source Q8. In balance, the current flow into the base of Q14 can be neglected, so the collector current of Q12 is equal to the current from Q8. Ignoring the base current of Q12, the emitter current of Q12 is half the collector current of Q13, so Q11 must carry the remainder. Hence, the currents in Q11 and Q12 are equally matched at balance, or no error condition. An unbalanced condition where the base of

## 550 REGULATOR SCHEMATIC



Figure 4-1

BASIC REGULATOR CONFIGURATION


Figure 4-2a

## CURRENT LIMITING CURVES



Figure 4-2b

Q11 is more positive (negative) than that of Q12 will lead to an increase (decrease) of current in Q11, a decrease (increase) of current in Q12, and a rise (fall) of the voltage at the base of Q14 and Q15. Thus, a positive voltage change on the base of Q11 will lead to a higher current from Vout, the emitter of Q15. The effect of voltage changes on the base of Q12 is, of course, the opposite. The voltage gain of the error amplifier is given by
(Equation 4-1)

$$
A V \cong \frac{R C}{2_{r_{e}}}=\frac{\mathrm{R}_{\mathrm{C} 12} / / \mathrm{R}_{\mathrm{C}} 8}{2 \mathrm{kT} / \mathrm{q} \mathrm{l}_{\mathrm{E}}}
$$

This is typically 5000 at room temperature, rising a little at low temperature, and falling slightly at high temperature. High frequency stability is ensured by connecting a capacitor from the compensation pin to the inverting input, giving the amplifier a 6dB/octave roll off. In this manner, external pass elements with arbitrary phase characteristics at high frequency can still be compensated for by rolling off the amplifier.

The error voltage is derived by resistor division of the output voltage. Since the error amplifier inputs will seek a balance between them, the output voltage will attain a value equal to the reference voltage multiplied by the amplifier gain.

The collector voltage of Q12 is set by the nearly constant output voltage. Power supply rejection of the amplifier may be improved by taking the collector of Q11 to the constant voltage of Q14 also.

The availability of both the inverting and non-inverting inputs to the error amplifier allows the regulator to be used in a wide variety of applications.

In some applications where the output is fed back to the non-inverting input, a nondestructive latch-up can occur in Q11. By feeding current into the compensation pin through a diode this phenomenon can be avoided. Those applications requiring the additional diode are shown with the necessary connections.

## CONTROL DEVICE

The control element is formed by the pass transistor Darlington pair Q14-Q15. The ultimate current capability of this pair is very high, but the usable current is restricted by packaging and assembly limitations to about 200 mA . In general, power dissipation factors lead to more severe limitations, and applications requiring currents in excess of 50 mA are best handled with external pass transistors. To this end, the collector of Q15 is brought out separately, allowing an extended range of pass transistor connections to be utilized. These are discussed in the applications sections.

## PROTECTION CIRCUITRY

Up to this point the design discussions have applied both to the 550 and $\mu \mathrm{A} 723$ devices. The short circuit protection sections differ slightly. Therefore, the following discussion will not necessarily apply to the $\mu \mathrm{A} 723$.

Isolating the regulator from the load during periods of overload is the function of Q16 and Q18. These two transistors are arranged to form an SCS device.
Figure 4-2 shows the basic positive voltage regulator configuration. The sense resistor RSC is connected between emitter and base of Q16. When load current increases to such a value as to turn on Q16 the SCS device
turns on removing the $120 \mu \mathrm{~A}$ base drive provided by Q8 to Q14, thus isolating the load.
After the SCS turns on, Q16 need only provide the small base current required by Q18 to sustain current limiting. The current at which current limiting occurs is given by:
(Equation 4-2)

$$
\mathrm{Isc}=\frac{\mathrm{V}_{\text {sense }}}{\text { RSC }}
$$

where Isc is the short circuit current and $V_{\text {sense }}$ is the $V_{B E}$ of Q16.

Since the $V_{B E}$ of Q16 falls with increasing temperature the short circuit also falls, a desirable trait.

The advantage of incorporating the SCS device for current limiting lies in foldback limiting the output. That is, the output current under overload conditions drops to a value far below the peak load current capability. This is essential in high current regulators to protect the regulator from excessive power dissipation. The technique of foldback limiting and the resultant locus are illustrated by Figure 4-3. In normal operation of the circuit no current is sourced, but when shut down, a current
(Equation 4-3)

$$
\mathrm{I}_{\mathrm{CL}} \simeq \mathrm{I}_{\mathrm{QB}} \bullet \mathrm{~h}_{\mathrm{FEL}} /\left(1+\mathrm{h}_{\text {FEL }}\right)
$$

is sourced. Bypassing this current through a resistor RFB as in Figure 4-3, a portion, (IcLRFB), of the $V_{\text {sense }}$ shutdown voltage can be generated regardless of current in Rsc, once the device is shut down.

Thus, when Q16 - Q18 are conducting the major portion of IQ8, the shutdown condi-

## FOLD BACK CURRENT LIMITING



Figure 4-3a

FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT


Figure 4-3b
tion changes from equation 4-3 to, (ignoring small terms),
(Equation 4-4)

$$
\mathrm{ISCR}_{\mathrm{SC}}+\mathrm{I}_{\mathrm{CL}} \cdot \mathrm{R}_{\mathrm{FB}}=\mathrm{V}_{\text {sense }}
$$

Thus, the actual short circuit current can be much less than the peak load current given by equation 4-2. The load current-voltage characteristics of Figure 4-3 are shown in the curve for various values of RFB.

Since the input impedance of the $C_{L}$ terminal is negative over some range of voltages, it is normally necessary to by-pass RFB with a capacitor to maintain stability if operation in this range is desired. A value of $0.01 \mu \mathrm{~F}$ is generally satisfactory.
By increasing $R_{F B}$ to such a value that $R_{F B} \bullet$ ICL $>\mathrm{V}_{\text {sense }}$, the circuit will shut down completely under overload, and not come back into operation unless the voltage between the $C_{L}$ and $C_{S}$ terminals is reduced below $V_{\text {sense }}$ by some external means. In general, this is most useful in remote shutdown applications discussed later.

The final feature available in the dual in-line package versions of the 550 and the $\mu \mathrm{A} 723$ is the zener diode D3 between $V_{\text {out }}$ and $V_{Z}$, (the $V_{Z}$ output is not available in the $L$ package since there are insufficient pins). This diode is useful in certain applications such as negative regulators, where it is desirable for the output of the amplifier to be level shifted to a point more negative that $\mathrm{V}_{\text {out }}$ is permitted to go ( +2 V referred to $\mathrm{V}-$ ). The Zener voltage is typically 6.4 V . The use of this feature is discussed in the next section.

## APPLICATIONS

Designing basic voltage regulators with high performance IC regulators is relatively
straightforward. Each functional block of the regulator should be considered as to its contribution to the system. Basic regulation of an output voltage is achieved by multiplying a reference voltage by the gain of an amplifier. Thus, the error amplifier may be treated as an operational amplifier where the 'virtual ground' and 'zero differential voltage' statements developed in section three apply. The reference voltage is applied to the positive input and a sample of the output voltage is fed back to the negative input via a resistor divider network. Since the junction of R1 and R2 in Figure 4-3 will equal the reference voltage (zero differential rule), the output will be set by the ratio of the resistors. Specifically the output voltage becomes:
(Equation 4-5)

$$
V_{\text {OUT }}=V_{\text {REF }} \frac{R 1+R 2}{R 2}
$$

Each input to the error amplifier requires a small bias current of typically $1 \mu \mathrm{~A}$. Since these currents will be flowing through the input impedances to the amplifier it is possible to generate an error voltage if the impedances to the amplifier are not equal. In addition temperature changes will cause fluctuations in bias current causing the output voltage to drift. Thus, the final design should provide a match of the input impedances both to improve accuracy and temperature stability of the output voltage. The effective impedance of the internal reference voltage of the 550 is 2 kohm . Therefore for best temperature stability the parallel combination of R1 and R2 should be 2kohm.
(Equation 4-6)

$$
\mathrm{RS}_{\mathrm{S}}=2 \mathrm{k}=\frac{\mathrm{R} 1 \cdot \mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}
$$

The design of the regulator should satisfy both equation 4-5 and equation 4-6 simultaneously. Solving both leads to equations 4-7 and 4-8 which express the resistor values as a function of output voltage.
(Equation 4-7)

$$
\mathrm{R} 2=\frac{2000 \mathrm{~V}_{\text {OUT }}}{\mathrm{V}_{\text {OUT }}-V_{\text {REF }}} \mathrm{OHMS}
$$

(Equation 4-8)

$$
R 1=\frac{2000 V_{\text {OUT }}}{V_{\text {REF }}} O H M S
$$

Having determined the required resistor values, the designer may find that they are not readily available in standard values and some adjustments are necessary. Such changes should maintain the ratio:

$$
\frac{V_{\text {OUT }}}{V_{I N}}=\frac{R 1+R 2}{R 2}
$$

The reference voltage of the 550 is 1.63 volts typically, with a spread of 1.53 volts minimum to 1.73 volts maximum. This variation from unit to unit may require that some portion of R1 or R2 be made adjustable for exact output voltage trimming.

## PASS TRANSISTOR CIRCUITS

The next major subject concerns the use of external pass transistor options. These can readily extend the usable output current range of the regulator to many amps and reduce power dissipation in the IC as well. In this way, thermal effects, (discussed later in detail), are minimized.
The simplest circuit is that shown in Figure 4-4. Here, the internal Darlington pass transistor configuration is extended to a triplet by the external npn transistor. For further extension, this external device can be a Darlington, extending the string to a quad.

## USE OF EXTERNAL NPN PASS TRANSISTOR



Figure 4-4

USE OF PNP-NPN PASS TRANSISTOR


ALL RESISTOR VALUES ARE IN OHMS
Figure 4-6

ALL RESISTOR VALUES ARE IN OHMS
Figure 4-5


ALL RESISTOR VALUES ARE IN OHMS


All resistor values are in ohms
Figure 4-7

This arrangement has the merit of economy, since npn power transistors are generally cheaper than pnp, but has the disadvantage that the minimum differential voltage between input and output is increased by the $V_{B E s}$ of the external transistors. The load regulation is also somewhat degraded since the error amplifier gain is finite and the $V_{B E}$
drops of the external transistors is a function of load current.

An alternative circuit avoiding the disadvantages mentioned above is shown in Figure 4-5. This circuit uses the pnp transistor whose base drive is obtained from the $\mathrm{V}_{\mathrm{C}}$ terminal.

The resistor R3 is used to ensure Q1 turns off under no load conditions, avoiding the excessive buildup of leakage current that can sometimes occur at high temperature. The effect of Q1 is to multiply the hFE of the output transistor in the IC, without increasing the $V_{B E}$, hence this circuit optimizes the load regulation also. Once again, this device
can be replaced by a Darlington pair, but the $V_{B E}$ buildup begins to affect the differential voltage limit. The best arrangement is that shown in Figure 4-6. The npn pass transistor is driven from a pnp device to enhance beta. Thus, large output currents are gained without sacrificing minimum input to output voltage differential.

The short circuit and overload protection techniques discussed later can all be applied to these pass transistor circuits. The currents can be scaled by altering the value of Rsc.
This will protect the entire regulator against overload but will not protect the IC from pass transistor failure. The limit is set at several amperes - enough to destroy the IC - should the transistor fail. Protection from such failure can be provided by the circuit of Figure 4-7.

RsC1 performs the main short circuit protection, but RsC2 limits the IC output current to a safe value if the pass transistors fail. The normal voltage drop in RsC2 should be small compared with the voltage drop in R $\mathrm{RC}_{1}$. This circuit may be modified to include all the protection techniques discussed next.

## OVERLOAD PROTECTION

The simple short circuit protection arrangement of Figure 4-2A gives the typical output characteristic illustrated in 4-2B. This shows the variation of limit current with temperature and the sharp knee between the constant voltage and constant current regions. Adequate for most applications,
this method has the benefit of simplicity. The value of the short circuit resistor RSC is given by:
(Equation 4-10)

$$
I_{S C} \simeq \frac{V_{\text {sense }}}{R_{s c}}
$$

Many variations of the basic circuit exist. Since the regulator is shut down when the voltage difference between $\mathrm{C}_{\mathrm{L}}$ and $\mathrm{C}_{S}$ reaches $V_{\text {sense }}$, a set of resistors to achieve limiting or a locus other than that given by equation 4-10 can be chosen. For instance, it might be beneficial to limit one supply to a lower current level than another.

The arrangement of Figure 4-8 produces a limit relationship
(Equation 4-11)

$$
I_{L 1} R_{S C}+I_{L 2}\left(R_{S C}+R_{S C 2}\right)<V_{\text {sense }}
$$

This allows a higher limit on output 1 [ $V_{\text {sense }} / R_{S C} 1$ if $\mathrm{IL}_{2}=0$ ] than on output 2 $\left[V_{\text {sense }} / R_{S C 1}+R_{S C 2}\right)$ if $\mathrm{I}_{\mathrm{L} 1}=0$ ], but protects both outputs to less than these limits if the other is carrying current. The price paid is that only one output can be well regulated. The other output has an effective output impedance derived from the Rsc's. If output 1 is stabilized (by tying R1 to it), then the output impedance of output 2 will be RSc2 higher; if output 2 is stabilized, then output 1 has a low output impedance, but a high mutual impedance from the load current IL2.

In general, any linear combination of load currents and input or output voltages can be
used to set the overload operating conditions. In extreme cases the use of an op-amp summing amplifier to drive $C_{L}$ or $C_{S}$ could be considered. However, the simple limit scheme depicted in Figures 4-2 and 4-3 is adequate to cover most cases.

## FOLD BACK CURRENT LIMITING

The primary limitation on the use of the simple protection of Figure 4-2 arises from the power dissipation under short circuit conditions. The power dissipation allowed depends on the package type. For simplicity, we will discuss the L package (10 lead T05) values, but the other package limits can be substituted readily. At ambient temperatures below $30^{\circ} \mathrm{C}$, this limit is 800 mW , giving a junction-to-ambient temperature difference in the neighborhood of $120^{\circ} \mathrm{C}$. Above this temperature, derating at $6.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$, we find at an ambient of $50^{\circ} \mathrm{C}$, 680 mW , at $75^{\circ} \mathrm{C}, 510 \mathrm{~mW}$, at $100^{\circ} \mathrm{C}, 300 \mathrm{~mW}$, and at $125^{\circ} \mathrm{C}, 170 \mathrm{~mW}$.

Clearly, under short circuit output conditions, the dissipation becomes the product of the full input voltage and the short circuit current. Consider a device with 20 V IN, 15 V OUT, and 60 mA current limit, operating at ambient temperature of $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$. The standby current will be assumed to be 2 mA or a dissipation of 40 mW . The pass transistor dissipation just before overload is 5 V at 60 mA , or 300 mW , for a total of 340 mW , well within ratings. But under short circuit conditions, the initial pass transistor dissipation is 20 V at 60 mA , or 1.2 W (a total of 1.24 W ), in excess of the allowed ratings. If the 340 mW



Figure 4-9a


Figure 4-9b

## REMOTE SHUTDOWN REGULATOR



Figure 4-10

## REMOTE SHUTDOWN REGULATOR

 WITH CURRENT LIMITING

Figure 4-11
dissipation is maintained to reach equilibrium, the junction temperature will rise to about $75^{\circ} \mathrm{C}$, and the short circuit current will fall to about 52 mA , so the short circuit dissipation is then 1.08 W , still in excess of ratings. Eventually, the junction temperature will reach $150^{\circ} \mathrm{C}$, where the short circuit current will be about 37 mA , and the total dissipation about 800 mW , just acceptable at an ambient temperature of $25^{\circ} \mathrm{C}$. High ambient temperature will degrade the situation. Taking a worst case situation, with $V_{I N}$ $=40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=125^{\circ} \mathrm{C}$, and I standby $=2.0 \mathrm{~mA}$,
the allowable package dissipation is 170 mW , of which 80 mW is taken by standby current, leaving 90 mW for the pass device. Thus, the short circuit current must not exceed 2.2 mA . However, with Vout at 35 V , the allowable output current is 18 mA . The same problem arises in circuits using pass transistors, except that the dissipation is transferred to the pass transistor itself.

The solution to this problem is found in foldback current limiting circuits. The 550 device is particularly well suited to this type
of circuit. The basic 550 foldback circuit is shown in Figure 4-3. The internal operation of this circuit was described earlier and will not be repeated here. The current that can be drawn without significant drop in Vout' called the knee current, ( $l_{\text {knee }}$ ), can be considerably greater than the short-circuited output current, in this case called the foldback current, Isc. The equations controlling the currents are, for $I_{\text {knee }}$,
(Equation 4-12)

$$
I_{\text {knee }}=V_{\text {sense }} / R_{\text {sc }}
$$

and for Isc,
(Equation 4-13)

$$
\begin{aligned}
\text { IsC } & =\left(V_{\text {sense }}-\mathrm{ICLRFB}^{2}\right) / R_{\text {sc }} \\
& =\left(\mathrm{V}_{\text {sense }}-\mathrm{RFB}_{\mathrm{FB}} \cdot 125 \mu \mathrm{~A}\right) / \mathrm{RsC}^{2}
\end{aligned}
$$

where ICL is $125 \mu \mathrm{~A}$.
The primary disadvantage of this scheme is that for certain load lines the circuit will not start. Large capacitive loads may trigger the fold back circuit causing the regulator to prematurely shut down. Momentary overloads such as start up may have to be tolerated in this case by shorting out Rsc until the capacitance has charged. The advantage of this circuit is that the dissipation under all types of overload is markedly reduced and by careful design, the knee current can be set at the dissipation limit value without exceeding this limit under overload.

An alternative circuit, with advantages and disadvantages of its own, is shown in Figure $4-9$. This circuit can be used with the 550 and the $\mu \mathrm{A} 723$ devices, and is basically a variant of the "linear combination of voltage and current" type.

Here, the combination is of load current and output voltage, such that

(where $\mathrm{I}_{\mathrm{cl}} \approx 125 \mu \mathrm{~A}$ for the 550 )
Solving for $I_{\text {knee }}$ we find
(Equation 4-15)

$$
I_{\mathrm{knee}}=\frac{(R 3+R 4)\left(V_{\text {sense }}-I_{\mathrm{c}}(R 3)+V_{\text {out }} 3\right.}{R_{\text {sc }} 4}
$$

The short circuit current is less than the full load or "knee" current and is described by
(Equation 4-16)

$$
I_{s c}=\frac{(R 3+R 4)\left(V_{\text {sense }}-I_{c \mid R}()\right.}{R s C R 4}
$$

The parallel combination of R3 and R4 form a feedback resistor so the impedance should be less than 1 kohm. Values larger than 1 kohm cause the inherent foldback characteristic of the 550 to latch back before assuming the linear load line of Figure 4-9.

Ignoring small quantities the resistor values of R3 and R4 are selected from the ratio
(Equation 4-17)

$$
\frac{R 4}{R 3}=\frac{\left(V_{\text {OUT }} \text { Isc }\right)}{V_{\text {sense }}\left(I_{\text {knee }}-I_{\text {sc }}\right)}-1
$$

A design example is included here to illustrate the design procedure.

> Design Example
> 18 Volt Input
> 10 Volts Output @ 1 Amp
> Foldback Current Limiting

Step 1 Compute minimum I short circuit with $I_{\text {knee }}=1 \mathrm{amp}$ by

$$
\frac{I_{\text {sc }}}{I_{\text {knee }}}>\frac{2 V_{\text {sense }}}{V_{\text {sense }}+V_{\text {out }}}>\frac{1.2}{10.6}>113 \mathrm{~mA}
$$

Step 2 Select $l_{\text {sc }}$ at 150 mA
Step 3 Calculate R3/R4 ratio by

$$
\begin{aligned}
\frac{R 4}{\mathrm{R} 3} & =\frac{\mathrm{V}_{\text {OUT }}\left(I_{\text {sc }}\right)}{V_{\text {sense }}\left(I_{\text {knee }}-I_{\text {sc }}\right)}-1 \\
& =\frac{(10)(150)}{.6(.850)}-1=2.94
\end{aligned}
$$

Step 4 Because R3 in parallel with R4 must be less than 1 kohm select R3 at $1 k$. Thus, R4 becomes 2.94 K . Rounding to standard values select $\mathrm{R} 3=1 \mathrm{~K}$ and $\mathrm{R} 4=3 \mathrm{~K}$.
Step 5 Calculate Rsc by

$$
\begin{aligned}
R_{\text {sc }} & =\frac{(R 3+R 4)\left(V_{\text {sense }}-I_{\text {cl }} R 3\right)+V_{\text {OUT }} 3}{I_{\text {knee }} R 4} \\
& =\frac{(4)(.475)+10}{3}=3.96 \Omega
\end{aligned}
$$

Step 6 Select standard value of $R_{s c}=4$ ohms
Step 7 Recalculate $1_{k n e e ~ u s i n g ~ t h e ~ s e l e c t e d ~}^{\text {l }}$ standard values.

$$
\begin{aligned}
I_{\text {knee }} & =\frac{(R 3+R 4)\left(V_{\text {sense }}-I_{c \mid} R 3\right)+V_{\text {OUTR }}}{R_{\text {sc }} R 4} \\
& =\frac{(4)(.475)+10}{4.3}=.991 \mathrm{amp}
\end{aligned}
$$

Step 8 Recalculate $I_{s c}$ using selected values

$$
\begin{aligned}
I_{\text {sc }} & =\frac{(R 3+R 4)\left(V_{\text {sense }}-I_{\text {cl }} R 3\right)}{R_{\text {sc }} R 4} \\
& =\frac{(4)(.475)}{12}=158 \mathrm{~mA}
\end{aligned}
$$

Figure $4-9 \mathrm{a}$ illustrates the final regulator arrangement with the shut down locus given by Figure 4-9b. Excellent alignment of calculated and measured results was obtained. The foldback characteristic is of the type shown in Figure 4-9b and should be contrasted with that of Figure 4-3.
Two distinct disadvantages of this circuit are readily apparent. First, the voltage drop across $\mathrm{R}_{\mathrm{sc}}$ becomes large and adds directly to the minimum differential voltage required between VIN and Vout. This in turn causes excessive power consumption in the regulator since the power dissipated by the pass transistor is equal to the input-output voltage differential multiplied by the peak load current.
Secondly, since $R_{\text {sc }}$ is larger than normal, and must handle all load current, its wattage must be increased. It should be noted that load regulation will be adversely affected as well.

With these disadvantages in mind, large peak current regulators are usually best protected by the foldback characteristic shown by Figure 4-3. This circuit is advantageous because $R_{s c}$ is small and therefore affects load regulation to a smaller degree and the latch back characteristic instantly switches the regulator from an overload condition back into one of safe power dissipation.

## REMOTE SHUTDOWN

Quite often, especially in large systems, a circuit failure or alarm may be required to remove power from the main system. Remote control of the 550 is relatively easy as shown in Figure 4-10. A current injected into $R_{x}$ sufficient to develop $V_{\text {sense }}$ across $R_{x}$ will shut down the regulator.

Note that for the 550 if $I_{C l} \bullet R_{x}$ is greater than $\mathrm{V}_{\text {sense }}\left(\mathrm{I}_{\mathrm{cl}}=125 \mu \mathrm{~A}\right.$ ), the regulator will latch in the shut down mode until $R_{x}$ is sufficiently reduced. This action can be beneficial in avoiding the requirement for an external latch should the initial remote command be
removed when the supply shuts down. Use of this technique will be discussed in more detail later.

A remote control circuit which retains any of the current limiting protection schemes so far discussed and adds control via a standard TTL logic level is shown in Figure 4-11. The gate listed in the figure is a suitable open collector gate with high voltage breakdown.

Selection of any other open collector gate should be based upon a breakdown at least 2 volts higher than the maximum Vout and with output leakage well below $50 \mu \mathrm{~A}$.
Naturally, no gate inputs or other loads should be tied to the line, but any number of gates meeting the above needs in total may be used in a wired-OR configuration. Tristate outputs may not be used. Note that if the normal Vout is high, the load capacitance may be discharged through the reverse emitter base diodes of the pass transistors and the gate. This current can be limited by a series resistor not to exceed 2 kohms. Remote shut down is especially useful to ensure turn off of multiple supplies if any one supply becomes overloaded.
A schematic showing one possible technique for doing this is shown in Figure 4-12, where the use of open collector AND gates gives a simple logic structure. The diodes are not needed for supplies not exceeding the Vcc logic level, and it has been assumed that each supply has a load adequate to turn on the gate input.
The string may be reset by shutting down the Vcc supply to the gates, which must be separate from the string of controlled supplies.

Another circuit technique giving linked shutdown of regulators is given in the NonBasic Configurations Section, (Figures 4-17 and 4-18).

Figure 4-13 shows another use of the latch capability of the 550 regulator in a remote latching shutdown regulator. The circuit is operated by TTL gates, with separate inputs for shutdown and unlatch (or reset). In normal operation, the shutdown line is high, so the output of the shutdown gate is low, and regardless of the state of the unlatch gate, Vout is set at the normal level.
If the unlatch input is low, and the shutdown input goes low, the CL input will be pulled up by R3 (and R4 if needed), the regulator will shut down, and the current sourced from the CL terminal will latch the regulator shutdown, even after the shutdown line goes high again, while the unlatch input remains low. When the unlatch line goes high, the sourced current is taken through

## REMOTE SLAVING OF MULTIPLE SUPPLIES



Figure 4-12

LATCHING REMOTE SHUTDOWN REGULATOR


All resistor values are in ohms

BASIC NEGATIVE REGULATOR


All resistor values are in ohms

Figure 4-13
the unlatched gate, the CL terminal drops below $V_{\text {sense, }}$ and the regulator resets. The figure lists some suitable gates, but any open collector gate can be used for the unlatch gate, and any gate at all for the shutdown gate. If an active pullup gate is used in the latter position, R4 may be omitted. Using 8T90 gates, a pulse width into the shutdown input of 50 ns was found adequate to ensure latched shutdown, although the
regulator output in the configuration tested did not decay fully until more than $1 \mu$ s after the pulse. Since this circuit uses the internal shutdown components, additional short circuit protection would require an external transistor, connected to the compensation terminal. This basic arrangement can also be used with MOS logic driving the $\mathrm{C}_{L}$ input, although diode gating will normally be needed to ensure correct operation.

## NON-BASIC CONFIGURATIONS

All the circuits discussed so far have been variations on the basic positive voltage regulator. There are many other circuit configurations that can be used, however, including negative voltage regulators, floating regulators (for voltages exceeding the maximum voltage ratings) and switching regulators for highly efficient regulation. Many of

NEGATIVE REGULATOR (LESS THAN -8.5 VOLTS)


All resistor values are in ohms

## PROVIDING NEGATIVE REGULATOR OVERLOAD PROTECTION



All resistor values are in ohms

Figure 4-15
Figure 4-16


All resistor values are in ohms

Figure 4-17
the pass transistor and overload protection circuits discussed in the previous section are applicable to these configurations also.

## NEGATIVE REGULATORS

The basic negative voltage regulator circuits are shown in Figure 4-14.
Note that for units not having the $V_{Z}$ terminal (those in 10 pin packages) an external 6.2V Zener can be used.

The inverting and non-inverting input connections are reversed, and the pass transistor Q1 acts as a level shifted emitter follower from Vout to drive the output. The regulator is driven from its own output, so the line regulation is excellent, the load regulation is controlled by the hFE of Q1 and the load
regulation of the IC. R3 must be of sufficient value to drive the maximum load current through Q1 at the minimum input voltage, and large enough not to draw more than 10 mA through the internal Zener (the Vz terminal) at minimum load and maximum VIN. This places a lower limit on the hFE of Q1, which for large currents may need to be a Darlington pair or equivalent.
The supply voltage for the regulator is derived from the output voltage. For this reason the output voltage available is limited to values more negative than -8.5 volts.
A circuit such as in Figure 4-15 overcomes this limitation but assumes the presence of a positive supply. This is usually acceptable since the majority of negative regulator
requirements arise from the need for symmetrical positive and negative voltages.

The diode and resistor frequently shown in negative regulator applications is necessary to avoid a possible forward base-collector bias on Q12 of Figure 4-1. Should forward base-collector bias occur, the regulator will latch up preventing regulation at initial power up. The diode can be a small signal type with a forward current of $100 \mu \mathrm{~A}$. Diode current flows only during initial turn on and sees approximately two volts reverse bias under normal operation. The resistor should be of sufficient value to allow approximately $100 \mu \mathrm{~A}$ to flow into the VOUT terminal.

Short circuit protection of negative regula-


Figure 4-18

NEGATIVE FLOATING REGULATOR


All resistor values are in ohms
Figure 4-19


Figure 4-20
tors cannot be implemented with the circuits previously described because of the inversion of the error amplifier inputs.

Protection can be provided with the addition of a transistor as illustrated by Figure 416. Note that the saturation voltage of Q2 at the maximum current through R5 must be less than the VBE of Q1. Other components are not critical.

## FLOATING REGULATORS

So far only output voltages less than the 40 volt maximum ratings of the 550 have been covered. The maximum voltage limitation can be overcome by using floating regulator techniques.
The limits on VIN can be overcome by using a preregulator to feed the $\mathrm{V}+$ and $\mathrm{V}_{\mathrm{c}}$ lines, but the Vout limitation requires greater sophistication. The circuits of Figures 4-18 and 4-19 show two techniques that can be used to give output voltages well outside the range of the IC device.

In both circuits, R3 and CR1 provide a low voltage supply to preregulate the input volt-
age to a level within the IC ratings. The circuits of Figure 4-18 connects the internal pass transistor in the grounded emitter configuration through the 6.2 volt zener $\mathrm{V}_{\mathrm{z}}$ with overload protection provided by R5. Cascaded into the pass transistor is the high voltage transistor Q1 which provides level translation and voltage control to Q2, the pass transistor.

Short circuit protection can be arranged by removing base drive from Q2 is desired.

## SWITCHING REGULATORS

Up to this point only series dissipative regulators have been discussed. All circuits presented thus far have the disadvantage of low efficiency. By definition these regulators must dissipate the power difference between input and output voltage and the load current such that

## (Equation 4-18)

$$
P_{D}=I_{L}\left(V_{\text {IN }}-V_{\text {OUT }}\right)
$$

This is in addition to the standby power dissipation of the regulator circuit itself.

Thus, it becomes prohibitive in terms of efficiency to build a dissipative regulator with high output currents and high input to output voltage differentials. These parameters are best implemented with a switching type regulator taking advantage of the very high efficiency of such a circuit. By using the switching technique the power transistor requirements and its associated heat sink size can be greatly reduced.

Switching regulators consist of a switch S , a level detector, and an LC network L1, C1 as depicted in Figure 4-20. The cycle begins when switch S is closed causing a nearly linear current to build up through L1. This current, less the load current, charges C1 until the upper threshold of the detector is reached.

At this point S1 is opened and D1 forward conducts eventually discharging C1 through L1 to the lower threshold limit at which time S1 closes, restarting the sequence. A sketch of the basic waveforms is shown in Figure 4-21 for two different duty cycles. The output voltage is a function of the duty cycle of the switching waveform.

## SWITCHING REGULATOR WAVEFORMS



Figure 4-21

Therefore, regulation can be achieved if the duty cycle is made variable as is the case with switching regulators. The detailed theory and design of switching regulators is complex, but the basic operation makes the following assumptions:

1. Operating frequency well above resonant frequency of $L$ and $C$.
2. Harmonics of input square wave are attenuated.
3. Phase shift of lowest frequency is $180^{\circ}$.

The last assumption provides the minimum output ripple at close to the hysteresis limits of the threshold control device.
The frequency of operation is a function of load levels, input voltage levels, and threshold levels. Although it is possible to synchronize the switching frequency with an external source, the electrical interference problem usually requires that the regulator be well shielded. The choice of operating frequency is in general a compromise between the inductor size becoming prohibitive at low frequencies, and switching losses in D1 and S1 becoming excessive at high frequencies. Values between 10 and 25 kHz are normally satisfactory. Note that the load current flows as a dc current through L1, and that the peak current Imax can be quite a bit more than that. The inductor should not saturate at that level, or the frequency will increase abruptly, the efficiency will fall rapidly, and potential disaster will ensue. The diode and switch must also handle Imax. There is a considerable high frequency ripple current in C 1 of $\mp\left(I_{\text {max }}-l_{\text {out }}\right)$. The component used must be capable of handling that current.

A circuit realization for Figure 4-20 is shown in Figure 4-22. The switch S 1 is replaced by a Darlington pnp pair Q1 and Q2 and the threshold detector by the 550 device, driving Q1 and Q2 from the $\mathrm{V}_{\mathrm{c}}$ pin.

The peak driving current through the 550 is set by Rsc. This does not, of course, protect the whole regulator, just the 550 itself. The threshold values are set by VREF in combination with R1 and R2, and the threshold hysteresis is controlled by R3 and the internal impedance of $V_{\text {ref }}$ (about $2 \mathrm{k} \Omega$ ), as derived from the voltage across D1. The capacitor across R1 reduces the ripple on the output by increasing the feedback at ripple frequencies. Diode D2 prevents the possibility of initial latchup in the 550. A similar circuit can be used for the $\mu \mathrm{A} 723$, if a resistor of $1-2 k \Omega$ is included between $V_{\text {REF }}$ and the junction of R3 and the non-inverting input, and the values of R1 and R2 are modified to suit the different $V_{\text {REF }}$ value.

The component values may be chosen by the following algorithm, which is approximate:
Neglecting switching transients,

$$
\text { VOUT }=\text { tONf } V_{I N}
$$

where tow is the time $S 1$ is on, and $f$ is the frequency of operation, so having chosen $f$ for some $\mathrm{V}_{\mathrm{IN}}$, and knowing Vout.
(Equation 4-19)

$$
\begin{aligned}
\text { ton } & =\frac{V_{\text {OUT }}}{V_{\text {IN }}}\left(\frac{1}{f}\right) \text { and tofF } \\
& =\left(1-\frac{V_{\text {OUT }}}{V_{\text {IN }}}\right)\left(\frac{1}{f}\right)
\end{aligned}
$$

The current in L 1 increases almost linearly during ton, so we may find L1 from lout, Imax, and ton, or toff
(Equation 4-20)

The output ripple is derived from the difference between IL1 and lout charging C1, so for a given output ripple $\Delta \mathrm{V}$ Out, we can write
(Equation 4-21)

$$
C_{1}=\frac{\text { IMAX }- \text { IOUT }}{4 f \Delta V O U T}=\frac{V_{I N}-V_{O U T}}{8 L 1+2 V_{I N}} \cdot\left(\frac{V_{\text {OUT }}}{\Delta V O U T}\right)
$$

Note that if we put

$$
\frac{V_{\text {IN }}-V_{\text {OUT }}}{V_{\text {IN }}} \simeq 1
$$

we find
(Equation 4-22)
$f \simeq \frac{1}{(8 \mathrm{~L} 1 \mathrm{C} 1) 1 / 2} \cdot\left(\frac{\Delta \mathrm{~V}_{\text {OUT }}}{\Delta \mathrm{VOUT}}\right)^{1 / 2}$
The values of L1 and C1 also control the load transient response. The voltage overshoot for a load decrease of $\Delta$ lout is
(Equation 4-23a)

$$
\Delta V_{\text {out }}=\left(\frac{\Delta \text { loutrr }_{r}}{2 \mathrm{C} 1}\right)=\left(\frac{\Delta \text { lout } 2}{V_{\text {OUT }}}\right)\left(\frac{\mathrm{L} 1}{\mathrm{C} 1}\right)
$$

where the recovery time
(Equation 4-23b)

$$
\mathrm{t}_{\mathrm{r}}=2 \mathrm{~L} 1\left(\frac{\text { IIOUT }}{V_{\text {OUT }}}\right)
$$

and for a load increase of slout is
(Equation 4-23c)

$$
\Delta \text { VOUT }=\frac{\Delta \text { lourtr }_{r}}{2 \mathrm{C} 1}=\left(\frac{\Delta \text { louT2 }}{V_{\text {IN }}-V_{\text {OUT }}}\right)\left(\frac{\mathrm{L} 1}{\mathrm{C} 1}\right)
$$

and
(Equation 4-23d)

$$
\mathrm{t}_{\mathrm{r}}=2 L 1\left(\frac{\Delta \text { IOUT }}{V_{\text {IN }}-V_{\text {OUT }}}\right)
$$

The exact frequency of oscillation and, in fact, the functionality of the circuit depends upon the parasitic components. From the preceding equations it follows that the circuit as shown will not sustain oscillation. Fortunately the imperfections of components comes to the rescue and the circuit is restored to operation by the parasitic elements indicated in Figure 4-23. The most
important of these is the series resistance of C1, R .

The effective series resistance of the inductor $R_{L}$ also contributes, and the storage in diode D1 adds a small step. These contributions are indicated in the waveforms of Figure 4-24. All generate a difference in Vout at the two switching points, which of course must correspond to the hysteresis in the threshold detector. Acting in the opposite direction are the delay, and the rise and fall times in the switch.
Considering first the effect of $R_{c}$, we may write at once (even through we don't know the value of $R_{c}$ ),
(Equation 4-24)

$$
V_{T / R_{C}}=2\left(I_{M A X}-I_{O U T}\right) R_{C}
$$

Substituting into equations 4-18 and 4-19, we obtain
(Equation 4-25)

$$
f=\frac{V_{\text {OUT }}}{V_{\text {IN }}}\left(\frac{1}{\text { toN }}\right)=\frac{V_{\text {OUT }}}{V_{T}}\left(1-\frac{V_{\text {OUT }}}{V_{\text {IN }}}\right) \frac{R_{C}}{2 L 1}
$$

The easiest way to establish the effect of RL is to assess the phase change for the first harmonic of the waveform on VD1. This procedure is at best approximate, but except for extreme duty cycles, the higher harmonics at the input are smaller than the first. Since the attenuation of $L$ and $C$ is at 12 dB per octave, the influence on the answer obtained of these harmonics is small. It is convenient to treat the switching delays in S1 as a phase change at the same point.
This total phase change can then be written
(Equation 4-26)

$$
\Theta \simeq \frac{\mathrm{R}_{\mathrm{L}}}{2 \pi \mathrm{fL} 1}-2 \pi \mathrm{fts}
$$

where

$$
t_{s}=\frac{1}{2}\left(t_{r}+t_{f}\right)
$$

This leads to a threshold voltage difference at the switching points (assuming the phase change is small) of

## (Equation 4-27)

$$
\begin{aligned}
& V_{T} \left\lvert\, R_{L}=\Delta V_{\text {OUTSin }}(\pi f \text { toN })\left[\frac{R L}{2 \pi f L 1}-2 \pi f t_{s}\right]\right. \\
& =\mathrm{V}_{\text {OUT }} \sin \left(\frac{\pi \mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\text {IN }}}\right)\left[\frac{\mathrm{R}_{\mathrm{L}}}{2 \pi \mathrm{f} 1}-2 \pi \mathrm{t}_{\mathrm{s}}\right]
\end{aligned}
$$

The stored charge in the transistor forming S 1 is primarily introduced by the threshold detector, and its removal can be included in the fall time $\mathrm{t}_{\mathrm{f}}$ accounted for in equation 4 26. The charge removal from the diode is performed by S1, which passes a current surge when switching on. This current does not pass through L1 and has no influence on the remainder of the circuit. However, the charge needed to turn the diode on is provided by the current in L1. The voltage impulse needed to do this gives a current step in IL1 given by

$$
I=\frac{Q_{D} R_{D}}{L 1}
$$

where $Q_{D}$ is the stored charge, and $R_{D}$ is the effective series impedance of the diode.


PARASITIC COMPONENTS



Figure 4-23

This leads to an effective $V_{T}$ of approximately
(Equation 4-28)

$$
\mathrm{V}_{T \mid}{Q_{D}}=\left(\frac{Q_{D} R_{D}}{2 L 1 C 1}\right)\left(\frac{V_{O U T}}{V_{I N}}\right) \text { toN }
$$

The waveforms resulting from these various terms are sketched in Figure 4-24.
Note that in the circuit of Figure 4-22, the value of $\mathrm{V}_{T}$ at which the circuit operates is a function of $V_{I N}$, so the frequency may be approximated by
(Equation 4-29)

$$
f \simeq\left(\frac{R_{S}}{R_{I N T}}\right)\left(\frac{V_{\text {OUT }}}{V_{I N}}\right)\left(1-\frac{V_{O U T}}{V_{I N}}\right)\left(\frac{R_{C}}{2 L 1}\right)
$$

where $R_{I N T}$ is the internal reference impedance, about $2 \mathrm{~K} \Omega$.

As a function of $\mathrm{V}_{\mathrm{IN}}$, we can see that f will be low for both high and low values of VIN and it will go through a maximum to the point near where $\mathrm{V}_{\mathrm{IN}} \approx 2 \mathrm{~V}_{\text {out }}$.

The value of Rc can be estimated from equation 4-28 and gives a value of 0.35 to $0.4 \Omega$. Since the performance of the circuit depends to some extent on the effective series impedance of C 1 , which may not be sufficiently well controlled for some applications, it may be worthwhile to place a small value resistor in series with C1 to reduce circuit to circuit variation.

In applications where the frequency of operation is important (such as EMI supression), the regulator may be locked to an external signal by means of the circuit of Figure 4-25.

## SYNCHRONIZED SWITCHING REGULATOR



Figure 4-25

The incoming signal is converted to a triangle wave by R3 and C3, and added to the reference voltage. If the drive signal is already a triangle wave, (derived from pin 4 of a 566 oscillator) C3 can be omitted, and R3 increased to about $100 \mathrm{~K} \Omega$. The amplitude of the triangle wave at the reference pin must exceed the amplitude of the ripple on Vout, $(50 \mathrm{mV}$ is suitable for normal use). The duty cycle of the switching pulse is controlled by the relative values of VOUT and the (referred) VREF with impressed triangle, thus ensuring the required regulation. The remainder of the circuit operates as precisely as before. Note that neither switching point is controlled in phase relative to the controlling waveform. Thus, spikes from other controlled regulators could cause false switching if inadequately shielded from each other. The line regulation is closely related to the amplitude of the triangle wave. The gain of the amplifier is adequate to give sharp switching transitions, even without explicit positive feedback.

A negative switching regulator may be constructed similarly, as shown in Figure 4-26. The same basic restrictions apply here as in the simple negative regulator of Figure 4-14, the output voltage must be at least -8.5 V unless a positive supply is available. The basic operation is the same as before. An alternative negative switching regulator is shown in Figure 4-27. This circuit always needs a positive supply.
All these regulators suffer from a lack of short circuit protection. The difficulty in providing protection is that the regulator must continue to switch. If it does not, the switching transistors will become pass transistors with an extreme increase in dissipation!


Figure 4-26

SWITCHING REGULATOR (LESS THAN -8.5 VOLTS)


Figure 4-27


In general, the best way to arrange for continued switching is to modify the voltage feedback to the amplifier in order to effectively maintain VREF at the comparison point even in shutdown. This can be achieved simply by sensing the current in the switching transistor, as shown in Figure 4-28.
This has a disadvantage in that the current surge when the transistor switches the diode off must be allowed for, and the limit point is somewhat dependent on duty cycle. A better arrangement is shown in Figure 429. This needs more external transistors, but gives much better control since the current through the inductor is sensed.

The current derived is used to raise the apparent output voltage as seen at the inverting input. Since the amplifier will not work with Vout at ground, the $\mathrm{V}_{\mathrm{z}}$ output is tied to ground. The $V_{z}$ output can be tied to Vout, avoiding the waste of that current, if the input-output differential is large enough. Note that this technique can be applied to the negative regulator shown in Figure 4-27, (provided $\mathrm{V}+$ is more than 8.5 V ), but not to that of Figure 4-26.

Since the dissipation in the switching devices is not very dependent on either VIN or Vout, the elaborate protection schemes devised for the pass transistor case are not
really applicable here. For applications where the ripple, transient and regulation performance of the switching regulators are unacceptable, a combination of a switching regulator which gives highly efficient preregulation for a static regulator may provide a satisfactory solution.

## NOISE, TEMPERATURE EFFECTS, AND TRANSIENT RESPONSE

An almost inherent property of reverse biased junctions of the emitter base type is voltage noise at breakdown as a result of socalled microplasmas. The noise arises as a
result of space-charge induced instability of the breakdown of localized minor imperfections and irregularities. The inherently clean and defect free processing used for integrated circuits reduces this effect to a minimum, but the statistical inevitabilities of diffusion processes have sufficient irregularity to lead to some small noise generation. The characteristic noise pattern is displayed as step-function current change as each microplasma switches on and off. Each microplasma switches at roughly constant voltages, leading to approximately constant voltage transitions.

Since the reference voltage for the 550 is derived from the breakdown of the emitterbase junction, this noise will appear at the reference terminal. Transformed by the internal network between the zener diode and the reference terminal, this is the major component of noise in the regulator. For applications where the noise level could be troublesome, it can be reduced by putting a low pass filter between the zener and the amplifier input. The low frequency component of the noise is quite small. Since the internal reference impedance of the 550 is $2 \mathrm{~K} \Omega$, placing a capacitor between VreF and ground will generally be all that is required.

In circuits where the reference is divided down, the divider impedance provides some effective series resistance, but in other applications better results may be obtained by the use of a simple series RC network Suitable circuits are shown in Figures 4-30a and 4-30b.

The line and load regulation performance discussed in previous sections and presented in the data sheets are all values defined and measured under such conditions that
the die temperature is constant. The circuit dissipation is changed by changes in input line voltage and load current. Therefore, the consequent changes in die temperature, which primarily affects the reference voltage, must be accounted for separately. The temperature effects are certainly not negligible in many applications.

A regulator operating at 10 V in and $5 \mathrm{~V}_{\text {out }}$ with a load current that steps from 1 mA to 50 mA will have a short time ( $1-10 \mathrm{msec}$ ) output voltage change of typically under 3 mV . The dissipation increases, however, by 250 mW , leading to a temperature rise of about $25^{\circ} \mathrm{C}$ at the die. With temperature coefficient of $0.005 \% /{ }^{\circ} \mathrm{C}$, this leads to an output voltage change of 6 mV , twice the short time value. If the input voltage had been higher, say 15 V , the same load step would eventually result in about four times the voltage change, though the short term change would not be affected significantly.

The effects of transient line and load changes are primarily concerned with the impulse response of the amplifier, which in turn depends on the compensation and external connections involved in the particular circuit being used. Typical transient responses for simple configurations are given for the 550 in Figure 4-31.

There are three effects to be considered, then, upon imposition of a line or load step to a regulator circuit; the initial reaction is controlled by the transient response. After a few microseconds, the transient dies away and the response becomes the data sheet defined regulation. After a time of many tens of milliseconds, the changing die temperature begins to take effect. After perhaps one minute, the die temperature stabilizes and
no further changes occur. As mentioned above, each of these effects is effectively separate, and should be allowed for separately.

## 3 TERMINAL REGULATORS

## Introduction

The $\mu \mathrm{A} 7800$ and 78 HV 00 series regulators are monolithic three terminal devices intended for fixed voltage outputs. Since no external elements are required they are excellent candidates for PC card and subsystem regulation. With the use of these devices much system crosstalk and power supply distributed noise can be eliminated.

These devices are available in $5,6,8,12,15$, 18 and 24 volts, positive or negative, with 3 output current ratings. The voltage and power output ranges are designated as follows:


## TRANSIENT RESPONSE



Figure 4-31a

## TRANSIENT RESPONSE



Figure 4-31b

| SERIES <br> PACKAGE | $\begin{aligned} & 7800 \\ & \text { TO-3 } \end{aligned}$ | $\begin{gathered} \text { 7800C } \\ \text { TO-3 } \end{gathered}$ | $\begin{gathered} \text { 7800C } \\ \text { TO-220 } \end{gathered}$ | $\begin{gathered} 78 \mathrm{MOO} \\ \text { TO-39 } \end{gathered}$ | $\begin{gathered} \text { 78MOOC } \\ \text { TO-39 } \end{gathered}$ | $\begin{gathered} 78 \mathrm{MOOC} \\ \text { TO-220 } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum junction temperature, TJ(MAX) <br> Minimum ambient temperature, TJ(MIN) | $\begin{array}{r} 150 \\ -55 \\ \hline \end{array}$ | $125$ <br> 0 | $\begin{gathered} 125 \\ 0 \end{gathered}$ | $\begin{array}{r} 175 \\ -55 \end{array}$ | $\begin{gathered} 175 \\ 0 \\ \hline \end{gathered}$ | $\begin{gathered} 125 \\ 0 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ ${ }^{\circ} \mathrm{C}$ |
| Thermal resistance junction-to-case, ӨJc Thermal resistance junction-to-case, @JA | 4 <br> 35 | 4 $35$ | 4 <br> 50 | $\begin{array}{r} 20 \\ 150 \\ \hline \end{array}$ | $\begin{array}{r} 20 \\ 150 \\ \hline \end{array}$ | $\begin{array}{r} 5 \\ 50 \\ \hline \end{array}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Maximum allowable dissipation, PD(MAX) | 15 | 15 | 15 | 5 | 5 | 5 | W |

Figure 4-32

The $\mu \mathrm{A} 78 \mathrm{HV} 00$ has a unique process which gives an input breakdown voltage greater than 60 volts. Standard operating conditions allow the input voltage to be as high as 48 volts continuous. Transients and momentary inputs may be as high as 60 volts without damaging the regulator. Under these high input conditions, the regulator may go into current limiting or thermal shutdown.
Voltages other than those listed are also available upon special order.

## Applications

As with any voltage distribution system, effort should be expended to keep the output impedance of three terminal regulators as low as possible.
Possessing 20 to 30 milliohms output impedance at low frequencies, the regulator's output impedance will increase with frequency. This becomes significant, especially in TTL systems, where current impulses from the logic are in the Megahertz regions.

Thus it becomes necessary to bypass the supply lines for high frequencies to insure stability and error free operation. The best technique for achieving low impedance at all frequencies is to use a large tantalum (10$47 \mu \mathrm{fd})$ in parallel with small ( $0.01 \mu \mathrm{fd}$ ) disc ceramics. In systems where fairly large printed circuit boards are used, the disc ceramics should be disbursed upon the board to neutralize the trace inductance. No other stabilization techniques should be required.

## Thermal Limitations

The maximum allowable junction temperature and the ambient temperature expected determine whether a heat sink will be required for a particular regulator application.
As seen from the derating curves of Figure 4-32 the maximum no heat sink power dissipation allowable for the TO-3 is 3 watts and for the TO-220 is 2 watts. Above $25^{\circ} \mathrm{C}$ this must be derated according to the relationship


NOTE
To determine either area required or thermal resistance of a given area, draw a vertical line between the top (or area) line down to the material of interest.

Figure 4-33
(Equation 4-30)

$$
\frac{T J(M A X)-T_{A}}{\Theta_{J A}}
$$

Figure 4-32 summarizes the maximum junction temperature and thermal resistivities of the TO-3 and TO-220 packages. The power dissipation qualities of heat sinks are usually well established by the manufacturer. Since the common terminal of these devices is common they may be bolted directly to the chassis, using the surface area as the heat sink.
Figure 4-33 provides a selection chart which relates surface area of the chassis material to the thermal resistivity. It should be noted that the surface area refers to both sides of the material.

In order to find a thermal resistivity scribe a vertical line from the surface area across the appropriate material.

## Heat Sinks

As a further aid in determining which package/heat sink combination is best suited to a given application, the following nomograph (Figure 4-35) solves for $\Theta \mathrm{JA}$ from basic current, input/output voltage differential and ambient temperature information. The package thermal resistances have been superimposed on the $\Theta_{J A}$ line $E$. If the required $\Theta_{J A}$ is less than $\Theta_{\mathrm{Jc}}$ for a package, then that package cannot be considered. Even if an infinite heat sink were possible, the junction temperature would exceed $125^{\circ} \mathrm{C}$. If the required $\Theta_{J A}$ is greater than $\Theta_{J A}$ for a package, that package may be used without a heat sink. In all other cases a package/heat sink combination is necessary. Subtract OJc for the preferred package from the required $\Theta_{\mathrm{JA}}$ to arrive at the necessary heat sink thermal resistance $\Theta$ Hs.
To use the nomograph, select the maximum load current on Line A and the maximum input/output voltage differential on Line D. The line joining these points intersects Line $B$ at a point representing the maximum

power dissipation. Join this Line B intersection to a point on Line C representing the maximum expected ambient temperature. Extend this line so it intersects Line $E$. The Line $E$ intersection represents the total junction-to-ambient thermal resistance required for the particular application. If the Line E intersection falls above the junction-to-ambient thermal resistance, $\Theta_{\mathrm{JA}}$, no heat sink is required.

To determine the thermal resistance of a heat sink, subtract the junction-to-case thermal resistance, ©uc, of the selectnd package from the Line E intersection.

- For TO-39, subtract $20^{\circ} \mathrm{C} / \mathrm{W}$
- For TO-3, subtract $4^{\circ} \mathrm{C} / \mathrm{W}$
- For TO-220, subtract $4^{\circ} \mathrm{C} / \mathrm{W}$


## Example:

Choose a regulator to supply 275 mA (max) with an input/output voltage differential of 6 V (max) at an ambient temperature of $50^{\circ} \mathrm{C}$
(max). Join the 275 mA point on Line $A$ to the 6 V point on Line D . The intersection with Line B gives a power dissipation of 1.7 W . Join 1.7 W to the $50^{\circ} \mathrm{C}$ point on Line C and extrapolate to an intersection with Line E . This gives a total junction-to-ambient thermal resistance requirement of $45^{\circ} \mathrm{C} / \mathrm{W}$. The regulator package choices are

- A TO-39 package with a heat sink of $25^{\circ} \mathrm{C} / \mathrm{W}$ thermal resistance (subtract $20^{\circ} \mathrm{C} / \mathrm{W} \Theta_{\mathrm{Jc}}$ ).
- A TO-220 package with a heat sink of $41^{\circ} \mathrm{C} / \mathrm{W}$ thermal resistance (subtract $\left.4^{\circ} \mathrm{C} / \mathrm{W} \Theta \mathrm{Jc}\right)$.
- A TO-3 package with no heat sink ( $45^{\circ} \mathrm{C} / \mathrm{W}$ falls above $\Theta \mathrm{JA}$ for the TO-3).


## Additional Applications Ideas

The versatility of the 7800 family of regulators may be increased beyond the basic 3terminal use by the addition of external components. The following applications contain circuits which cover the range of
0.5 V to 30 V output, and output currents in excess of 10A. Note that apart from power considerations the 7800 and 78 M 00 devices are interchangeable in all applications.

## Fixed Output Regulator

In this basic application of Figure 4-35, the last two digits of the device code specify the nominal output voltage. The insulating washer normally used when heat-sinking a power transistor may be omitted when mounting the regulator since the case of the device is at ground potential. This is true unless circulating ground currents are a problem.

## Current Regulator

The circuit shown in Figure 4-36 supplies a regulated current to a load, its value being determined by an external resistor. The minimum input/output differential in this application is (minimum regulator input/ output differential voltage) + (maximum

regulator output voltage). For currents up to $1 \mathrm{~A} 0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$, this voltage is typically 2.2 V +5.25 V , or 7.45 V .

## High Current Voltage Regulators

Currents in excess of the output capabilities of the basic regulator can be obtained with the circuit shown in Figure 4-37. The value of R1 determines the point at which Q1 begins to conduct and hence bypasses the regulator. This supply can be protected against a short circuit load by adding a short circuit sense resistor, R2, and a pnp transistor Q2. In this circuit Q2 must be able to handle the short circuit current of the regulator, since when Q1 is bypassed, the regulator goes into its short-circuit mode.

## Variable Output Voltage <br> Regulators

In Figure 4-38 a voltage pedestal is developed across R2, which is then added to the normal regulated output $\mathrm{V}_{\mathrm{xx}}$, such that

$$
v_{0}=v_{x x}\left(1+\frac{R 2}{R_{1}}\right)+l_{q} R 2
$$

The current through R1 should be set much higher than the quiescent current $\mathrm{I}_{\mathrm{Q}}$ to minimize the effects of the change in $\mathrm{I}_{\mathrm{Q}}$ which occurs with a change in $\mathrm{V}_{\mathbb{I}}$.

## Switching Regulators

A switching regulator may be used in those cases where the dissipation of a linear regulator is excessive. Figure 4-39 shows that when power is first applied, current flows through R3 and the 7800 device to the output. As soon as the current generates a voltage drop sufficient to forward bias Q1's base-emitter junction, Q1 is driven toward saturation. The increase in voltage at the collector applies power through L1 to the load and provides positive feedback through R1 and R2 to assure a full switching action. As the output voltage approaches the sum of the 7800 regulated output plus the voltage developed across R2, current flow through the 7800 decreases

Input voltages in excess of the maximum input voltage rating of the regulator may be commodated by the inclusion of a voltage dropping Zener (D1). This reduces the
voltage appearing across leads 1 and 3 of the 7800 to an acceptable level.
When the base current drops below the level required to keep Q1 in saturation, the collector voltage starts to decrease and the positive feedback loop completes the switching action.

## $\mu \mathrm{A} 7814$

There is a sufficient requirement for a power supply output voltage of 13.8 volts. Therefore, Signetics Analog now offers the $\mu \mathrm{A} 7814$ type 1 amp three terminal regulator with 13.8 volts nominal output.
One of the main requirements for this 13.8 volt regulator is for AC line operation of automotive type equipment. With the increase in the number of CB sets and the servicing required on CB, AM/FM stereo radio, the battery substitution power supply is becoming more prevalent. Another major need for battery substitution power supplies is in the home operation of the portable automotive equipment. The portable CB can be removed from the vehicle to prevent theft and also utilized in the home with a

## BATTERY SUBSTITUTION POWER SUPPLY


battery substitution power supply using the $\mu \mathrm{A} 7814$.

## NEGATIVE REGULATORS

## Introduction

The $\mu \mathrm{A} 79$ series regulators are monolithic three terminal devices intended for negative fixed voltage outputs. They are an excellent choice for PC card and subsystem regulation due to their self-contained simplicity. These devices are available in negative 5, 6, $8,12,15,18$ and 24 volts. The voltage and power output ranges are designated as follows:


Voltages other than those listed are also available upon special order.

## Applications

As with the $\mu \mathrm{A} 78$ voltage regulators, effort should be made to keep the output impedance as low as possible. This is accomplished with bypass on the supply lines for high frequencies to insure stability and error-free operation. Use a large tantalum ( $10-47 \mu \mathrm{fd}$ ) in parallel with a small (. $01 \mu \mathrm{fd}$ ) disc ceramic. Output bypass capacitors will improve the transient response of the regulator. A good high frequency ceramic or tantalum of $1 \mu \mathrm{f}$ will generally suffice. Keep lead lengths as short as possible.
All of the applications for Signetics positive regulators can be used with the negative regulators. The polarities are inversed, the sense diode is reversed and the pnp's are replaced with NPN transistors. Specific circuit configurations follow:

TYPICAL APPLICATIONS $\mu$ A79XX SERIES


FIXED OUTPUT REGULATOR


BASIC CURRENT REGULATOR


Output current $=\frac{5.0 \mathrm{~V}}{\mathrm{R} 1}+1 \mathrm{Q}$



HIGH OUTPUT CURRENT, FOLDBACK CURRENT LIMITED



## PROGRAMMABLE REGULATORS

## Introduction

The $\mu \mathrm{A} 78 \mathrm{G}$ and $\mu \mathrm{A} 79 \mathrm{G}$ are positive and negative programmable regulators respectively. They are identical to their $\mu \mathrm{A} 78$ and $\mu$ A79 counterparts with the exception to the reference to the error amplifier being brought out and the voltage determining divider being supplied by the circuit designer rather than internal to the regulator. The voltage may be adjusted over the range of 5 to 30 V for the $\mu \mathrm{A} 78 \mathrm{G}$ and $\mu \mathrm{A} 79 \mathrm{G}$ from- 30 to -2.2 volts. They have the same inherent feature that other devices in the series have.

## Applications

The basic programmable voltage regulator circuits and design considerations follow.

## DESIGN CONSIDERATIONS

The 78G and 79G adjustable voltage regulators have an output voltage which varies from $V_{\text {CONTROL }}$ to typically $\mathrm{V}_{\text {IN }}-2 \mathrm{~V}$ by Vout $=V_{\text {CONTROL }} \frac{(\mathrm{R} 1+\mathrm{R} 2)}{\mathrm{R} 2}$. The nominal reference in the 78 G is 5.0 V and 79 G is -2.23 V . If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make $\mathrm{R} 2=5 \mathrm{k} \Omega$ in the 78G. The output voltage is then: Vout $=(\mathrm{R} 1+\mathrm{R} 2) \mathrm{V}$, where R 1 and R2 are in $k \Omega$ s.

Example: If $\mathrm{R} 2=5 \mathrm{k} \Omega$ and $\mathrm{R} 1=10 \mathrm{k} \Omega$ then $V_{\text {OUT }}=15 \mathrm{~V}$ nominal, for the 78 G ; $\mathrm{R} 2=2.2 \mathrm{k} \Omega$ and $\mathrm{R} 1=12.8 \mathrm{k} \Omega$ then Vout $=-15.2 \mathrm{~V}$ typical, for the 79 G .
By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.
Both 78 G and 79 G regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

|  | TYP | MAX | TYP | MAX |
| :---: | :---: | :---: | :---: | :---: |
| Package | $\theta \mathrm{Jc}$ | $\theta \mathrm{Jc}$ | $\theta \mathrm{JA}$ | $\theta \mathrm{JA}$ |
| POWER TAB | $7.5^{\circ} \mathrm{C} / \mathrm{W}$ | $11^{\circ} \mathrm{C} / \mathrm{W}$ | $75^{\circ} \mathrm{C} / \mathrm{W}$ | $80^{\circ} \mathrm{C} / \mathrm{W}$ |
| TO-3 | $4.0^{\circ} \mathrm{C} / \mathrm{W}$ | $6^{\circ} \mathrm{C} / \mathrm{W}$ | $44^{\circ} \mathrm{C} / \mathrm{W}$ | $47^{\circ} \mathrm{C} / \mathrm{W}$ |
| PD (MAX) | TJ (MAX | $-T_{A}$ or | $T J$ (MA | $-T_{A}$ |

(Without a heat sink)
$\theta \mathrm{CA}=\theta \mathrm{CS}+\theta_{\mathrm{SA}}$
Solving for $T_{J}: T_{J}=T_{A}+P_{D}\left(\theta_{J C}+\theta_{C A}\right)$ or $T_{A}+$ PDOJA (Without heat sink)

Where $\quad T_{J}=$ Junction Temperature
$\mathrm{T}_{\mathrm{A}}=$ Ambient Temperature
$P_{D}=$ Power Dissipation
$\theta_{\mathrm{J}-\mathrm{A}}=$ Junction to ambient thermal resistance
$\theta_{\mathrm{JC}}=$ Junction to case thermal resistance
$\theta \mathrm{CA}=$ Case to ambient thermal resistance
$\theta C s=$ Case to heat sink resistance $\theta S A=$ Heat sink to ambient thermal resistance



## TEST LOAD CIRCUITS



## TYPICAL APPLICATIONS FOR

 $\mu$ A78GIn many $\mu \mathrm{A} 78 \mathrm{G}$ applications, compensation capacitors may not be required. However, for stable operation of the regulator over all input voltage and output current ranges, bypassing of the input and output $(0.33 \mu \mathrm{~F}$ and $0.1 \mu \mathrm{~F}$, respectively) is recommended. Input bypassing is necessary if the regulator is located far from the filter capacitor of the power supply. Bypassing the output will improve the transient response of the regulator.


If load is not ground referenced, connect reverse biased diodes from outputs to ground.


POSITIVE 5 TO 30V ADJUSTABLE REGULATOR IOUT > 5.0A


NOTE: External series pass device is not short circuit protected.

POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR


OUTPUT WAVEFORM


## TYPICAL APPLICATIONS FOR $\mu$ A78G <br> (Cont'd)



## NE/SE5554 DUAL TRACKING <br> REGULATOR

The Signetics NE/SE5554 is a monolithic dual tracking regulator designed for use where dual supplies must track with close tolerances. It was designed with ease of production and high performance in mind. The intent was to supply a product which has performance surpassing its intended need and no additional features.

The device is composed of a negative, zener referenced regulator with an inverting amplifier-follower. The zener regulator has a zener controlled current source and a forward biased diode for temp. compensation. This classical reference was used for one main reason . . . simplicity. The main justification to use this is the devices intended use. Considering 4 basic contributors to output voltage change, (1) Line regulation, (2) Load regulation, (3) Temperature Coefficient, (4) Popcorn noise, all of these and combinations of them, are small considering the uses this device is intended for:

1. Op-Amp Supplies
2. Sense-Amp Supplies
3. Analog Signal Processors (Driver-Gates, Mpx, etc.)
4. MOS-LSI Systems
5. Communications Circuits

These applications all have excellent power supply rejection or limited need for very close control of slight variations on supply lines. In short, it is an attempt to supply a customer with a device designed for his uses, but not costing money for features he doesn't need.

Both actual regulators are differential amplifiers followed by a gain stage followed by a Darlington with current limit. The negative regulator is the complement of the positive with the exception that the output stage is a compound PNP. The 5554 is essentially a dual 78 M regulator.
The voltage dividers around the zener set
the actual reference at 5 volts and allow positive and negative output voltages to be programmed conveniently. The various resistor values available with metal mask options, allow many different output voltage options as well as externally controlling output voltages by programming resistors to +Vout, -Vout, control and null.

The output current limit of 200 mA was chosen as a compromise. The 100 mA limit of the 78LXX Family is only marginally useful for many systems, where 0.5 amp is too much dissipation for two regulators in a TO-5 package thus, the 200 mA limit.

The regulators were designed to be on-chip compensated so external capacitors are not

## MOTOR SPEED CONTROL



Use flyback diode across motor if necessary.
needed. This is a great advantage as most of the currently available devices require $10 \mu \mathrm{f}$ output capacitors or other cumbersome externally compensation.

The performance expectations reflect the intended use:

| Vout | Tolerance | $5 \%$ |
| :--- | :--- | :--- |
| Vout | Regulation | $1 \%$ |
|  | (Load \& Line) |  |
| Vout | Temp. Coefficient | $65 \mathrm{PPM} /{ }^{\circ} \mathrm{C}$ |
| VOUT | Noise | $100 \mu \mathrm{VRMS}$ |
|  |  | $10 \mathrm{~Hz}-10 \mathrm{kHz}$ |

The intended use being power supplies, not reference supplies. Most devices these regulators would be driving have excellent

power supply rejection, such as operational amplifiers, Analog switches, MOS logic, communication circuits, and will not be adversely affected by the output voltage tolerances, including noise and temperature coefficient.

The initial output voltages of the 5554 will track exactly but the absolute pos voltage will be different from the absolute neg voltage. This is due to small process variations in the internal balance resistors.

## NE/SE5554 DUAL TRACKING REGULATOR APPLICATION NOTE

For most applications, this difference is of no concern. For those applications where exact positive and negative voltages are necessary external balance potentiometer may be added as shown.


This output balance control may be used to change the positive regulated voltage from about 0.2 volts to $\geq 16$ volts without changing the negative regulated voltage.

To change the negative regulator voltage from its fixed value it is necessary to use the
control function. With zero resistance between the control pin and -Vout, the output will be $\pm 5.0$ volts. Increasing the resistance to 50 K will give full output. This control, in conjunction with the balance, can give output voltage of $\pm 5 \mathrm{~V}$ to about $\pm \mathrm{V} \mathrm{IN}-3$ volts.


In order to prevent instability in this circuit when the control resistance approaches zero ohms, it is necessary to use a filter
capacitor on -Vout of $0.1 \mu \mathrm{f}$ or larger to ground. $A^{-} 10 \mu$ from +VOUT and -VOUT to ground will improve transient response, where this is of concern.

## Increasing output above $\pm 15$ volts on NE/SE5554

To increase the regulated output above $\pm 15$ volts, it is necessary to trim the op amp negative input reference resistor ( $R_{1}$ in the NE/SE5554 equivalent circuit).


HIGH CURRENT DUAL TRACKING REGULATOR


## sECTION 22 InTERFACE CIRCUITS

## INTRODUCTION

Large systems are comprised of many different subsystems, all of which must interface to complete the system. All types of circuits, including linear, digital and discrete are often used in the subsystems.

Interface circuits provide the necessary function of tying the parts of a system together. These circuits are usually not purely linear or digital but contain both types of circuit functions. For instance, sense amplifiers are designed for interface between low level memory outputs and bipolar levels, while differential comparators are designed for interface between analog systems and TTL/DTL systems. In general, this section will cover such devices as comparators, sense amplifiers, line drivers/receivers, and display drivers.

## CONVERTERS

Digital computers, digital communications, digital instruments and displays have created a demand for low cost reliable converters. Key factors in this demand are:

- The need to communicate with digital computers for processing and storage of analog signals.
- Severe limitations encountered in reliable analog data transmission over any considerable distance.
- The need for more easily readable displays.

General application areas for converters include: Data processing, data transmission, graphics and displays, audio systems, control systems and arithmetic operations.

## Specific Applications

## Test Systems

- Transistor tester (Force $\mathrm{I}_{\mathrm{B}}$ and $\mathrm{I}_{\mathrm{C}}$ )
- Resistor matching (Use both outputs)
- Programmable power supplies
- Programmable pulse generators
- Programmable current source
- Function generators (ROM drive)


## Arithmetic Operations

- Analog division by a digital word
- Analog quotient of 2 digital words
- Analog product of 2 digital wordssquaring
- Addition and subtraction with analog output
- Magnitude comparison of 2 digital words
- Digital quotient of 2 analog variables
- Arithmetic operations with words from different logic families


## Graphics and Displays

- Polar to rectangular conversion
- CRT character generation
- Chart recorder driver
- CRT display driver


## Data Transmission

- Modern transmitter
- Differential line driver
- Party line multiplexing of analog signals
- Multi-level 2-wire data transmission
- Secure communications (constant power dissipation)


## Control Systems

- Reference level generator for setpoint controllers
- Positive peak detector
- Negative peak detector
- Disc drive head positioner
- Microfilm head positioner


## Audio Systems

- Digital AVC and reverberation
- Music distribution
- Organ tone generator
- Audio tracking A/D
- Speech compression and expansion
- Audio digitizing and decoding


## D/A CONVERTERS

D/A converters perform the function of converting a digitally coded signal input into an analog signal output (See Figure 51). D/A converters are useful in systems requiring analog signals derived from digital data.

## DAC Bullding Blocks

The actual implementation of a D/A system contains four separate parts: A reference

CONVERSION OF A DIGITALLY CODED SIGNAL INPUT INTO AN ANALOG SIGNAL OUTPUT


Output $=$ Ref. $\mathbf{x}$ digital word
Output $=$ Ref. $\times\left(\frac{B_{1}}{2}+\frac{B_{2}}{4}+\ldots+\frac{B_{N}}{2 N}\right)$
Figure 5-1
quantity; a set of binary switches to simulate binary coefficients $\mathrm{B}_{1}$. . . $\mathrm{B}_{\mathrm{N}}$; a weighting network; and an output summing means.

## Binary-Weighted Ladder Employing Voltage Switching

The disadvantages of a binary-weighted ladder employing voltage switching include: A wide range of resistor values which are used in weighting the network; and nodal capacitances which are charged/discharged during conversion. See Figure 5-2.

## R-2R Ladder Network Employing Current Switching

The advantages of this type of network include: No need for a wide range of resistor

values; and current switching eliminates transients in nodal parasite capacitances. See Figure 5-3.

## KEY SPECIFICATIONS

## Speed

The conversion process should represent the input signal with the highest fidelity and minimal lag in time (Real time applications).

## Settling Time

Settling time is a measure of a converter's speed and is defined as the elapsed time after a code transition for DAC output to reach final value within specified limits, usually $\pm 1 / 2$ L.S.B. See Figure 5-5.

## Errors

Offset Error -The output voltage of DAC with zero code input. Offset can and usually is trimmed to zero with an offset zero adjust potentiometer. See Figure 5-6.


## DAC OUTPUT TYPES


a. True Current Output/Voltage Output
resistive output


LItTLE OR NO OUTPUT VOLTAGE COMPLIANCE

c. Complementary High Compliance Current Switch
b. Resistive Output

Figure 5-4


Gain Error - Deviation in output voltage from correct level when the input calls for a full scale output. This error may be trimmed to zero. See Figure 5-7.

Relative Accuracy - The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale (1 L.S.B.). See Figure 5-8.
Differential
Non-Linearity - Incremental error from any ideal L.S.B. analog output change when the digital input is changed (1 L.S.B.). See Figure 5-9.

Monotonicity - As the input code is incre-



Figure 5-6

## Stability

Stability is a measure of the independence of converter parameters with respect to variations in external conditions such as temperature and supply voltage.

## Temperature

Coefficient -The effects of temperature

## Supply

Rejection
mented from one code to the next in sequence, the analog output will either increase or remain constant. See Figure 5-10.

> changes of the output. Specified as \%F.S. change.
-Ability to resist changes in the output with supply changes, specified as \% full scale change.



| PARAMETER | $\begin{gathered} \text { MC140 } \\ \text { 6/7/8 } \end{gathered}$ | NE5008 | NE5009 | UNITS |
| :---: | :---: | :---: | :---: | :---: |
| Resolution | 8 | 8 | 8 | Bits |
| Relative | .78/.39/ | 0.19 | 0.1 | \% |
| accuracy | . 19 |  |  |  |
| Settling time | 300 | 85 | 60 | ns |

Table 5-1

## D/A CONVERTER COMPARISON

## 5007/5008 DAC

## Reference Amplifier Setup

The 5007/5008 is a multiplying D-to-A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0 mA . The full scale output current is a


Figure 5-10
linear function of the reference current and is given by this equation where $I_{\text {REF }}=I_{14}$.

$$
I_{F S}=\frac{255}{256} \cdot I_{\text {REF }}
$$

In positive reference applications shown in Figure 5-11, an external positive reference voltage forces current through R14 into the $\mathrm{V}_{\text {REF }}(+$ ) terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $\mathrm{V}_{\text {REF }}(-)$ at pin 15 , shown in Figure 5-12. Reference current flows from ground through R14 into $V_{\text {REF }}(+)$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.
Bipolar references may be accommodated by offsetting $V_{\text {REF }}$ or pin 15 as shown in Figure 5-13. The negative common mode range of the reference amplifier is given by the following equation. The positive common mode range is $\mathrm{V}+$ less 1.5 V .

$$
V_{C M}-=V_{-}+\left(I_{\text {REF }} \cdot 1 \mathrm{k} \Omega\right)+2.5 \mathrm{~V}
$$

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0 V TTL logic supply is not recommended as a reference. If a regulated power supply is
used as a reference R14 should be split into 2 resistors with the junction bypassed to ground with a $0.1 \mu \mathrm{~F}$ capacitor.

For most applications, $a+10.0 \mathrm{~V}$ reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier Vos and TCVos. For most applications the tight relationship between IREF and IFS will eliminate the need for trimming IREF. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in Figure 5-14.
Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a dc reference current is +0.2 mA to +4.0 mA .
The reference amplifier must be compensated by using a capacitor from pin 16 to V -. For fixed reference operation, a $0.01 \mu \mathrm{~F}$ capacitor is recommended. For variable reference applications, see section entitled Reference Amplifier Compensation for Multiplying Applications.

## Multiplying Operation

The 5007/5008 provides excellent multiplying performance with an extremely linear


Figure 5-11

$I_{\text {REF }} \geq$ Peak Negative Swing of $l_{\text {IN }}$

$+V_{\text {REF }}$ must be above Peak Positive Swing of $V_{I N}$

Figure 5-13

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT


Figure 5-14
relationship between Ifs and IREF over a range of 4 mA to $4 \mu \mathrm{~A}$. Monotonic operation is maintained over a typical range of $I_{\text {REF }}$ from $100 \mu \mathrm{~A}$ to 4.0 mA . Consult the factory for devices selected for monotonic operation over wider I ReF ranges. For better multiplying accuracy see the 5009 data sheet.

## Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V -. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and $5.0 \mathrm{k} \Omega$, minimum values of Cc are 15 , 37 and 75pF. Larger values of R14 require proportionately increased values of Cc for proper phase margin.

## PULSED REFERENCE OPERATION



Figure 5-15

For fastest multiplying response, low values of R14 enabling small $\mathrm{C}_{\mathrm{C}}$ values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For $\mathrm{R} 14=1 \mathrm{k} \Omega$ and $\mathrm{C}_{\mathrm{C}}=15 \mathrm{pF}$, the reference amplifier slews at $4 \mathrm{~mA} / \mu \mathrm{s}$ enabling a transition from $I_{\text {REF }}=0$ to $I_{\text {REF }}=$ 2 mA in 500 ns .
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5-15. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ( l REF $=0$ ) condition. Full scale transition ( 0 to 2 mA ) occurs in 120ns when the equivalent impedance at pin 14 is $200 \Omega$ and $\mathrm{C}_{\mathrm{C}}=0$. This yields a reference slew rate of $16 \mathrm{~mA} / \mu \mathrm{s}$, which is relatively independent of RIN and $\mathrm{V}_{\mathrm{IN}}$ values.


Figure 5-16

## Logic Inputs

The 5007/5008 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, $2 \mu \mathrm{~A}$ logic input current and completely adjustable logic threshold voltage. For $\mathrm{V}-=-15 \mathrm{~V}$, the logic inputs may swing between -10 V and +18 V . This enables direct interface with +15 V CMOS logic, even when the $5007 / 5008$ is powered from a +5 V sup-
ply. Minimum input logic swing and minimum logic threshold voltage are given by this equation.

$$
\mathrm{V}-+\left(I_{\text {REF }} \cdot 1 \mathrm{k} \Omega\right)+2.5 \mathrm{~V}
$$

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control in (pin 1, $\mathrm{V}_{\mathrm{LC}}$ ). Figure 5-16 shows the relationship between $V_{L C}$ and $V_{T H}$ over the temperature range, with $\mathrm{V}_{\text {TH }}$ nominally 1.4 above $\mathrm{V}_{\mathrm{LC}}$. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an IreF $=1 \mathrm{~mA}$ is recommended. For interfacing other logic families, see Figure 5-17. For general setup of the logic control circuit, it should be noted that pin 1 may source up to $200 \mu \mathrm{~A}$. External circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a $1 \mathrm{k} \Omega$ divider, for example, it should be bypassed to ground by a $0.01 \mu \mathrm{~F}$ capacitor.

## Analog Output Currents

Both true and complemented output sink currents are provided, where $\mathrm{I}_{0}+\mathrm{T}_{\mathrm{O}}=\mathrm{I}_{\text {Fs }}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is

## INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTE
Do not exceed negative logic input range of DAC

Figure 5-17
applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases lo as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing Ifs. Do not leave an unused output pin open.
Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36 V above V and is independent of the positive supply. Negative compliance is given by this equation.

$$
V-+\left(I_{\text {REF }} \cdot 1 \mathrm{k} \Omega\right)+2.5 \mathrm{~V}
$$

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

## Power Supplies

The 5007/5008 operate over a wide range of power supply voltages from a total supply of 9 V to 36 V . When operating at supplies of $\pm 5 \mathrm{~V}$ or less, $\mathrm{I}_{\mathrm{ref}} \leq 1 \mathrm{~mA}$ is recommended.

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at -4.5 V with $I_{\text {REF }}=$ 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8 V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the 5007/5008 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.
Power consumption may be calculated by this equation.

$$
\left.P_{D}=(I+)(V+)+(I+)(V-)+(2)_{\text {REF }}\right)(V-)
$$

A useful feature of the 5007/5008 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

## Temperature Performance

The linearity and monotonicity specifications of the 5007/5008 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is low, typically $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$, with zero scale output current and drift essentially negligible compared to $1 / 2$ LSB.

Full scale output drift performance will be best with +10.0 V references, as Vos and TCVos of the reference amplifier will be very small compared to 10.0 V . The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift. Settling times of the 5007/5008 decrease approximately $10 \%$ at $-55^{\circ} \mathrm{C}$ and an increase of about $15 \%$ at $+125^{\circ} \mathrm{C}$ is typical.

## Settling Time

The $5007 / 5008$ is capable of extremely fast settling times (typically 85ns at lReF $=$ 2.0 mA ). Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 ns for each of the 8 bits. Settling time to within $1 / 2$ LSB of the LSB is therefore 35 ns , with each progressively larger bit taking successively
longer. The MSB settles in 85 ns , thus determining the overall settling time of 85 ns . Settling to 6-bit accuracy requires about 65 to 70 ns. The output capacitance of the 5007/5008 including the package is approximately 15 pF . Therefore the output RC time constant dominates settling time if RL > $500 \Omega$.
Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for IREF values down to 1.0 mA , with gradual increases for lower I IREF values. The principal advantage of higher I IREF values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 4 \mu \mathrm{~A}$. Therefore a $1 \mathrm{k} \Omega$ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 5-18 uses a cascode design to permit driving a $1 \mathrm{k} \Omega$ load with less than 5 pF of parasitic capacitance at the measurement node. At IREF values of less than 1.0 mA , excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000


Figure 5-18
provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within $\pm 0.2 \%$ of the final value; thus, settling time may be observed at lower values of I REF.
The 5007/5008 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and VLC terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. $0.1 \mu \mathrm{~F}$ capacitors at the supply pins provide full transient performance.

## TYPICAL APPLICATIONS

## BASIC UNIPOLAR NEGATIVE OPERATION



|  | $\mathbf{B}_{\mathbf{1}}$ | $\mathbf{B}_{\mathbf{2}}$ | $\mathbf{B}_{\mathbf{3}}$ | $\mathbf{B}_{\mathbf{4}}$ | $\mathbf{B}_{\mathbf{5}}$ | $\mathbf{B}_{\mathbf{6}}$ | $\mathbf{B}_{\mathbf{7}}$ | $\mathbf{B}_{\mathbf{8}}$ | $\mathbf{I}_{\mathbf{O}}^{\mathbf{m A}}$ | $\overline{\mathbf{I}}_{\mathbf{0}} \mathbf{m A}_{\mathbf{a}}$ | $\mathbf{E}_{\mathbf{O}}$ | $\overline{\mathbf{E}_{\mathbf{O}}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Full scale | 1 | 1 | 1 | $\mathbf{1}$ | 1 | 1 | 1 | 1 | 1.992 | 000 | -9.960 | .000 |
| Full scale - LSB | 1 | 1 | 1 | $\mathbf{1}$ | 1 | 1 | 1 | 0 | 1.984 | .008 | -9.920 | -.040 |
| Half scale + LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.008 | .984 | -5.040 | -4.920 |
| Half scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.000 | .992 | -5.000 | -4.960 |
| Half scale - LSB | 0 | 1 | 1 | $\mathbf{1}$ | 1 | 1 | 1 | 1 | .992 | 1.000 | -4.960 | -5.000 |
| Zero scale + LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | .008 | 1.984 | -.040 | -9.920 |
| Zero scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | .000 | 1.992 | .000 | -9.960 |

Figure 5-19

## BASIC BIPOLAR OUTPUT OPERATION



|  | $\mathbf{B}_{\mathbf{1}}$ | $\mathbf{B}_{\mathbf{2}}$ | $\mathbf{B}_{\mathbf{3}}$ | $\mathbf{B}_{\mathbf{4}}$ | $\mathbf{B}_{\mathbf{5}}$ | $\mathbf{B}_{\mathbf{6}}$ | $\mathbf{B}_{\mathbf{7}}$ | $\mathbf{B}_{\mathbf{8}}$ | $\mathbf{E}_{\mathbf{0}}$ | $\overline{\mathbf{E}_{\mathbf{0}}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| POS full scale | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -9.920 | +10.000 |
| POS full scale - LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -9.840 | +9.920 |
| Zero scale + LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -0.080 | +0.160 |
| Zero scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | +0.080 |
| Zero scale - LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +0.080 | 0.000 |
| Neg full scale + LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +9.920 | -9.840 |
| Neg full scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +10.000 | -9.920 |

Figure 5-20

TYPICAL APPLICATIONS (Cont'd)
SYMMETRICAL OFFSET BINARY OPERATION


|  | $\mathbf{B}_{\mathbf{1}}$ | $\mathbf{B}_{\mathbf{2}}$ | $\mathbf{B}_{\mathbf{3}}$ | $\mathbf{B}_{\mathbf{4}}$ | $\mathbf{B}_{\mathbf{5}}$ | $\mathbf{B}_{\mathbf{6}}$ | $\mathbf{B}_{\mathbf{7}}$ | $\mathbf{B}_{\mathbf{8}}$ | $\mathbf{E}_{\mathbf{0}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| POS full scale | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +9.920 |
| POS full scale - LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | +9.840 |
| (+) Zero scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +0.040 |
| (-) Zero scale | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -0.040 |
| Neg full scale + LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -9.840 |
| Neg full scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -9.920 |

Figure 5-21

POSITIVE LOW IMPEDANCE OUTPUT OPERATION


For complementary output (operation as negative logic DAC), connect inverting input of OP-amp to lo (pin 2), connect lo (pin 4) to ground.

Figure 5-22

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


For complementary output (operation as a negative logic DAC), connect noninverting input of OP-amp to lo (pin 2); connect lo (pin 4) to ground.

Figure 5-23

LOW COST 8-BIT 1 MICROSECOND A-TO-D CONVERTER


Figure 5-24


Figure 5-25

DC-COUPLED DIGITAL ATTENUATOR/ PROGRAMMABLE GAIN AMPLIFIER


Bipolar input offset Performs 2 quadrant
multiplications-AC input
controls output polarity.

NOTES

1. $\mathrm{R} 1=\mathrm{R} 2=\mathrm{R} 3$
2. $\mathrm{R} 4=\mathrm{R} 5$
3. Eo DC to $20 \mathrm{KHz}= \pm 5 \mathrm{~V}$
4. EO $D C$ to $10 \mathrm{KHz}= \pm 10 \mathrm{~V}$

Figure 5-27


Figure 5-26


## A/D CONVERTER CIRCUITS

Conversion schemes usually fall into one of two categories:

D/A Feedback A/D Converters
a. Digital ramp (Counting)
b. Tracking (Up-down)
c. Successive approximation*

## Integrating A/D Converters

a. Single slope
b. Double slope
c. Triple slope*

## Indirect Schemes

## Feedback Methods

- Very fast
- Accurate
- Good differential linearity
- Constant conversion time


## Integrating Methods

- Slow conversion time
- Accurate
- Excellent differential linearity
- Excellent rejection of high frequency noise
- Fixed averaging period, but variable conversion time


## CONSIDERATIONS FOR <br> A/D CONVERTERS

- Analog input signal range and resolution required
- Linearity requirement and stability
- Conversion speed required
- Monotonicity requirement: Can missing codes be tolerated?
- Character of input signal: Is it noisy, sampled, filtered, slowly varying?
- Transfer characteristics (Type of coding)


## A/D CONVERTER TERMS

## Resolution

Resolution is the input change required to increment the output between the two adjacent codes. This term also refers to the number of bits in the output word and; hence, the number of discrete output codes the input analog signal can be broken into. Expressed in "bits" resolution.

## Transfer Characteristic

The Transfer Characteristic is the relationship of the output digital word (code) to the input analog signal, i.e., Binary, BCD.

## Conversion Speed

The Conversion Speed is the speed at which an ADC can make repetitive data conversions.

## Quantizing Error

Quantizing Error is an inherent error in the conversion process due to finite resolution (discrete output). See Figure 5-29.

## Offset Error

An Offset Error is shown in Figure 5-30.

## Gain Error

A Gain Error is shown in Figure 5-31.

## Relative Accuracy

Relative Accuracy is the deviation of an actual bit transition from the ideal transition value at any level over the range of the ADC (\% F.S.). See Figure 5-32.


Figure 5-30


Figure 5-31


Figure 5-32

## Hysteresis Error

A Hysteresis Error is the code transition voltage dependence relative to the direction from which the transition is approached.

## Monotonicity

Monotonicity is when the output code either increases or remains the same for increasing analog input signals. The opposite is true in the reverse direction.

## Missing Codes

A Missing Code is a code combination that is skipped. See Figure 5-33.
*Converter schemes used at Signetics


Figure 5-33

## INTRODUCTION

The advent of MSI digital logic has made feasible the digital display at a reasonable cost with virtually all instrumentation now taking that course. The key features of digital displays are ease of readability and high reliability.

## SEVEN SEGMENT DISPLAYS

Seven segment displays are used for many types of applications. These applications include:

## Instruments (Industrial)

- Voltmeters
- Frequency Counters
- Digital Thermometers
- Medical Equipment
- Process Control Equipment
- Avionic Displays


## EDP and Minicomputer

- POS Terminals
- Calculators
- Misc. EDP Peripheral Equipment, e.g., Tape Drivers
- Accounting Machines


## Consumer

- Automotive-Dashboard Indicators
- Appliances-Ranges, Clocks
- Audio-Digital Tuning
- Games

The most popular and commonly used of the various display technologies are:

- Liquid Crystal Displays (LCD)
- Light-Emitting Diodes (LED)
- Gas-Discharge
- Fluorescent
- Incandescent

The choice of which technology to be used is often dictated by the system constraints, such as:

- Cost
- Size
- Readability (Ambient light)
- Operating Temperature Range
- Reliability
- Power and Supply Limitations
- Ability to be Multiplexed


## LIGHT-EMITTING DIODES (LEDs)

LED displays have taken over an appreciable part of the display market, primarily due to:

- High Reliability
- Long Life
- Fast Response Time
- Low Operating Voltage
- Ease in Interfacing


## GAS DISCHARGE DISPLAYS

Gas discharge displays have several advantages over LEDs, LCDs and other displays in the applications area. These advantages are generally in products where performance, rather than cost, is of prime importance. These advantages include:

- Larger Digits
- Increased Readability in Bright, Ambient Light
- High Reliability
- Operation in Wide Temperature Extremes


## Applications for Gas Discharge Displays

## Automotive Industry

- Operating temperature range $\left(-40^{\circ} \mathrm{F}\right.$ to $+120^{\circ} \mathrm{F}$ )
- LCDs-Freeze at lower temperature
- LEDs-Poor efficiencies at high temperature


## Avionics

- Visibility
- LCDs-Difficult to multiplex (Poor response)
Poor operating temperature range
Need direct light
- LEDs-Poor visibility in bright light


## Games

- Size and Brightness
- LCDs-Poor viewing angle
- LEDs-Not bright enough


## NE580 BAR GRAPH DRIVER

## Bar-graph System Operation

The bar-graph display is a thick-film planar, gas discharge device. The principal of operation is called self-scan ${ }^{(m)}$, in which a neon glow-discharge is propagated from one cathode spot to another under one anode. The bar-graph device appears as a series of cathode bars arranged in a column. A glow discharge is continually propagated along the column from a keep-alive cathode at one end. Provided the scan rate for a whole column is above the eye flicker detection rate, then the glow appears as a continuous column of light.

## Bar-graph Signal Requirements

The NE580 comprises most of the electronic components necessary to interface an analog voltage level to the bar-graph display. Each column of the display requires an anode control signal and each cathode (usually from 4 to 7 in number) requires an interlaced logic signal of $1 / \mathrm{N}$ duty cycle (where $N$ is the number of cathode phases). The pulse width of each cathode signal is of the order of 50 to $100 \mu \mathrm{~s}$. The cathode signals clock continuously throughout the frame period. The anode signal is on only for a proportion of time corresponding to the input voltage.
Thus $\quad V_{I N}=V_{\text {REF }} \times \frac{T_{A N}}{200}$
for a 200 element device, where $T_{A N}$ is the number of cathode clock cycles for which the anode is on Figure 5-35 illustrates the relative output phasing of the linear ramp cathode and anode lines for 5 phase operation.

## Circuit Operation

The NE580 provides the circuitry to generate all these signals to the point where they drive the high voltage display elements. An on-chip clock generator drives the master counter and cathode phase generator.
The clock also gates a constant current source which charges the ramp capacitor with a staircase waveform of equal increment steps. These steps correspond to the cathode segments. There are two steps per


Figure 5-35


Figure 5-36
segment so that the comparison of input voltage with respect to the ramp is made at the mid-point of each segment. The master counter inhibits the current source and discharges the ramp after 200 cathode counts. At the 200 th count, the ramp voltage is strobed into a sample-and-hold amplifier. This voltage is compared with the reference voltage and a signal fed back to the ramp constant current source. Hence, the maximum value of the ramp will be adjusted to the same level as the reference voltage.

## NE584/585 GAS DISCHARGE DISPLAY DRIVERS

## Introduction

The NE584 and NE585 Gas Discharge Display Drivers find wide application in driving displays such as Burroughs Panaplex II, Cherry Plasma-Lux, Beckman SP, etc. They feature high reliability, simplicity in interfacing, programmable segment current,
and internal feedback. External components required include a resistor used in programming the segment currents, and a capacitor used in limiting anode bus voltage variations. The purpose of this application note is to supply the designer with the information necessary to design systems based on these drivers.

## Selection of Program Current Resistor

The NE584, available in either an eight or nine channel unit, drives the cathodes of the displays. Segment drive current, a factor in determining the brightness of the display, is set on all channel outputs simultaneously by selection of a single resistor.

Currents may be programmed up to 3 mA (in the internal feedback mode) and up to 5 mA (when using external feedback or no feedback). Component values may be selected using Figure 5-37.

## Selection of Feedback Capacitor

The NE584 and NE585 may be operated with or without feedback. The feedback mode may be controlled internally or externally. When using external feedback current, capabilities of the drivers are extended as a result of eliminating the power dissipation in the internal feedback network which is a current limiting factor. Also certain system timing conditions may make it necessary to operate in this mode because of improper feedback operation. Operating in the feedback mode offers consistency of operation under conditions such as supply voltage variations, temperature variations blanked leading zeros, variations in display panel ionization voltage, component tolerances, etc.

When operating in the feedback mode, a capacitor is required to limit variations on the anode bus. This prevents the cathode

output from going into saturation causing feedback current to flow and anode bus voltages to be higher than required. Selection of this capacitor is mainly determined by the cathode pulse width and by the segment currents and may be selected using Figure 5-38.

## Interface Considerations Input Requirements

Driver inputs may be directly interfaced with TTL, MOS, and C-MOS logic families. Each of these logic families will provide enough drive to fully enable the driver outputs.
Unused inputs should not be grounded. They should be left open to prevent loading of selected inputs.

## Single Supply Operation

Because of the increased external component count, single supply operation is usu-

## feedback capacitor valves



Figure 5-38
ally not recommended. If it is necessary to operate in this mode, all voltage levels must be shifted by $1 / 2$ the supply voltage. For example:

| PIN | Split Supply <br> $\pm \mathbf{1 0 0}$ volts | Single Supply <br> $+\mathbf{2 0 0}$ volts |
| :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | 5 to 15 volts | 105 to 115 volts |
| $\mathrm{V}_{2}$ | -100 volts | 0 volts |
| $\mathrm{V}_{3}$ | +100 volts | +200 volts |
| GND | 0 volts | +100 volts |

The input levels must also be shifted. One method of accomplishing this is shown in Figure 5-39.


## Pull-Up Option

When operating the drivers at fast scanning rates, the turn-off time of the display may become a limiting factor. This may become noticeable when operating with a 5 volt supply ( $\mathrm{V}_{1}$ ).
The pull-up option is provided on the segment driver and is used to decrease turn-off delays by allowing charge to be removed more quickly from the cathodes and from stray capacitance. This is accomplished by grounding this pin, which increases the drive current to the pull-up network.

## Cathode Pull-Up Resistors

When driving long cables, it is helpful, as with all drivers, to add an external pull-up resistor from the output of the cathode driver to ground. The value of this resistor is in the range of 1 Meg , placed close to the display, and allows charge to be removed more rapidly from both the display and from the cable.

## Timing Considerations and Feedback

A number of system requirements and panel parameters must be considered in making a decision as to what constraints should be imposed on cathode and anode signals and on selecting the frame rate. The two driver modes of operation require different timing constraints-each mode offering its own unique advantages. Feedback ModeVariations in both ionization voltages from panel-to-panel as well as from digit-to-digit within the same panel and in the supply voltages, make it advantageous to float the anode bus and make it self compensating for such variations. This is accomplished by the use of a current feedback scheme and imposes constraints on both the duration and relative timing of the driver input signals.
The feedback scheme is relatively simplewhenever an input is applied to the cathode driver and the display has not yet ionized the coincidence of this condition is sensed by the cathode driver and a current pulse is sent along the feedback link to the digit driver. The amplitude of this pulse is proportional to the program current and to the number of segment inputs selected. Its duration is equal to the ionization time or to the duration of the segment pulse input-the shorter of the two. This current pulse is sensed by the digit driver, amplified, and is used to charge the feedback capacitor. This results in an increase in the voltage level of the anode bus.
Once the display is ionized, a current must be supplied by the anode bus for the duration of the cathode input. The cathode driver, which functions as a constant current sink, senses this current and terminates the feedback current pulse. Once feedback current has ceased, the feedback capacitor begins to discharge lowering the anode bus voltage. The average voltage level on the anode bus is stabilized when the charge entering the anode bus during the ionization time equals the charge leaving the bus during on-time of the display, cathode pulse duration minus the ionization time. This level is defined by the supply voltage and display panel parameters and is self compensating since the anode bus voltage is directly related to the ionization time and the ionization time inversely related to the anode bus voltage.

The following constraints are unique to the feedback mode of operation.
1-a A digit input should always be selected before or at the same time that one or more segment inputs are selected and remain on for the duration of the segment inputs or longer.

## TYPICAL APPLICATIONS



Figure 5-40

## MULTIPLE ANODE DRIVER SINGLE CATHODE DRIVER



## NOTES

(a) Digits are multiplexed (only one digit on at any given time)
(b) Feedback pins are connected together.
(c) Anode bus pins are connected together and a single feedback capacitor used.
(d) Max segment current should be limited to 5 mA .
(e) If displays with different parameters are used, it may be necessary to operate the system in the non-feedback mode. This may be accomplished by leaving all feedback pins open connecting the anode bus pins together and connecting a single zener diode of the proper power and current rating to the $-\mathrm{V}_{3}(+100$ volts) supply.

## NON-FEEDBACK MODE



NOTES
(a) Feedback pins left open.
(b) Segment current set by Rp and limited to 5 mA .
(c) Anode bus connectd to $\mathrm{V}_{3}$ supply ( +100 volts) through zener diode ( $15-20$ volt range) and maintains anode bus at a constant voltage.

Figure 5-41


NOTES
(a) Displays are multiplexed in parallel. (Each anode driver output selects two digitsone from each display)
(b) Segment currents may be set independently by RP1 and RP2 and the total should not exceed 5 mA .
(c) All feedback pins are left open.
(d) Anode bus pin connected to the $\mathrm{V}_{3}$ supply ( +100 V ) through a zener diode 20 volt ( $15-20$ volt range) and maintains a constant voltage as the anode voltage.

1-b Blanking should be accomplished by inhibiting segment inputs or both segment and digit inputs.
2. For large cathode pulse widths combined with high segment currents, it is recommended that the non-feedback mode be used a result of limitations on the magnitude of the feedback current and on power dissipation. If any of the constraints are not met, then the nonfeedback mode of operation should be used.

The following constraints are common to both modes of operation.

1. Adequate blanking should be used when scanning digits sequentially to inhibit adjacent digit arcing. Interlacing of digits may be used to eliminate the necessity for such blanking, but this in many cases will require a greater amount of hardware. Typical blanking time would range between $10-20 \%$ of total digit time.
2. Minimum pulse widths for the segment inputs should be typically greater than $200 \mu$ s so that variations in ionization time do not cause brightness variations in displays.
3. Scanning rate should be greater than 50 Hz to prevent flickering of display.
4. Brightness of the display is directly proportional to the segment current level and to the cathode input pulse width. Typically, the brightness may be varied over a $3: 1$ range by variation of segment current and over a 10:1 range by variation of cathode pulse width. Both ranges are dependent on display parameters.

## CONCLUSION

The switching of the high voltages necessary for display panels has long presented difficulties to the semiconductor industryparticularly to the IC manufacturers. Signetics now makes available a driver set capable of switching these high voltages with high reliability and ease in interfacing. Flexibility in configuring systems and small external component count, together with internal feedback and programmable segment current capabilities is why Signetics drivers find such wide applications in terminals, calculators, clocks, electronic games, instrument, cash registers, and medical equipment.

## MULTIPLE ANODE AND CATHODE DRIVER CONFIGURATION



NOTES
(a) Extension to the concepts presented in Figure 5-42 and 5-43. Non-feedback mode employed.
(b) Segment currents independently set and their sum limited to 5 mA

Figure 5-44

## APPENDIX A



## APPENDIX B

## NE584/585 Digital Clock Application

The system operates in the non-feedback mode. A 15 V zener diode maintains the anode bus at +85 volts which allows for variations in display panel ionization voltage. Display segment current is programmed by R1 and is set at 5 mA to allow maximum brightness. No other external components are required for interfacing.

## DESCRIPTION OF OPERATION

A three position brightness control is provided as well as a blanking switch. When in the blanking mode of operation the clock operates in a normal manner, but the display is blanked. Controls are provided for setting the time. The hours digit will be advanced by depressing S2. Minutes may be advanced in ten minute increments by depressing S3 and in one minute increments by depressing S2 and S3 simultaneously. A count inhibit switch is also provided which will allow setting of seconds.
A snooze alarm feature may be added by adding additional switches which allow the following pins in the Mostek chip to be connected to +15 volts. Pin (12) alarm enable, Pin (15) alarm set, Pin (11) snooze. In the alarm set mode the alarm time is displayed and may be set. The snooze feature will temporarily turn off an activated alarm for ten minutes.
An output tone, available at Pin (13), is in the range between $400-600 \mathrm{~Hz}$ and when buffered is used to drive a speaker.

## PARALLEL INPUT DIGIT DRIVER OUTPUTS



NOTES
(a) Corresponding inputs and outputs on each digit driver are connected together directly.
(b) Non-feedback mode is used
(c) Max segment current should be limited to 5 mA on each cathode driver and digit current limited to 60 mA where $\mathrm{I}_{\mathrm{D}}=\Sigma \mathrm{I} \mathrm{I}_{\mathrm{s}}$
(d) Separate zener diodes may be used to decrease power ratings, but a single diode may also be used and the anode bus pins tied together.
(e) Extended current capability of the 585 is increased to 60 mA .

Figure 5-45

## COMPARATORS

Voltage comparators are high gain differential input-logic output devices. They are specifically designed for open loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function of Figure 5-49. As shown device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input. The threshold in this example is 0 volts.
Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example the circuit of Figure 550 produces a logic 1 level when the noninverting input is more positive than the reference voltage.

## DEFINITIONS

Many similarities exist between operational amplifiers and the amplifier section of voltage comparators. In fact op amps can be
used to implement the comparator function at low frequencies.
Thus, the characteristic definitions presented here are similar to those reviewed for op amps in Section 3.

## Input Offset Voltage

As with operational amplifiers the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the dc voltage required at the input to force the output to the logic threshold of ensuing devices ( 1.2 volts for TTL).

## Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

## Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Hence, the average input current required defines bias current.

## Common Mode Range

When specifying voltage comparators one of the key parameters is common mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common mode signals at threshold. All ranges of input signals thus must be within the common mode range of the input amplifier.

## Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general higher gains would be advantageous for resolving smaller input signals. Of course the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000 volts per volt. This gain provides 5 volts of output swing with 1 mV



Figure 5-48
input signal change for reasonable accuracy but does not contribute severely to the overload recovery delay.

## Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the


Figure 5-49
analog signal in the meantime has changed value. At low frequencies the delay is of small consequence but at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes as a prime goal, the minimizing of transit times.

Propagation delay testing is done under worst case conditions. The recovery from saturation varies depending upon the initial state of the amplifier and the overdrive. Worst case conditions begin applying a 100 mV signal on the reference terminal. With no signal applied the amplifier is in saturation in one direction. A step input pulse on the signal line of $100 \mathrm{mV} \pm \mathrm{Vos}_{\text {s }}$ will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 5-51. The input is a step function of 100 mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst case propagation delay. Note that larger overdrive improves delay time as can be seen in Figure 5-52. An overdrive of 5 mV causes 12 ns delay, whereas a 100 mV overdrive improves transit time to only 6 ns .

## BASIC COMPARATOR CIRCUIT



Figure 5-50

If the measurement were made without initial saturation (less than 100 mV V threshold) the delay time would be smaller, due to the smaller storage times of unsaturated transistors.

## STATE-OF-THE-ART

Comparator design has always been optimized for four basic parameters. They are:

1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately these four parameters are not compatible. For instance gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that comparators such as the 526 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately the transistor beta is adversely affected by gold causing slightly higher bias and offset currents.


It was not until the advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky barrier diode's (SBD) location is illustrated in Figure 5-53.

The Schottky clamped transistor is formed by parallelling the Schottky diode with the base-collector junction of the npn transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter

## RESPONSE TIME FOR NE/SE521 COMPARATOR FOR VARIOUS input overdrives



Figure 5-52
voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4 volts-less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction. The Schottky diode becomes forward biased when the collector voltage falls 0.4 volts below the base voltage. Excess base drive is then shunted into the collector circuit prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

A cross sectional area of the Schottky diode is shown in Figure 5-54.


Figure 5-53

## SCHOTTKY CLAMPED TRANSISTOR GEOMETRY



Figure 5-54

## COMPARING THE COMPARATORS

Presently available comparator ICs range from the ultra fast 521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Often times speed of conversion is of primary importance to minimize pulse position errors of high frequency signals. At other times the parameters are much less stringent allowing the use of a general purpose comparator.

A handy reference guide to the major parameters is summarized in Table 5-3. At a glance the necessary parameters can be chosen to select the proper device.

## 521/522 Comparators

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.
Processed with state-of-the-art Schottky barrier diodes the 521/522 series devices provide good input characteristics while providing the fastest analog to TTL conversion to date. Total delay from input to output is typically 6 ns with a guaranteed speed of 12 ns . Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The 522, although sacrificing some speed, features open collector outputs for party line or wired-OR configurations for additional system flexibility.

| Device | Propagation <br> Delay (ns) | Vos <br> $(\mathbf{m V})$ | Ios <br> $(\mu \mathbf{A})$ | Ibias <br> $(\mu \mathbf{A})$ | Gain | CMR <br> $(\mathbf{V})$ | Benefits |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- |
| 521 | 12 | 7.5 | 5 | 20 | 5000 | $\pm 3$ | Dual, very fast, standard sup- <br> plies, TTL compatible, individ- <br> ual \& common strobe. |
| 522 | 15 | 7.5 | 5 | 20 | 5000 | $\pm 3$ | Same as 521 plus open collec- <br> tor outputs for additional de- <br> coding. |
| 526 | 48 | 5 | 5 | 35 | - | +4.2 <br> -3.2 | General purpose, $\pm 5 \mathrm{~V}$ sup- <br> plies, strobe, separate amplifi- <br> er output, large common mode <br> range. |
| 527 | 26 | 6 | 0.75 | 2 | 5000 | $\pm 6$ | Fast, very low input current, <br> differential outputs, flexible <br> surplus wide common mode <br> range. |
| 529 | 22 | 6 | 5 | 20 | 5000 | $\pm 6$ | Same as 527 but with faster <br> response. |

NOTE Parameters are based on $\mathrm{min} /$ max limits at $25^{\circ} \mathrm{C}$ as defined in the individual data sheet.

Table 5-3 COMPARATOR SELECTION GUIDE

## 526 Comparator

The 526 is a medium speed analog comparator intended for applications where rapid recovery from common mode or differential overdrive is necessary. The circuit consists of a medium gain differential amplifier and high speed TTL gate, Compatible with all TTL logic families, the 526 provides independent amplifier and gate outputs and operates from standard $\pm 5$ volt supplies.

If desired more than one gate may be driven from the 526 amplifier output. Should this be necessary, a 5 k ohm pull down resistor from the amplifier output to $V$ - should be added to increase the sink current capability as shown in Figure 5-55. More than one amplifier may also be tied together for system flexibility. This configuration produces the logic NOR of 2 analog signals at the output of the gate.


## 527 Comparator

Featuring darlington inputs for very low bias current, the 527 is generically related to the 529 comparator. Emitter follower inputs to the differential amplifier are used to trade better input parameters for slightly less speed. As Table 5-3 shows, a factor of 10 improvement in $I_{B I A S}$ is gained with an increase of propagation delay of only 4 ns maximum.

## 529 Comparator

Second in speed only to the 521 device, the 529 is also manufactured using Sihottky technology. Although a few nano seconds slower than the 521, the 529 features variable supplies from $\pm 5$ to $\pm 10$ volts with a high common mode range of $\pm 6$ volts. Both the 527 and 529 Schottky comparators boast complimentary logic outputs with output A being in phase with input A. In addition the supplies of both the 527 and 529 may be non-symmetrical to produce a desired shift in the common mode range.

This technique is illustrated by the ECL to TTL and TTL to ECL translators of Figures $5-65$ and 5-66 respectively. The only major requirement of the supplies is that the negative supply be at least 5 volts more negative than the ground terminal of the gate. This is necessary to insure that the internal bias arrangement has sufficient voltage to operate normally.

## APPLICATIONS

Today's state-of-the-art ultra-high speed comparators are capable of making logic decisions in less than 10 nano seconds. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs however, some preliminary steps should be taken in their use.

## General Precautions Layout

The comparator is capable of resolving submillivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies hidden signal paths become dominant. Of a particular nuisance is distributed capacitance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.
Another source of spurious signal is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, or ringing. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

## Power Supplies

Another general precaution that should always be exercised is power supply bypassing. As mentioned the name of the game is speed. Very high speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason good power supply by-passing is always mandatory very close to the device itself. A tantalum capacitor of 1 to $10 \mu \mathrm{~F}$ in parallel with 500 to 1000 pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

## Unused Inputs

Some currently available comparators such as the 521 and 522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain-bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100 mV to insure the comparator assumes a known state.
If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

## Common Mode Signals

As defined previously manufacturers specify the maximum voltage range over which the inputs may be taken. In addition the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the 529 comparator the differential voltage is restricted to less than $\pm 5$ volts, with a common mode of $\pm 6$ volts. That these two quantities interact cannot be overlooked during application. For instance with both inputs at $\pm 4$ volts the common mode restriction is satisfied. If $V$ ref is now left at +4 volts the signal input may not be taken below ground more than 1 volt because the differential signal becomes 5 volts.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

## Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

## BASIC APPLICATIONS

The basic comparator circuit and its transfer function were presented by Figures 5-49 and 5-50.

When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A to $D$ converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic circuit. Both are only a small deviation from the basic level detector.

## Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.
They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore if the compared voltages remain at or near the threshold for long periods of time, the comparator may oscillate or respond to noise pulses. For instance this is a common problem with successive approximation D/A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 5-56 defines the arrangement. Both positive and negative feedback is provided by RIN and $\mathrm{R}_{\mathrm{f}}$.
Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This

## LEVEL DETECTOR WITH HYSTERESIS



Figure 5-56

## 0 VOLT LEVEL DETECTOR

 WITH $\pm 10 \mathrm{mV}$ HYSTERESIS

Figure 5-57
feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 5-57, prevents output chatter with signals having slow and erratic zero crossings.
As shown in Figure 5-56 the voltage feedback is calculated from the expression:
$V_{H Y S T}=\frac{E_{\text {OUT }} \cdot R_{I N}}{R_{I N}+R_{f}}$
where EOUT is the gate output voltage. The hysteresis voltage is bounded by the common mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired an additional inverting gate is required if the comparator does not have differential outputs. The 527 and 529 devices provide inverted signals from differential outputs while the 521, 522 and 526 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum especially for very high speed comparators such as the 521.

## Line Receiver

Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common mode signal, the very high common mode rejection of the 521/522 makes the unit ideal for differential line receivers. Figure 5-58 depicts the simple schematic arrangement. The 521 is used as a differential amplifier having a logic level output. Because common mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 5-59 illustrates the 521 response to the 200 mV peak to peak 10 MHz differential signal. In Figure 5-60 the same signal has been buried in 5 volts peak to peak of 1 MHz common mode "noise."

As shown the circuit suffers no degradation of signal. If desired several 522 comparators may be "wire OR'd," or a latch output can be accomplished as shown.
The 521 and 529 comparators have the advantage of wider bandwidth to permit higher data rates. Where speed is slower the 526 comparator will also provide the excellent common mode rejection needed for line receiving.

## Double Ended Limit Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single 522 package. The schematic and transfer curve of the circuit is shown in Figure 5-61.

Each half of the 522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open collectors of the 522 minimize external components and connections.

## Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The 521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 5-62 shows a typical oscillator circuit.
The crystal is operated in its series resonant mode, providing the necessary feedback through the capacitor to the input of the 521. The resistor $R_{\text {adj }}$ is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The 521 will oscillate up to 70 MHz . However, crystals with frequencies


## DOUBLE ENDED LIMIT DETECTOR



Figure 5-61a


Figure 5-61b

higher than about 20 MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using input and output mode suppression or tuning. The 522 is especially desirable since the bare collector topology allows the output to be collector tuned readily.

## Analog to Digital Converter

There are many types of $A$ to $D$ converter designs, each having its own merits. However, where speed of conversion is of prime interest the multi-threshold conversion type is used exclusively. It is apparent from Figure 5-63 that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.
The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N -bit converter is $2^{n-1}$. Although the 521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3-bit parallel A-D converter is shown in Figure 5-64 with a 3bit digital equivalent of an analog input shown in Figure 5-63.

Reference voltages for each bit are developed from a precision resistor ladder network. Values of $R$ and $2 R$ are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of $\pm 1 / 2$ bit.

It is apparent from the schematic that the individual strobe line and duality features of the 521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 5-63. All 3-bit outputs have settled and are true a mere 15 ns after the input step of 3 volts has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

## Logic Interface

During the design of the 527 and 529 devices, particular attention was paid to the biasing network so that balanced supplies need not be provided. For example, if the "ground" terminal is set at -5.2 volts and the
other supplies are adjusted accordingly, the output logic 1 state will be at -1.5 volts and logic 0 will be at -5.0 volts. With this freedom of power supply voltage, the user may adjust the output swings to match the desired logic levels even if that logic is other than TTL levels.

## ECL to TTL Interface

Emitter coupled logic is becoming very popular due to its speed. Systems are often built around standard TTL logic with those portions requiring higher speed being implemented with emitter coupled logic. As


3-BIT PARALLEL A-D CONVERTER


Figure 5-64
soon as such a decision is made the problem of interfacing TTL to ECL logic levels is encountered. The standard logic output swings of ECL are -0.8 V to -1.8 V at room temperatures. Converting these signals to TTL levels is accomplished simply by using the basic voltage comparator circuit with slight modifications. Figure 5-65 reveals that the power supplies have been shifted in order to shift the common mode range more negative. This insures that the common mode range is not exceeded by the logic inputs. Since ECL is extremely fast the 529 is usually selected because of its superior speed so that a minimum of time is lost in translation.

## TTL to ECL

Operating in the reverse, TTL levels can also be converted to ECL levels by the 529. Again the 529 is selected as the fastest converter with the necessary power supply flexibility to accomplish the level shifting with a minimum of effort and cost.

A check of output voltage for the 529 reveals that the voltage is slightly less than required by the ECL logic for fast switching. R2 and the diode of Figure 5-66 raises the gate supply voltage and therefore the 529 output voltage by 0.7 V sufficient to guarantee fast switching of the translator. Resistive pull up from the 529 output to $V_{c c}$ can also be used with the gate supply grounded. This method is dependent upon RC time constants of distributed capacitance and is therefore much slower.

## Photo Diode Detector

Responding to the presence or absence of light, the photo diode increases or decreases the current through it. Detecting the changes becomes a matter of converting light and dark currents to voltage across a resistor as shown in Figure 5-67. R1 is selected to be large enough to generate detectable differences between light and dark conditions. Once the signal levels are defined by R1 and the diode characteristics, the average between light and dark signals is used for $V$ reference and is produced by the resistive divider consisting of R1 and R2. The comparator then produces an output dependent upon the presence or absence of light upon the diode.

## SENSE AMPLIFIERS

Closely related to the comparator is the sense amplifier. Signals derived from the many sources such as transducers and core memories are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

As an example, the 1103 MOS RAM output is of the bare drain variety. Hence the output of the memory takes the form of a current for a one level with zero current for a zero level.

It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice resistors larger than 1 k ohm are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. Signetics comparators 521 and 522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.
Design of the sense amplifier network depends upon the 1103 used (1103 or 1103-1) and the input characteristics. Two sense amplifiers will be discussed in this application, the 521/522 and the 75107/75108. Both sets of devices are very similar in operation with basic differences in input parameters

and speed. The significiant specifications are given in Table 5-4.

| DEVICE | $\mathrm{VOS}^{\text {(mV) }}$ | ${ }^{1} \mathrm{~B}(\mu \mathrm{~A})$ | $\mathrm{V}_{\text {IN }}(\mathrm{MIN})(\mathrm{mV})$ | $\begin{array}{\|c\|} \hline \text { SPEED (NS) } \\ \left(\mathrm{V}_{\text {IN }}=100 \mathrm{mV}\right) \end{array}$ | GAIN |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 521 | 10 | 40 | 15 | 12 | 5000 |
| 522 | 10 | 40 | 15 | 15 | 5000 |
| 75107 | - | 75 | 25 | 25 | - |
| 75108 | - | 75 | 25 | 25 | - |

Table 5-4 IMPORTANT SENSE AMPLIFIER PARAMETERS

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

$$
V_{\text {ref }} \leq\left(I_{1}-I_{B}\right) R 1-V_{\text {diff }}
$$

Where $I_{1}$ is the 1103 output current, $I_{B}$ is sense amplifier bias current and $V_{\text {diff }}$ is minimum differential voltage to switch the sense amplifier.
Thus, referring to Figure 5-68, the calculation for the 522 and the 1103-1 becomes:

$$
V_{\text {ref }} \leq(900 \mu \mathrm{~A}-40 \mu \mathrm{~A}) \mathrm{R}-15 \mathrm{mV}
$$

Hence $V_{\text {ref }}$ must be less than 71 mV for a 100 ohm resistor. Values of R1 can be selected from 100 to 1000 ohms. Resistor values less than 100 ohms do not produce sufficient voltage swings while values over 1 k ohm tend to generate excessive noise from capacitively coupled signals.

In large systems noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines being as short as possible will help, but large memories can still be difficult


Figure 5-67

to control. One method of eliminating noise is to use a balanced sense line as shown in Figure 5-69.

During layout a dummy line is run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the $\mathrm{V}_{\text {ref }}$ point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp causing the output to switch.

## Core Memory Sense Amps

The core memory is another device requiring a sense amplifier.

Figure 5-70 shows a simplified block diagram of memory organization in a computer. The appropriate command to the address register selects the appropriate x and $y$ address lines. Two wires are threaded through each core. One is common to all cores in that column arranging a matrix in which any $x$-address line and any $y$-address line has only one core in common.

Both reading and writing are accomplished by driving current through the wires linking the cores. If this current exceeds a minimum value $I_{m}$, the core is reset to zero. Therefore, by driving $\mathrm{Im}_{\mathrm{m}} / 2$ through one of the x -address lines and through one of the $y$-address lines, any one core may be reset. Only the core common to both lines will receive the sum of the currents and will be reset. The rest of the cores receive $I_{\mathrm{m}} / 2$ and will be only halfselected. For a core to be set to the "1" state, the current is reversed in the two selecting wires.

A sense line linking all the cores in the plane together couples the read data out of the array. In order to read a specific core, a " 0 " is first written into that core. If its initial state was at " 1 ", it is reset, generating a pulse on the sense line. If the core is in "0" state, no signal results.

The high currents used in core memory generate a good deal of noise. The sense amplifier used must be able to detect the difference between the disturbed one voltage, without responding to undesired signals. The threshold voltages of the sense amplifier should be adjusted to approximately the mid-point between the sum of the disturbed zero voltages and the minimum disturbed one voltage as defined in Figure 5-71.

The region on either side of the threshold voltage in which the sense amplifier cannot detect the difference between a 0 and a 1 is called the uncertainty region. This region is the sum of the varition of the input threshold voltage and the differential offset voltage and must be less than the voltage difference between ones and zeros generated by the memory core.

Signetics series N7520 Dual Core Memory Sense Amplifiers, successfully solve the basic sense amplifier problems: It provides a stable narrow input threshold, an adjustable reference and output logic functions to fulfill the several variations required in different core memory systems.

The N7520 series uses the "true comparator" technique to achieve superior amplifier threshold performance. A unique circuit design of the internal logic guarantees the fastest possible propagation. Series N7520 is pin compatible with other 7520 series and offers the user these advantages:


Figure 5-69

a. True Comparator technique guarantees that narrow input threshold devices can be built in volume production.
b. An external capacitor is not required for stability. True Comparator technique allows use of simple single stage preamp.
c. Clamp diodes are provided at all gate and strobe inputs.

Figure 5-72 illustrates the necessary connections to utilize the 7524 sense amplifier. The reference voltage against which the sense voltage is compared is derived via the resistor divider network from the 5 volt supply. Other connections are straight forward and for the most part self explanatory.

Care should be exercised in the board layout to minimize stray coupling of signals. Of
extreme importance to the device, the reference voltage must be kept as clean as possible. For instance, ground currents from the gate structure should not be allowed to pass near the reference terminals before finding system ground. Small voltages generated by this current can cause reference instability. Oscillations and general poor performance can also occur if proper techniques are not used in layout.

## 55/75325 MEMORY DRIVERS TYPICAL APPLICATIONS

## Balanced Bipolar Logic Line Driver

The circuit shown in Figure 5-73 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data
or clock pulses over long lines. This linedriver may be operated from a single 5 volt supply; however; the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a tri-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several miles in length or low-impedance coaxial lines.
In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drivelines branch off as shown in Figure 5-74. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13,75154 No. 1 must be set to 3 (with mode select high), enabling source $X$ of 75325 No. 2 to drive lines 12 through 15, and 74154 No. 2 must be set to 2 , providing a sink at $Y$ of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the modeselect voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 5-75. These 256 drive-lines are sufficient to serve $(256 / 2) 2=16,384$ individual cores.

## External Resistor Calculation

A typical magnetic-memory word-drive requirement is shown in Figure 5-76. A source-output transistor of one 75325 delivers load current ( $I_{L}$ ). The sink-output transistor of another 75325 sinks this current.

The value of the external pull-up resistor ( Rext ) for a particular memory application may be determined using the following equation:
$\left.R_{\text {ext }}=\frac{16\left(V_{C C 2}(\min )-V_{S}-2.2\right)}{I_{L}-1.6\left(V_{C C 2}(\text { min })\right.}-V_{S}-2.9\right) \quad$
(Equation 1)
where: $\quad R_{\text {ext }}$ is in $k \Omega$,
$V_{c c 2}(\mathrm{~min})$ is the lowest expected value of $V_{C C 2}$ in volts, $V_{S}$ is the source output voltage in volts with respect to ground, $I_{L}$ is in mA.

TYPICAL SENSE AMPLIFIER HOOK UP USING 7524


Figure 5-72

The power dissipated in resistor Rext during the load current pulse duration is calculated using Equation 2,
$P_{\text {Rext }} \approx \frac{L_{L}}{16}\left[\mathrm{~V}_{\operatorname{CC} 2(\text { min })}-\mathrm{V}_{\mathrm{S}}-2\right]$
(Equation 2)
where: PRext is in mW .
After solving for Rext, the magnitude of the source collector current (Ics) is determined from Equation 3,

$$
\mathrm{Ics} \approx 0.94 \mathrm{IL}
$$

(Equation 3)
where: Ics is in mA.
As an example, let $\mathrm{V}_{\mathrm{CC} 2(\mathrm{~min})}=20 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{L}}=$ 3 V while I of 500 mA flows.

Using Equation 1,
$R_{\text {ext }}=\frac{16(20-3-2.2)}{500-1.6(20-3-2.9)}=0.5 \mathrm{k} \Omega$

BALANCED BIPOLAR LOGIC LINE DRIVER

a. Test Circuit

b. Voltage Waveforms

75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES


NOTE A This optional mode select and timing strobe technique can be used in place of the 7440 mode select and 74154 timing strobe when minimum time skew is desired.

Figure 5-74


and from Equation 2,
$P_{\text {Rext }} \approx \frac{500}{16}(20-3-2) \approx 470 \mathrm{~mW}$
The amount of the memory system current source (Ics) from Equation 3 is:

$$
\mathrm{ICS} \approx 0.94(500) \approx 470 \mathrm{~mA}
$$

In this example the regulated source-output transistor base current through the external pull-up resistor ( Rext ) and the source gate is approximately 30 mA . This current and Ics comprise IL.

## VIDEO AMPLIFIER PRODUCTS

## 592 Video Amplifier

The 592 is a two stage differential output, wideband video amplifier with voltage gains as high as 400 and bandwidths up to 120 MHz .

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins $G_{1 A}$ $\mathrm{G}_{1 B}$ and $\mathrm{G}_{2 A}-\mathrm{G}_{2 B}$ respectively. As shown
by Figure 5-78 the emitter circuits of the differential pair return thru independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400 volts per volt. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single ended gains are one half the stated value.
2. The circuit 3 dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer the input bias current required by the 592 may be passed directly thru the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a dc path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output dc offset, they should be small ideally 0 ohms. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5 V ).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents ( $1.5 \mathrm{~V}-1.0 \mathrm{~V}=0.5 \mathrm{~V}$ ).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.

## THERMAL INFORMATION



FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE


NOTE A rated operating free add temperature ranges must be observed regardless of heat sinking.

Figure 5-77

| PARAMETER | $\mathbf{5 0 1}$ | $\mathbf{5 9 2}$ | $\mathbf{7 3 3}$ |
| :---: | :---: | :---: | :---: |
| BANDWIDTH <br> (MH $\mathbf{Z}$ ) | 150 | 120 | 120 |
| GAIN | $6,10,20,50$ | $0,100,400$ | $10,100,400$ |
| $\mathbf{R}_{\text {IN }}$ <br> (K) | 1 | $4-30$ | $4-250$ |
| VPP <br> (VOLTS) | 3.5 | 4.0 | 4.0 |

Table 5-5 VIDEO AMPLIFIER COMPARISON FILE
4. The maximum input resistor size is:
$R_{\text {MAX }}=\frac{\text { Input Offset Voltage }}{\text { Max Input Offset Current }}$

$$
\begin{aligned}
& \frac{.005 \mathrm{~V}}{3 \mu \mathrm{~A}} \\
& =1.67 \mathrm{k} \Omega
\end{aligned}
$$

Of paramount importance during the design of the 592 device was bandwidth. In a monolithic device, this precludes the use of pnp transistors and standard level shifting techniques used in lower frequency devices. Thus without the aid of level shifting the output common mode voltage present on the 592 is typically 2.9 volts. Most applications, therefore, require capacitive coupling to the load. An exception to the rule is a differential amplifier with an input common mode range greater than +2.9 V as shown in Figure 5-79. In this circuit, the 592 drives a 511B transistor array connected as a differential cascode amplifier. This amplifier is capable of differential output voltages of 48 V peak-to-peak with a 3 dB bandwidth of approximately 10 MHz (depending on the capacitive load). For optimum operation, R1 is set for a no signal level of +18 V . The emitter resistors, $R_{E}$, were selected to give the cascode amplifier a differential gain of 10. The gain of the composite amplifier is adjusted at the gain selected point of the 592.

## 592 INPUT STRUCTURE



All resistor values are in ohms.

Figure 5-78


## Filters

As mentioned earlier, the emitter circuit of the 592 includes two current sources. Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 5-80 the overall gain at low frequencies is a negative 48 dB .
Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10 MHz the gain is 0 dB or unity.
Referring to Figure 5-81, the impedance seen looking across the emitter structure includes small $r_{e}$ of each transistor.
Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2 mA causing the quantity of 2 $r_{e}$ to be approximately 32 ohms. Overall device gain is thus given by

$$
\frac{V_{0}(S)}{V_{I N}(S)}=\frac{1.4 \times 104}{Z_{(S)}+32}
$$

where $Z_{(S)}$ can be a resistance or a reactive impedance. Table 5-6 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 5-6 is the gain calculation to determine the voltage gain as a function of frequency.

## Differentiation

With the addition of a capacitor across the gain select terminals the 592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common mode rejection for proper operation.

## Disc file Decoding

In recovering data from disc or drum files, several steps must be taken to pre-condition the linear data. The NE592 video amplifier, coupled with the 8T20 bi-directional oneshot, provides all the signal conditioning necessary for phase encoded data.
When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually $500 \mu \mathrm{~V}$ p-p to 3 mV p-p for oxide coated disc files and 1 to 20 mV p-p for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

The classical approach to peak-time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.


Figure 5-80

A circuit which provides the preconditioning described above is shown in Figure 5-83. Readback data is applied directly to the input of the first 592. This amplifier functions as a wideband ac coupled amplifier with a gain of 100 . The NE592 is excellent for this use because of its high phase linearity, high grain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common mode rejection ratio of the amplifier is preserved. DC components are also rejected because the 592 has no gain at dc due to the capacitance across the gain select terminals.

## BASIC GAIN CONFIGURATION


$\begin{aligned} \frac{V_{0}(s)}{V_{1}(s)} & =\frac{1.4 \times 10^{4}}{Z(s)+2 r e} \\ & =\frac{1.4 \times 10^{4}}{z(s)}\end{aligned}$
$=\frac{1.4 \times 10^{4}}{Z(s)+32}$

Figure 5-81

| Z NETWORK | FILTER TYPE | $V_{0}$ (s) TRANSFER <br> $V_{1}$ (s) FUNCTION |
| :---: | :---: | :---: |
| $0 ـ \overbrace{\text { R }}^{\text {R }}$ | LOW PASS | $\frac{1.4 \times 10^{4}}{L}\left[\frac{1}{s+R / L}\right]$ |
|  | HIGH PASS | $\frac{1.4 \times 10^{4}}{R}\left[\frac{s}{s+1 / R C}\right]$ |
|  | BAND PASS | $\frac{1.4 \times 10^{4}}{L}\left[\frac{s}{s^{2}+R / L s+1 / L C}\right]$ |
|  | BAND REJECT | $\frac{1.4 \times 10^{4}}{R}\left[\frac{s^{2}+1 / L C}{s^{2}+1 / L C+s / R C}\right]$ |

NOTE: in the networks above, the $R$ value used is assumed to include $2 \mathrm{r}_{\mathrm{e}}$, or approximately, 32 ohms.

Table 5-6 FILTER NETWORKS

The output of the first stage amplifier is routed to a linear phase shift low pass filter. The filter is a single stage constant K filter, with a characteristic impedance of $200 \Omega$ Calculations for the filter are as follows:
$\mathrm{L}=2 \mathrm{R} / \omega \mathrm{c}$ Where $\mathrm{R}=$ characteristic impedance (ohms)
$C=1 / \omega C \omega C=$ cutoff frequency (radians $/ \mathrm{sec}$ )

The second 592 is utilized as a low noise differentiator/amplifier stage. The 592 is excellent in this application because it allows differentiation with excellent common mode noise rejection.

The output of the differentiator/amplifier is connected to the 8T20 bi-directional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 5-83 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 5-85.

## Automatic Gain Control

The 592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system. With the circuit of Figure 5-84, the signal is fed to the signal input of the MC1496 and RC coupled to the 592. Unbalancing the carrier input of the MC1496 causes the signal to pass thru unattenuated. Rectifying and filtering one of the 592 outputs produces a dc signal which is proportional to the ac signal ampli-
tude. After filtering this control signal is applied to the MC1496 causing its gain to change.

## LINE DRIVERS AND RECEIVERS

Many types of line drivers and receivers are available today. Each device has been designed to meet specific criteria. For instance, the device may be extremely wide band or be intended for use in party line systems. Some include built in hysteresis in the receiver while others do not.

DIFFERENTIAL WITH HIGH COMMON MODE NOISE REJECTION


For frequency $\mathrm{F}_{1} \ll 1 / 2 \pi(32) \mathrm{C}$
$\mathrm{V}_{0} \cong 1.4 \times 10^{4} \mathrm{C} \frac{\mathrm{dvi}}{d T}$
All resistor values are in ohms.

Figure 5-82

5MHz PHASE-ENCODED DATA
READ CIRCUITRY


All resistor values are in ohms.

Figure 5-83

WIDE BAND AGC AMPLIFIER


All resistor values are in ohms

Figure 5-84

## The EIA Standard

The Electronic Industries Association has produced a set of specifications dealing with the transmission of data between data terminal and communications equipment. This is EIA Standard RS-232-C and delineates much information about signal levels and hardware configurations in data systems.

## MC1488/1489

As line driver and receiver the MC1488 and MC1489 meet or exceed the RS-232 specification.
Standard RS-232 defines the voltage level as being from 5 to 15 volts with positive voltage representing a logic 0 . The MC1488 meets these requirements when loaded with resistors from $3 k$ to 7 k ohms.

## TEST RESULTS



Figure 5-85

Output slew rates are limited by RS-232 to 30 volts per microsecond. To accomplish this specification the MC1488 is loaded at its output by capacitance as shown by the typical hookup diagram of Figure 5-86. A graph of slew rate vs output capacitance is given in Figure 5-87. For the standard $30 \mathrm{~V} / \mu \mathrm{s}$ a capacitance of 300 pF is selected.

The short circuit current charges the capacitance with the relationship.

$$
C=\frac{\operatorname{Isc} \Delta T}{\Delta V}
$$

The EIA standard also states that output shorts to any other conductor of the cable must not damage the driver. Thus the MC1488 is designed such that the output will withstand shorts to other conductors indefinitely even if these conductors are at worst case voltage levels. In addition to output protection the MC1488 includes a 300 ohm resistor to ensure that the output impedance of the driver will be at least 300 ohms even if the power supply is turned off. In cases where power supply malfunction produces a low impedance to ground, the 300 ohm resistors are shorted to ground also. Output shorts then can cause excessive power dissipation. Preventing such a case from happening, series diodes should be included in both supply lines as pictured in Figure 5-88.
The companion receiver MC1489 is also designed to meet RS-232 specifications for receivers. It must detect a voltage from $\pm 3$ to $\pm 25$ volts as logic signals but cannot generate a differential voltage of greater than 2 volts should its inputs become open circuited. Noise and spurious signals are rejected by incorporating positive feedback internally to produce hysteresis. Featured also in the receiver is an external response node so that the threshold may be externally varied to fit the application. Figure 5-89 shows the shift in high and low trip points as a function of the programming resistance.

## PERIPHERAL DRIVERS

Peripheral drivers are general purpose interface devices which interface between logic and devices requiring high current.

## Application Areas

## POWER SWITCHING

- Relay Drivers
- Electromechanical Controls
- SCR or TRIAC Gates


## LAMP DRIVERS

- Pilot Lamps
- Intensity Control

TYPICAL LINE DRIVER-RECEIVER APPLICATION


Figure 5-86

## OUTPUT SLEW RATE vs. LOAD CAPACITANCE



Figure 5-87


Figure 5-88

## LEVEL SHIFTERS

- TTL-to-MOS
- MOS-to-TTL

SIGNAL COMPARISON

- In-Phase Logic Detector

SIGNAL GENERATION

- Square Wave Generator


## TIMING

- Dual Channel One Shot
- Two Phase MOS Clock Driver

Basic Requirements for a Peripheral Driver

- Input Logic Compatibility
- High Output Current/High Voltage Compliance


Figure 5-89


## DARLINGTON TRANSISTOR

 ARRAYSDarlington Transistor Arrays are high voltage, high current arrays comprised of seven silicon npn Darlington pairs on a common monolithic substrate.

## ULN 2001 Series

The ULN 2001 Series features

- General purpose (DTL, TTL, PMOS, CMOS)
- High current: 500 mA continuous
- High voltage: VCE $=50 \mathrm{~V}$
- Output suppression diodes
- Fast switching: $1 \mu \mathrm{~s}$ typ. $5 \mu \mathrm{~s}$ max.
- Open collector outputs


## NE 5501 Series

The NE 5501 Series features are the same as the ULN 2001 Series with the following exceptions:

- High voltage: VCE $=90 \mathrm{~V}$
- High current: 350mA continuous
- High Speed
- Application Versatility


## Other Requirements Include:

- Compatability with popular supply voltages
- Medium to high power capability
- Economical packaging
- Good pin arrangement

A peripheral driver has two basic building blocks:
(See Figure 5-90)

1. TTL gate
2. Discrete transistor with good output drive capabilities

| DEVICE | FEATURES |
| :--- | :--- |
| $75450 B$ | 30 volt breakdown, 24-35ns |
| $75451 B$ | switching, choise of logic |
| $75452 B$ | function, 300mA output |
| DS3611 | 80 volt breakdown |
| DS3612 | 100-300ns switching |
| DS3613 | speed, 300mA |
| DS3614 | output |
| UDN5711 | Same as DS3611 series with |
| UDN5712 | the addition of output |
| UDN5713 | suppression diodes |
| UDN5714 |  |
| ULN2001 | General purpose |
| ULN2002 | Darlington NPN |
| ULN2003 | Transistor arrays |
| ULN2004 | 50 volt breakdown |
|  | 500mA output |
| NE5501 | Output suppression diodes |
| NE5502 | Same as ULN 2001 series except |
| NE5503 | for 90 volt breakdown, and 350mA |
| NE5504 | output |

TABLE 5-7 PERIPHERAL DRIVER PRODUCTS

## Typical Applications




## sECTION 23 TImers

## INTRODUCTION

In mid 1972, Signetics introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the I.C. operational amplifier.
The simplicity of the timer in conjunction with its ability to produce long time delays in a variety of applications has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

## DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 6-1.
changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network When the capacitor voltage exceeds $2 / 3$ of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", hereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.
The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of $1 \%$ with a $50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ timing drift with temperature. To operate the timer as a one shot, only two external components are necessary; resistance \& capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to $500 \mathrm{KHz}_{z}$ can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage


The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at $2 / 3$ of supply voltage level and the trigger comparator is referenced at $1 / 3$ of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below $1 / 3$ of the supply, the comparator
control of timing and oscillation functions is also available,

## Timer Circuitry

The timer is comprised of five distinct circuits; two voltage comparators, a resistive voltage divider reference, a bistable flip-flop, a discharge transistor, and an output stage that is the "totem pole" design for sink or source capability.
$\mathrm{Q}_{10}-\mathrm{Q}_{13}$ comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger; $\mathrm{Q}_{10}$ and $\mathrm{Q}_{11}$ turn on when the voltage at pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R7, R8 and R9. All three resistors are of equal value ( 5 K ohms). At fifteen volts supply, the triggering level would be five volts. When $\mathrm{Q}_{10}$ and $\mathrm{Q}_{11}$ turn on, they provide a base drive for $\mathrm{Q}_{15}$, turning it on. $\mathrm{Q}_{16}$ and $\mathrm{Q}_{17}$ form a bistable flip-flop. When $\mathrm{Q}_{15}$ is saturated, $\mathrm{Q}_{16}$ is 'off' and $\mathrm{Q}_{17}$ is saturated. $\mathrm{Q}_{16}$ and $\mathrm{Q}_{17}$ will remain in these states even if the trigger is removed and $\mathrm{Q}_{15}$ is turned 'off'. While $\mathrm{Q}_{17}$ is saturated, $\mathrm{Q}_{20}$ and $\mathrm{Q}_{14}$ are turned off.

The output structure of the timer is a "totem pole"design, with $\mathrm{Q}_{22}$ and $\mathrm{Q}_{24}$ being large geometry transistors capable of providing 200 mA with a fifteen volt supply. While $\mathrm{Q}_{20}$ is 'off', base drive is provided for $\mathrm{Q}_{22}$ by $\mathrm{O}_{21}$, thus providing a high output.

For the duration that the output is in a high state, the discharge transistor is 'off'. Since the collector of $\mathrm{Q}_{14}$ is typically connected to the external timing capacitor, C, while $\mathrm{Q}_{14}$ is off the timing capacitor now can charge thru the timing resistor, $\mathrm{R}_{\mathrm{A}}$.

The capacitor voltage is monitored by the threshold comparator ( $\mathrm{O}_{1}-\mathrm{Q}_{4}$ ) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$ thru $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$. Amplification of the current change is provided by $\mathrm{Q}_{5}$ and Q6. Q5- Q6 and $\mathrm{Q}_{7}-\mathrm{Q}_{8}$ comprise a diode-biased amplifier. The amplified current change from Q6 now provides a base drive for $\mathrm{Q}_{16}$ which is part of the bistable flip-flop to change states. In doing so, the output is driven "low", and $\mathrm{O}_{14}$ the discharge transistor is turned "on" shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is important; more than that, it is essential that one understands all the variations possible in order to utilize this device to its fullest extent.

## SCHEMATIC 555 OR $1 / 2556$ DUAL TIMER


all resistor values are in ohms

Figure 6-2

## Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, $\mathrm{Q}_{25}$, is off with its base held high. When the base of $\mathrm{O}_{25}$ is grounded, it turns on, providing base drive to $Q_{14}$, turning it on. This discharges the timing capacitor, resets the flip-flop at Q17, and drives the output low. The reset overrides all other functions within the timer.

## Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into
the trigger. By $A C$ coupling the trigger, see Figure 3, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of $\mathrm{Q}_{15}$ on the base of $Q_{16}$, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

## Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, $\mathrm{Q}_{10}-\mathrm{Q}_{13}$, and the threshold comparator, $\mathrm{Q}_{1}-\mathrm{Q}_{4}$, are referenced to an internal resistor divider network, $\mathrm{R}_{7}$, R8, R9. This network establishes the nominal two thirds of supply voltage ( Vcc ) trip point for the threshold comparator and one third of

## AC COUPLING OF THE TRIGGER PULSE



ALL RESISTOR VALUES ARE IN OHMS


SWITCH GROUNDE:
AT THIS POINT

Figure 6-3

Vcc for the trigger comparator. The two thirds point at the junction of $\mathrm{R}_{7}, \mathrm{R}_{8}$ and the base of $\mathrm{O}_{4}$ is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage controlled oscillator, pulse width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor $(.01 \mu \mathrm{~F})$ be place across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

## Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one shot)
2. Astable (oscillatory)
3. Time delay

By utilizing any one or combination of basic operating modes and suitable variations it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.
One of the simplest and most widely used operating modes of the timer is the monostable (one shot). This configuration requires only two external components for operation (See Figure 6-4). The sequence of events starts when a voltage below one third Vcc is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative going pulse. On the negative going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, $C$, starts charging thru the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant $T=R C$. Ignoring capacitor leakage, the capacitor will reach the two thirds Vcc level in 1.1 time constants or

$$
\mathrm{T}=1.1 \mathrm{RC}
$$

where $T$ is in seconds; $R$ is in ohms and; C is in Farads. This voltage level trips the threshold comparator, which in turn


Figure 6-4


Figure 6-5
drives the output low and turns on the discharge transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

## Astable Operation

In the astable (free run) mode, only one additional component, Rb is necessary.

The trigger is now tied to the threshold pin. At power up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path thru $\mathrm{R}_{\mathrm{A}}$ and $\mathrm{R}_{\mathrm{B}}$. When the capacitor reaches the threshold level of $2 / 3 \mathrm{Vcc}$, the output drops low and the discharge transistor turns on.

The timing capacitor now discharges thru $\mathrm{R}_{\mathrm{B}}$. When the capacitor voltage drops to $1 / 3 \mathrm{Vcc}$, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$
f=\frac{1.49}{\left(R_{A}+2 R_{B}\right) C}
$$

Selecting the ratios or $R_{A}$ and $R_{B}$ varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if $\mathrm{R}_{\mathrm{A}}=0$, the charge time cannot be made smaller than the discharge time because the charge path is $R_{A}+R_{B}$ while the discharge path is $R_{B}$ alone. In this case it becomes necessary to insert a diode in parallel with $\mathrm{R}_{\mathrm{B}}$, cathode toward the timing capacitor. Another diode is desireable, but not mandatory, this one in series with $\mathrm{R}_{\mathrm{B}}$, cathode away from the timing capacitor. Now the charge path becomes $\mathrm{R}_{\mathrm{A}}$, thru the parallel diode into C . Discharge is thru the series diode and $\mathrm{R}_{\mathrm{B}}$ to the discharge transistor. This scheme will afford a duty cycle range from less than $5 \%$ to greater than $95 \%$. It should be noted that for reliable operation a minimum value of $3 \mathrm{~K} \Omega$ for $R_{B}$ is recommended to assure that oscillation begins.


## Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied, the output immediately changed to the high state, timed out, and returned to its pre-trigger low state. in the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.


The threshold and trigger are tied together monitoring the capacitor voltage. The discharge function is not used. The operation sequence begins as transistor ( $\mathrm{T}_{1}$ ) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off the capacitor commences its charge cycle. When the capacitor reaches the threshold level, then and only then does the output change from its normally high state to the low state. The output will remain low until $\mathrm{T}_{1}$ is again turned on.

## GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5 volts to 15 volts DC, with 16 VDC being the absolute max. rating. Most of the devices, however, will operate at voltage levels as low as 3 VDC. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply volatage may be provided by any number of sources: however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the Vcc and ground, ideally, directly across the device is necessary. The size of capacitor will depend on the specific application. Values of capacitance from $.01 \mu \mathrm{~F}$ to $10 \mu \mathrm{~F}$ are not uncommon. Note that the bypass capacitor would be as close to the device as physically possible.

## Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.
Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e. deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by $.01 \%$ to 10 and 20 percent. Capacitors may have a 5 to 10 percent deviation from rated capacity. Therefore, in a
system where timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance will allow for best adjustability and performance.
The timing capacitor should be a high quality, stable component with very low leakage characteristics. Under no circumstances should ceramic disc capacitors be used in the timing network! Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantulum or similar types.

The timer typically exhibits a small negative temperature coefficient ( $50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ ). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is $.25 \mu \mathrm{~A}$. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$
\begin{aligned}
& \text { Vpotential }=\mathrm{V}_{\mathrm{cc}}-\mathrm{V} \text { capacitor } \\
& \text { Vpotential }=\mathrm{V}_{\mathrm{cc}}-2 / 3 \mathrm{~V}_{\mathrm{cc}}= \\
& 1 / 3 \mathrm{~V}_{\mathrm{cc}}
\end{aligned}
$$

Maximum resistance is then defined as

$$
\begin{aligned}
& R_{\max }=\frac{V_{c c}-V_{\text {cap }}}{l_{\text {thresh }}} \\
& \text { Example: } V_{c c}=15 \mathrm{~V} \\
& R_{\max }=\frac{15-10}{.25\left(10^{-6)}\right.}=20 \mathrm{M} \Omega \\
& V_{c c}=5 \mathrm{~V} \\
& R_{\max }=\frac{5-3.33}{.25\left(10^{-6)}\right.}
\end{aligned}
$$

NOTE: If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, $\mathrm{Q}_{14}$, is current limited at 35 mA to 55 mA internally. Thus, at the current limiting values, $\mathrm{Q}_{14}$, establishes high saturation voltages. When examining the currents at $\mathrm{Q}_{14}$, remember that the transistor, when turned on will be carrying two current loads. The first being the constant current thru timing resistor, $R_{A}$. The second will be the varying discharge current from the timing capacitor. To provide best operation the current contributed by the $R_{A}$ path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5 K ohm value be the minimum feasible value for $R_{A}$. This does not mean lower values cannot be used successfully in certain applications. Yet there are extreme cases that should be avoided if at all possible.
Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized though. (It should be a cardinal rule that applies to the usage of all I C's.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor, may be necessary.
The most important characteristic of the capacitor should be as low a leakage as possible. Obviously any leakage will subtract from the charge count causing the calculated time to be longer than anticipated.

## Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R7, or R8. The combination of $R_{7}, R_{8}$ and $R_{9}$ comprise the resistive voltage divider network that establishes the nominal $1 / 3$ Vcc trigger comparator level (junction R8, R9) and the $2 / 3$ Vcc level for the threshold comparator (junction R7, R8).
For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold compara-
tor "set" level above or below the $2 / 3$ Vcc nominal, hereby varying the timing. In the monostable mode, the control voltage may be varied from 45 percent to 90 percent of Vcc. The 45 to 90 percent figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free run) mode, the control voltage limitations are from 1.7 volts to Vcc. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level it also raise the trigger comparator level by one half that amount due to Rs and R9 of Figure 2. As a voltage controlled oscillator, one can expect $\pm 25 \%$ around center frequency (fo) to be virtually linear with a normal RC timing circuit. For wider linear variations around $F_{\circ}$ it may be desireable to replace the charging resistor with a constant current source. In this manner the exponential charging characteristics of the classical configura: tion will be altered to linear charge time.

## Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e. - device off during power up). It can also be used in conjunction with the trigger pin to establish a positive edge triggered circuit as opposed to the normal negative edge trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4 V and 1.0 V ( $\min / \max$ ). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1 volt. At that point the trigger is in the "turn on" region, below $1 / 3$ Vcc. This will cause the device to trigger immediately, effectively triggering on the positive going edge if a pulse is applied to pins 4 and 2 simultaneously.

## FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncracies that may exhibit themselves from time
to time in various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the first time constant is approximately twice as long as the rest. Why?

Answer: In the oscillator mode the capacitor voltage fluctuates between $1 / 3$ and $2 / 3$ of the supply voltage. When reset is pulled down the capacitor discharges completely. Thus for the first cycle it must charge from ground to $2 / 3 \mathrm{Vcc}$ which takes twice as long.
2. What is maximum frequency of oscillations?
Answer: Most devices will oscillate about 1 M Hz . However, in the interest of temperature stability one should operate only up to about 500 kHz .
3. What is temperature drift for oscillator mode?
Answer: Temperature drift of oscillator mode is 3 times that of one shot mode due to addition of second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.
4. Oscillator exhibits spurious oscillations on cross over points. Why?
Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.
5. Trying to drive a relay but 555 hangs up. How come?

Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving pin 3 below a negative .6 volts. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode thus preventing pin 3 from ever seeing a negative voltage.
6. Double triggering of the TTL loads sometimes occurs. Why?
Answer: Due to the high current capability and fast rise and fall times of the output a totem pole structure different from the TTL classical structure was used. Near TTL threshold
this output exhibits a cross over distortion which may double trigger logic. A 1000 pF capacitor from the output to ground will eliminate any false triggering.
7. What is the longest time I can get out of the timer?
Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point dependent on required accuracy. Normally 20 to 30 min . is the longest feasible time.

## DRIVING HIGH Q INDUCTIVE LOADS



Figure 6-8

## DESIGN FORMULAS

Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.



MODIFIED DUTY CYCLE (ASTABLE)


ASTABLE TIMING


## APPLICATIONS

The timer since introduction has spurred the imagination of thousands. Thus the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.

## Missing Pulse Detector

Using the circuit of Figure 6-9a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure $6-9 \mathrm{~b}$ shows the actual waveforms seen in this mode of operation.


If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle.

## Frequency Divider




Figure 6-10b
Figure 6-10b shows the waveforms of the timer in Figure 6-10a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

## Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 611a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5 ). This has the effect of modulating the pulse width as the control voltage varies. Figure 6-11b shows the actual waveform generated with this circuit.


Figure 6-11a

## EXPECTED WAVE FORMS

$\mathrm{t}=0.5 \mathrm{MS} / \mathrm{CM}$
$\begin{aligned} & \mathbf{t}=0.5 \mathrm{MS} \\ & \text { MODULATION INPUT }-2 \mathrm{~V} / \mathrm{CM}\end{aligned}$


Figure 6-11b

## Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation, Figure $6-12 a$, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure $6-12 b$ shows the waveform generated for triangle wave modulation signal.


Figure 6-12a
EXPECTED WAVE FORMS


Figure 6-12b


## Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one shot and the second half as an oscillator. (Figure 6-13)
The pulse established by the one shot turns on the oscillator allowing a burst to be generated.

## Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a $.001 \mu \mathrm{fd}$ coupling capacitor sequential timing may be obtained. Delay $t_{1}$ is determined by the first half and $t_{2}$ by the second half delay. (Figure 6-14)
The first half of the timer is started by momentarily connecting pin 6 to ground. When it is timed out (determined by $1.1 \mathrm{R}_{1} \mathrm{C}_{1}$ ) the second half begins. Its duration is determined by $1.1 \mathrm{R}_{2} \mathrm{C}_{2}$.

## SEQUENTIAL TIMER


all resistor values are in ohms

Figure 6-14

## METHOD OF ACHIEVING LONG TIME DELAYS



Figure 6-15

## Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays expensive capacitors with extremely low leakage are required. the practicality of the components involved limits the time between pulses to something in the neighborhood of twenty minutes.
To achieve longer time periods both halves may be connected in tandem with a "divide-by" network in between.
The first timer section operates in an oscillatory mode with a period of $1 / \mathrm{f}_{0}$. This signal is then applied to a "Divide-by- $\mathrm{N}^{\prime \prime}$ network to give an output with the period of $\mathrm{N} / \mathrm{fo}$. This can then be
used to trigger the second half of the 556. The total time is now a function of N and $\mathrm{f}_{0}$ (Figure 6-15).

## Auto Burglar Alarm

This circuit utilizes the time delay mode of operation. When the arm/disarm switch is opened (normally closed) the exit timer starts its timing cycle. Pin 5 will go low after the exit time lapse to energize the alarm circuit. Door switches, when closed will keep the PNP transistor of. by keeping pin 9 high. When any door switch is opened, after a delay, the transistor will turn on sounding horn of the arm/disarm switch is not closed within the delay time (Figure 6-16).

## Speed Warning Device (1)

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 6-17a).

## Car Tachometer (1)

The timer receives pulses from the distributor points. Meter $M$ receives a calibrated current thru R6 when the timer output is high. After time out the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 6-18).

## BURGLAR ALARM CIRCUIT



Figure 6-16


## Oscilloscope Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage $(0.33 \mathrm{Vcc})$, the flipflop resets and the transistor conducts, discharging the capacitor (Figure 6-19).

## Square Wave Tone Burst Generator (4)

Depressing the pushbutton provides square-wave tone bursts whose duration depends on the duration for which the voltage at pin 4 exceeds a threshold. Components $\mathrm{R}_{1}, \mathrm{R}_{2}$ and $\mathrm{C}_{1}$ causes the astable action of the timer IC (Figure 6-20).

## Regulated DC-to-DC

## Converter (2)

Regulated DC to DC converter produces 15 V DC outputs from a +5 V DC input. Line and load regulation is $0.1 \%$ (Figure 6-21).

## Voltage to Pulse Duration Converter (1)

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than $1 \%$ can be obtained with this circuit (a) and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 6-22).

## SCHEMATIC OF TRIGGERED SWEEP



Figure 6-19

SQUARE WAVE TONE BURST GENERATOR

all resistor values in ohms

Figure 6-20

## REGULATED DC TO DC CONVERTER



Figure 6-21

VOLTAGE-TO-PULSE-DURATION CONVERTER


Figure 6-22

## Servo System <br> Controller (1)

To remoteley control a servo motor, the 555 needs only six extra components (Figure 6-23).

## Stimulus Isolator (5)

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200 V at $200 \mu \mathrm{~A}$ (Figure 6-24).

## Voltage to Frequency Converter <br> (0.2\% Accuracy) (6)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to -10 V . Its mirror image (b) provides the same linearity over the 0 -to +10 V range but is not DTL/TTL compatible (Figure $6-25 \mathrm{a}$ \& b.)



Figure 6-24


## Positive to Negative Converter (7)

Transformerless dc-dc converter derives a negative supply voltage from a positive. As a bonus the circuit also generates a clock signal.
The negative output voltage tracks the dc input voltage linearity (a), but its magnitude is about 3 V lower, Application of a $500 \Omega$ load, (b), causes $10 \%$ change from the no-load value (Figure $6-26 a, b, \& c)$.

POSITIVE TO NEGATIVE CONVERTER

all resistor values are in ohms
Figure 6-26a

## Auto Burglar Alarm (8)

Timer A produces a safegaurd delay, allowing driver to disarm alarm and eliminating vulnerable outside control switch. The SCR prevents timer A from triggering timer $B$, unless timer $B$ is triggered by strategically located sensor switches (Figure 6-27).


Figure 6-26b


Figure 6-26c

## Cable Tester (9)

Compact tester checks cables for opencicuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse-generated by the timer IC - appears at both ends of the line. A clock pulse just at the clock end of the line lights green light-emitting diode; and a clock pulse only at the other end lights a red LED (Figure 6-28).

Low Cost Line Receiver (10)
The timer makes an excellent line receiver for control applications involving relatively slow electro-mechanical devices. It can work without special drivers over single unshielded lines (Figure 6-29).


CABLE TESTER


Figure 6-28

all resistor values are in ohms

## Temperature Control (11)

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within $\pm 1$ Hertz over a $78^{\circ} \mathrm{F}$ temperature range (Figure 6-30a \& b).

## Automobile Voltage Regulator (12)

Monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (pin 3 ) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4 volts in this case), the timer turns on and the Darlington pair conducts (Figure 6-31).

Figure 6-29


Figure 6-31

## Switching Regulator (13)

The basic regulator of Figure 6-32 is shown here with its associated timing and pulse generating circuitry. The block diagram illustrates how the over-all regulator works. The multivibrator determines switching frequency, and the error amplifier adjusts the pulse width of the modulator to maintain output voltage at the desired level. The output resistor divider provides the sensing voltage. (Figure 6-35)

DC-to-DC Converter (14)


Figure 6-32
Ramp Generator (14)


Audio Oscillator (14)


## SWITCHING REGULATOR



Figure 6-35

## Low Power Monostable Operation

In battery operated equipment where load current is a significant factor figure 36 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series
and 74LOO series. During the monostable time, the current drawn is 4.5 mA for $T=1.1 \mathrm{RC}$. The rest of the time the current drawn is less than $50 \mu \mathrm{~A}$. Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.
In other low power operations of the timer where Vcc is removed until timing
is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

LOW POWER MONOSTABLE


Figure 6-36

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## INTRODUCTION

The 558/559 are monolithic Quad Timers designed to be used in the timing range from a few microseconds to a few hours. Four entirely independent timing functions can be acheived, using a timing resistor and capacitor for each section. Two sections of the quad may be interconnected for astable operation. All four sections may be used together, in tandem, for sequential timing applications up to several hours. No coupling capacitors are required when connecting the output of one timer section to the input of the next.

## FEATURES

- 100 mA OUTPUT CURRENT PER SEC. TION
- EDGE TRIGGERED (NO COUPLING CAPACITOR)
- OUTPUT INDEPENDENT OF TRIGGER CONDITIONS
- WIDE SUPPLY VOLTAGE RANGE 4.5V TO 16V
- TIMER INTERVALS FROM MICROSECONDS TO HOURS
- TIME PERIOD EQUALS RC


## CIRCUIT OPERATIONS

In the one shot mode of operation, it is necessary to supply a minimum of two external components, the resistor and capacitor for timing. The time period is equal to the product of $R$ and $C$. An output load must be present to complete the circuit due to the output structure of the 558/559.
For astable operation, it is desireable to cross couple two devices from the 558/ 559 Quad. The outputs are direct coupled to the opposite trigger input. The duty cycle can be set by ratio of $\mathrm{R}_{1} \mathrm{C}_{1}$ to $\mathrm{R}_{2} \mathrm{C}_{2}$ from close to zero to almost $100 \%$. An astable circuit using one timer is shown on page 13.

## OUTPUT STRUCTURE 558

The 558 structure is open collector which requires a pull-up resistor to Vcc and is capable of sinking 100 mA per unit but not to exceed the power dissipation and junction temperature rating of the die and package. The output is normally low and is switched high when triggered.

## OUTPUT STRUCTURE 559

The 559 output is normally low and off. It sources up to 100 mA from a Darlington emitter follower when switched on. A pull down resistor to ground is required.

## RESET

A reset function has been made available to reset all sections simultaneously to an output low state. During reset the trigger is disabled. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.
The reset voltage must be brought below 0.8 V to insure reset.

## THE CONTROL VOLTAGE

The control voltage is also made available on the 558/559 timers. This allows the threshold voltage to be modulated, therefore controlling the output pulse width and duty cycle with an external control voltage. The range of this control voltage is from about 0.5 V to Vcc minus 1 volt. This will give a cycle time variation of about $50: 1$. In a sequential timer with voltage controlled cycle time, the timing periods remain proportional over the adjustment range.

## TEST BOARD FOR 558/559

The circuit layout can be used to test and characterize the 558 or 559 timer. $\mathrm{S}_{2}$ is used to connect the loads to either Vcc or ground. The main precaution, in layout of the 558 and 559 circuits, is the path of the discharge current from the timing capacitor to ground (pin 12). The path must be direct to pin 12 and not on the ground buss. This is to prevent voltage spikes on the ground buss return due to current switching transient. It is also wise to use good power supply bypassing when large currents are being switched.

## 558/559 TEST CIRCUIT



558/559 TEST BOARD LAYOUT


FOIL SIDE


558 TWO HOUR TIMER


558 SEQUENTIAL TIMER WITH VOLTAGE CONTROLLED CYCLE TIME (50:1 RANGE)



## NE558 400 Hz SQUARE WAVE OSCILLATOR



A single section of the Quad time may be used as a non precision oscillator. The values given are for oscillation at about 400 Hz . $\mathrm{T}_{1} \approx \mathrm{R}_{1} \mathrm{C}_{1}$ and $\mathrm{T}_{2} \approx 2.25 \mathrm{R}_{2}$ $\mathrm{C}_{2}$ for Vcc of 15 volts. The frequency of oscillation is subject to the changes in Vcc.

559 ASTABLE OPERATION


EXPECTED WAVEFORMS


## sECTION 24 COMMUNICATIONS CIRCUITS

## INTRODUCTION

The following chapter will cover those devices which can be referred to as communications circuits. Such devices as balanced modulators, RF/IF amplifiers, and video amplifiers are included. Many other devices such as the ULN2111 partially fit the communication heading but also fit the consumer category since they are intended primarily for the home entertainment market. These devices will be covered in detail in the consumer section.

## RF/IF AMPLIFIERS

Ideally, semiconductor devices for use in the RF amplifiers should have a high forward transconductance and a low reverse transadmittance, that is, low feedback capacitance. A single transistor may have a high transconductance, but it will also have high reverse transadmittance, making it difficult to fully utilize its high tranconductance in a tuned amplifier.

## DIFFERENTIAL AMPLIFIER



Figure 7-1

There are two multiple transistor circuit configurations available that allow the reduction of the reverse transadmittance. The first circuit, Figure 7-1, is basically a differential amplifier with a high impedance emitter coupling circuit (a current generator). Rearranging the circuit and adding a source, load, and ground result in the circuit of Figure 7-2. The input stage is common collector and the output stage is common base. Therefore, the currents in the collector to base capacitance of the input stage are completely isolated from the input stage. The reverse transadmittance then consists primarily of the stray capacitive reactance occurring in the package in which the device is encased. Figure 7-3 shows the circuit with suitable biasing applied.

The second circuit, Figure $7-4$, is a series transistor connection. When a source and loading are incorporated, it is apparent that
this is a common emitter-common base connection, commonly called a "cascode" circuit. Again, as in the circuit of Figure 7-3, the currents in the collector to base capacitance of the output stage are completely isolated from the input circuitry. The currents in the collector to base capacitance of the input stage do not flow directly to


Figure 7-2

## COMMON COLLECTOR-COMMON

 BASE STAGE WITH BIASING

Figure 7-3

COMMON EMITTER-COMMON BASE AMPLIFIER


Figure 7-4

## REARRANGEMENT SHOWING LOADS AND PARASITIC ELEMENTS



Figure 7-5
ground as in the circuit of Figure 7-3 and some feedback does occur. However, it is negligible because the collector of the first stage is heavily loaded by the emitter of the second stage. Therefore, very little feedback voltage may be developed across it. Figure 7-6 shows the circuit as it might be used. It has a gain capability greater than the circuit of Figure 7-3.
In most RF/IF amplifiers, the circuit designer wishes to operate from a single power supply. To permit this method of operation, a bias must be supplied for the bases of transistors Q1 and Q2.
This bias is obtained by inserting two more diodes, CR1 and CR2, in a series with the bias current resistor R, of Figure 7-7. Two diodes are used to ensure that if either of the transistors, Q1 or Q2, should become saturated the voltage cannot fall low enough to disturb the operation of the current generator.

## COMMON EMITTER-COMMON BASE AMPLIFIER WITH BIASING



Figure 7-6

## ADDITIONAL BIASING TECHNIQUE



Figure 7-7

The final circuit design is shown in Figure 78. The transistors used are of small geometry and have an $\mathrm{F}_{\mathrm{T}}$ of about 700 MHz .
As shown the 510 and 511 configurations are quite similar. The emitters of the current sources are brought out for the 511 so that degeneration may be introduced for better signal handling capability and linearity.


Table 7-1

## CIRCUIT CHARACTERIZATION

The circuit is characterized with " $Y$ " parameters as is common with RF amplifiers used in the frequency range for which this device was designed. Table 7-1 is a summary of the low frequency " $Y$ "parameters of the circuit. The real part of all the parameters remains nearly constant until the operating frequency exceeds 10 MHz , at which time input and output conductances start to rise and the forward transconductance starts to fall.

The reverse transconductance of both the common emitter/common base and common base/common collector configurations is extremely small, the real part being
negligible while the imaginary part corresponds to a capacitance of less than 0.1 pico Farad.
Table 7-1 shows that the forward transconductance, Y21, of both configurations is a function of power supply voltage. A plot of Y21 versus bias network current for the common collector-common base configuration, Figure 7-9, shows that the Y21 is directly proportional to the bias current. A plot of Y21 versus differential input voltage of the common emitter-common collector configuration, Figure 7-10, shows that Y21 may be controlled by changing differential input voltage. These circuit characteristics allow the application of automatic gain control to RF amplifiers made from either circuit configuration.

## CIRCUIT BIASING

Since this circuit is completely devoid of resistors and bias networks, their selection


All resistor values are in ohms
Figure 7-8


Figure 7-9

TRANSCONDUCTANCE vs CONTROL VOLTAGE


Figure 7-10
is at the discretion of the user. This allows the circuit designer complete freedom of choice in operating parameters and transistor. interconnections. His only constraints are the absolute maximum ratings of the device; for example, applied voltage, current, junction temperature, etc.
A typical bias connection, option No. 1, is given in Figure 7-11. Operating currents are determined by the voltage between the base of the transistors Q1 and Q2 and V-, and resistors R1 and R2. The voltage for the bases of Q1 and Q2 is obtained from the temperature compensated voltage divider consisting of R3, R4, and diode CR1. Including CR1 in the bias network compensates for the temperature coefficient of the baseemitter voltage of Q1 and Q2. The current in the voltage divider should be approximately $75 \%$ of the emitter current of Q1 and Q2. Should it become necessary for the collector currents of Q1 and Q2 to be unequal but of the same order of magnitude, then it is suggested that the voltage divider current be selected as the average of the emitter currents. A design example is as follows:

1. Assume operating currents of 2 mA for IC1 and IC2.
2. Assume $V$ - is at ground and $V^{+}$at +12 volts.
3. Assume that the design requires that resistors R1 and R2 be 1000 ohms.
4. Calculate the voltage at the emitters and the bases of Q1 and Q2.

$$
\begin{aligned}
V_{E 1} & =V_{E 2}=I_{C 1} \times R_{1}=1000 \Omega \times 2 \mathrm{~mA}=+2 \mathrm{~V} \\
V_{B 1} & =V_{B 2}=V_{E 1}+V_{B E}=+2 \mathrm{~V}+0.7 \mathrm{~V} \\
& =+2.7 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{a}}=25^{\circ} \mathrm{C}\right)
\end{aligned}
$$

## BIAS CIRCUIT-OPTION 1



Figure 7-11
5. Calculate bias network current.
$\mathrm{I}_{\mathrm{B}}=0.75 \mathrm{I}_{\mathrm{C} 1}, \mathrm{I}_{\mathrm{C} 2}=0.75 \times 2 \mathrm{~mA}=1.5 \mathrm{~mA}$
6. Calculate bias resistors.
$R 1=\frac{V_{E 1}}{I_{B}}=\frac{2 \mathrm{~V}}{1.5 \mathrm{~mA}}=1.33 \mathrm{k} ;$
$R 3=\frac{V^{+}-V_{B 1}}{I_{B}}=\frac{12-2.7}{1.5}=6.2 k$

The bias diode is formed from a planar type transistor which has had its collector and base connected together. It may be operated in either the forward mode or in the reverse breakdown region as a 6.8 V Zener diode. When used as a Zener diode, the operating current should be kept less than 10 mA .
Figure 7-12, option No. 2, shows utilization of the diode in this mode to develop a third

BIAS CIRCUIT-OPTION 2


Figure 7-12
power supply required to bias the bases of the emitter-coupled transistors.

The selection of the load for these circuits is entirely application oriented. If it is to be resistive, its magnitude will be a function of the following amplifier requirements:

1. Output Voltage Swing
2. Voltage Gain
3. Bandwidth

In most applications, the load should be selected to ensure that the transistors do not saturate for the largest positive common mode input voltage.

## DIFFERENTIAL AMPLIFIERS

Differential amplifiers are the easiest circuits to design. The following parameters must be considered in their design:

1. Voltage Gain
2. Output Swing
3. Input Resistance
4. Bandwidth

It may be possible to design a one-stage amplifier with all of these parameters optimized but it is highly unlikely. Usually the designs are a compromise of these parameters. For example, several cascaded stages may be required to obtain the desired gain. The gain and the output swing may have to be compromised so the required input resistance and bandwidth may be obtained.
Until bandwidths of greater than 10 MHz are required, the bandwidth of the amplifier is determined solely by the RC time constant consisting of the load resistance and load capacitance, be it a discrete capacitor, stray
capacitance to ground, or collector to base capacitance (Figure 7-2, 7-5). The 3 dB bandwidth is determined from the following equation:
$F_{3 \mathrm{~dB}}=\frac{1}{6.28 R_{L} C_{L}}$
When $R_{L}=$ total load resistance and $C_{L}=$ total load capacitance
The single-ended output voltage gain $\left(\mathrm{A}_{\mathrm{v}}\right)$ of the circuit may be calculated from the product of the transconductance ( $\mathrm{g}_{\mathrm{m}}$ ) and load resistance ( $R_{L}$ ).
$A v=g_{m} R_{L}$
The transconductance of the 511 may be determined for any collector current from a curve on the data sheet entitled Transconductance vs. Collector Current (EmitterCoupled).

A second method of calculating the gain of a single-ended output differential amplifier uses the relationship between the load resistance and the resistance in the emitter circuit. Figure $7-14$ shows this type of amplifier. The gain is approximated by the ratio of the load resistance to the total resistance in the emitter circuit.

The resistance in the emitter circuit consists of the emitter contact and bulk resistance, $R_{E}$ and the diffusion resistance, $r_{e}$. For the $510 / 511$, RE is approximately 3 ohms per transistor and $r_{e}$ is given by the following equation:
$r_{e}=\frac{k T}{q_{\mathrm{e}}}$
which reduces to:
$r_{e}=\frac{26 m V}{l_{e}}$
at $25^{\circ} \mathrm{C}$ and for emitter currents in milliamperes.

The circuit gain measured from the differential input to one output becomes:
$A_{V}=\frac{R_{L}}{2 R_{E}+2 r_{e}}=\frac{R_{L}}{2\left(3+\frac{26 \times 10^{-3}}{I_{E}}\right)}$
For differential output, the differential gain is twice the single-ended output gain. The input resistance of the differential amplifier in Figure 7-14 may be approximated by the following equation:
$R_{\text {in }}=h F E\left(2 R_{E}+2 r_{e}\right)$

In utilizing this equation, the designer should be cognizant of the fact that the hFE and $r_{e}$ will change as a function of temperature and emitter current. The hFE is typically 125 for collector currents of 1 mA (at $25^{\circ} \mathrm{C}$ ). The output swing capability is determined by the power supply voltage available. The maximum power supply voltage is determined by the absolute maximum ratings of the collector to base voltage of the differential transistors. It is this voltage which sets the maximum peak-to-peak swing for noninductive loads. To maximize the output swing, the collector current is set so that the quiescent output voltage is one-half of the positive supply voltage. A circuit example is Figure 7-15. If, however, the input signal is differential in nature with a common mode



Figure 7-14


Figure 7-15

DIFFERENTIAL AMPLIFIER WITH COMMON MODE INPUT SIGNAL


Figure 7-16
signal relative to ground, the collector operating point must be made more positive to allow for the common mode input signal if nonsymmetrical distortion is to be eliminated. For example, if the input signal is 10 mV peak-to-peak riding a 2 V common mode signal, the collector operating point must be raised according to the following equation:
$\mathrm{v}_{\mathrm{o}}=\frac{\mathrm{v}^{+}+\mathrm{V}_{\mathrm{cm}}}{2}$
When $\mathrm{V}^{+}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=7 \mathrm{~V}$
The circuit of Figure 7-16 is a differential amplifier designed using the following design criteria.
Circuit Design Example: Differential Input, Single-Ended Output Amplifier

## Goals:

1. Gain $=100$
2. Output Swing $=10 \mathrm{~V}$ peak-to-peak
3. Common Mode Range $= \pm 1 \mathrm{~V}$
4. Input Resistance $=5000 \Omega$

Assumptions:

1. $\mathrm{h}_{\mathrm{FE}}=125$
2. Ambient Temperature $\left(T_{a}\right)=25^{\circ} \mathrm{C}$

Solution:

1. The input resistance of a differential amplifier is set by the emitter currents of the transistors. Therefore, in order to obtain the required amplifier input resistance, the emitter currents must be determined first.
a. Find $\mathrm{r}_{\mathrm{e}}$ :
$R_{\text {in }}=h_{\text {FE }}\left(2 R_{E}+2 r_{e}\right)$
$r_{e}=\frac{R_{\text {in }}}{2 h_{F E}}-R_{E}=\frac{5000}{2 \times 125}-3 \Omega$
$r_{e}=17 \Omega$
b. Determine required emitter current to give desired $\mathrm{r}_{\mathrm{e}}$ :
$\mathrm{I}_{\mathrm{e}}=\frac{26}{\mathrm{r}_{\mathrm{e}}} \mathrm{mA}$ at $25^{\circ} \mathrm{C}$
$\mathrm{I}_{\mathrm{e}}=\frac{26}{17}=1.53 \mathrm{~mA}$
c. Once the emitter currents have been obtained, the collector currents (Ic) are easily found:
$I_{C}=I_{e}-I_{b}=I_{e}-\frac{I_{e}}{h_{F E}}$
$I_{C}=1.53-\frac{1.53}{125}$
for all practical purposes
$I C \approx 1.5 \mathrm{~mA}$
2. At this point the emitter currents have been selected to provide the required input resistance and the collector currents have been found. It is now necessary to determine the load resistance that will provide the desired gain.

The voltage gain

$$
\begin{aligned}
(A v) & =\frac{R_{L}}{2 R_{E}+2 r_{e}} \text { or } \\
R_{L} & =2 A v\left(R_{E}+r_{e}\right) \\
& =2 \times 100(3+17) \\
& =4000 \Omega
\end{aligned}
$$

3. Having determined the load resistance, we next determine the collector operating point, $\mathrm{V}_{\mathrm{q}}$.

$$
v_{\mathrm{q}}=\mathrm{V}^{+}-I_{\mathrm{C}} \mathrm{R}_{\mathrm{L}}
$$

when $\mathrm{V}^{+}=12 \mathrm{~V}$

$$
\begin{aligned}
\mathrm{v}_{\mathrm{q}} & =12-4000 \times 1.5 \times 10-3 \\
& =+6 \mathrm{~V}
\end{aligned}
$$

4. The requirement for output swing is 10 V peak-to-peak or the output collector must swing $\pm 5 \mathrm{~V}$ from its operating point. The collector will swing $+6 \mathrm{~V} \pm 5 \mathrm{~V}$ or from +1 V to +11 V .
5. The positive common mode range (CMR) is determined by the most negative excursion of the output collector and will be +1 V . The negative common mode range is a function of the negative power supply and is limited by the $\mathrm{V}_{\text {be's }}$ of the input stage and the saturation voltage of the current source. A "rule of thumb" for determining the saturation voltage of the current source is to assume that it is equal to the $\mathrm{V}_{\text {be }}$ of the transistors. The negative common mode range is then:

Negative CMR $=\mathrm{V}^{-}+2 \mathrm{~V}_{\mathrm{be}}$
The $V_{\text {be's }}$ of the 511 are 0.8 V or less, therefore:

Negative CMR $=\mathrm{V}^{-}+1.6 \mathrm{~V}$.
For the design example, a negative CMR of -1 V may be obtained with a negative power supply of -2.6 V .

V - = Negative CMR -1.6 V
$=-1 \mathrm{~V}-1.6 \mathrm{~V}$
$=-2.6 \mathrm{~V}$

Increasing the negative supply voltage, while staying within the ratings will allow a greater negative CMR to be achieved.
6. The current in the current source transistor, Q3, is set by the resistance of $R_{B}$ and the magnitude of the negative power supply. For the 511, the best current stability is obtained when the bias current in the resistor $\mathrm{R}_{\mathrm{B}}$ is $75 \%$ of the required current source current.

$$
R_{B}=\frac{V^{-}-V_{b e}}{0.75 I_{c 3}}=\frac{V^{-}-V_{b e}}{1.5 I_{e}}
$$

For the design example where $\mathrm{V}^{+}=12 \mathrm{~V}$.
$R_{B}=\frac{12-0.8}{1.5 \times 1.5 \times 10-3}$
$R_{B} \cong 5000 \Omega$

## CASCODE RF/IF <br> AMPLIFIER (CE-CB)

The cascode configuration will be used where the maximum gain is required and where there is no requirement for symmetrical limiting. The circuit of Figure 7-17 is typical. For frequencies below 10Mhz, no particular precautions need to be taken to design a stable amplifier, other than the usual efforts to isolate the output from the input. Because of the excellent input to output isolation and because the gain control voltage has little effect on the input or output parameters, it is not necessary to mismatch the interstage transformers to ensure a stable amplifier that shows no appreciable change in the bandwidth characteristics as the gain is adjusted by the automatic gain control voltage.

Circuit Design Example: Cascode Amplifier (Figure 7-18)

## Goals:

1. Output Voltage Swing $\left(\mathrm{V}_{0}\right)=12 \mathrm{~V}$ peak-topeak
2. Voltage Gain $\geq 10$.
3. Bandwidth $\geq 2 \mathrm{MHz}$ (with 20 pF capacitive load).

## Assumptions:

1. Assume high hfE's (typically 125)
2. $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C}$

Solution:

1. Determine the maximum load resistance It is a function of required bandwidth.

$$
\begin{aligned}
& R_{\mathrm{L}}=\frac{1}{2 \pi \mathrm{fC}}=\frac{1}{2 \pi \times 2 \times 106 \times 20 \times 10-12} \\
& R_{\mathrm{L}}=4.03 \mathrm{k}
\end{aligned}
$$

If $5 \%$ resistors are used, a $3.6 \mathrm{k} \Omega$ is the largest standard value which will ensure that the required minimum bandwidth will be obtained.
2. Determine the required Power Supply Voltage ( $\mathrm{V}^{+}$):
$\mathrm{V}^{+} \geq$Sum of the voltage at the base of the common base transistor (Q2) and the output swing, $\mathrm{V}_{\mathrm{o}}$. The bias voltage at the base of Q2 is set by the reverse breakdown voltage of the 511 bias diode which is used as a Zener diode in this example.
$\mathrm{V}^{+} \geq 6.8 \mathrm{~V}+12 \mathrm{~V}=18.8 \mathrm{~V}$
To allow for power supply fluctuations and measurement tolerances, use $\mathrm{V}^{+}=20 \mathrm{~V}$.
3. Determine the output collector current:
$\mathrm{IC}=\frac{\mathrm{V}^{+}-\mathrm{V}_{\mathrm{q}}}{\mathrm{R}_{\mathrm{L}}}$
where: $\mathrm{V}_{\mathrm{q}}$ is the quiescent dc output level.



Figure 7-19
$\mathrm{V}_{\mathrm{q}}=$ Power supply voltage minus one-half the possible output swing
$\mathrm{V}_{\mathrm{q}}=\mathrm{V}^{+}-\left[\frac{\mathrm{V}^{+}-\mathrm{V}_{\mathrm{b}}}{2}\right]=13.4 \mathrm{~V}$
therefore:
$I_{C}=\frac{20 V-13.4 V}{3600 \Omega}=1.83 \mathrm{~A}$
4. Determine the resistance of $\mathrm{R}_{\mathrm{E}}$ :

The voltage gain of the circuit is a function of the ratio of the load resistance to the resistance in the emitter circuit.

Circuit Gain $=\frac{R_{L}}{R_{E}+r_{e}+r_{C}}$
where: $r_{e}$ is the diffusion resistance and is
$\underline{26 \mathrm{mV}}$
1.83 mA
$r_{e}=14.2 \Omega, \mathrm{~T}_{\mathrm{a}}=25^{\circ} \mathrm{C}$
$r_{c}$ is the emitter contact resistance and is $3 \Omega$.

Substituting in the circuit gain equation from above:

$$
\begin{aligned}
& 10=\frac{3600}{R_{E}+14.2+3} \\
& R_{E}=360-17.2=343 \Omega
\end{aligned}
$$

5. Select the bias network resistors:
a. The 511 data sheet shows that the bias diode, when operated in the reverse breakdown region, has a low dynamic resistance for currents up to 10 mA . The bias current was arbitrarily set at 5 mA , this being a point halfway between the knee of the curve and the 10 mA limit.
b. RX and RY are selected to apply the appropriate bias at the base of Q1. This voltage is determined by the level which must appear across $R_{E}$ to obtain the desired operating current and the base emitter voltage of Q1. In the example, the base voltage of Q1 is +1.3 V . The voltage divider resistor is selected to provide this voltage when the input bias current is $10 \mu \mathrm{~A}$.
In the design, a number of approximations were made. In all but the most critical applications, this design technique will prove quite adequate.
An expansion of the cascode amplifier is the 455 KHz IF strip shown in Figure 7-19.
This amplifier has been designed using "off the shelf" IF transformers. The circuit was built using the NE510 in a 14 dual in-line plastic package. The resulting amplifier has a voltage gain of 66 dB when the gain control input is grounded. Gain, in this instance, is defined as a ratio of dc output voltage at the detector to RMS input voltage. Figure 7-20
is a curve of the gain versus gain control voltage. At the maximum gain setting, the input was set so that there was no output clipping and the dc output voltage was plus 2 volts.

### 10.7MHz LIMITING <br> IF AMPLIFIER

An RF amplifier, using the NE510 in the common collector-common base configuration, is shown in Figure 7-21. Although the common collector/common base circuit has a lower gain than the common emitter/ common collector configuration, it will prove extremely useful when a limiting amplifier is required. When it is operated in this configuration, an input level of 0.3 volts peak-to-peak will cause the maximum realizable output swing, and no further increase in the input signal level will affect the output. In addition, selecting the load impedance so that the output transistor can never saturate will ensure a limiter design having excellent characteristics with a minimum of phase distortion.

Figure 7-22 is a schematic of the IF amplifier using the circuit of Figure 7-21. The intent of the design is to demonstrate the device characteristics and the ease with which the circuit was designed and constructed. The IF frequency used in commercial FM broadcast receivers $(10.7 \mathrm{MHz})$ was selected for the IF frequency for this amplifier so that there would be a basis for comparison.

GAIN vs. CONTROL VOLTAGE


Figure 7-20

COMMON COLLECTORCOMMON BASE R.F. AMPLIFIER


Figure 7-21

When the design was initiated, checking the Y parameters for 10.7MHz showed very little deviation from the dc and low frequency parameters. Since the feedback capacitance was very small, it was decided to use low frequency design techniques and not attempt to mismatch the coupling circuits. It was felt that if the design were made in this manner, and no instability problems occurred, the usefulness of the circuit would be proved. A typical commercial 10.7 MHz IF amplifier has a 3dB bandwidth of 250 to 300 KHz . It was decided to design this amplifier for 300 KHz bandwidth. The bandwidths
of the individual transformers in this design were selected using the equation: Amplifier Bandwidth $(3 \mathrm{~dB})=$ Transformer Bandwidth (3dB) $X \sqrt{2^{1 / n-1}}$ where " $n$ " is the number of transformers. In our case, $n=3$ and $\sqrt{2^{1 / n-1}}$ $=0.5$. Therefore, each transforme $\bar{r}$ must have a bandwidth of 600 KHz . In order to have transformers critically coupled and have a minimum saddle, the primary to secondary winding space is quite large, precluding the use of subminiature transformers for this first design. It was decided to use dual cup core transformers of the type used for many years in vacuum tube IF
amplifiers. Winding data for the coils is given in Figure 7-22. The transformers used were taken from an old receiver and all the windings stripped and rewound. The transformers had a capacitance of about 12 picofarads in the base, so an additional 39 picofarads were added to the transformer externally to obtain the desired tuning capacitance.
The final amplifier designed had the desired bandwidth of 300 KHz and full limiting was obtained with an input voltage at 70 microvolts RMS. No circuit prmblems appeared and tuning was not critical.
10.7MHz LIMITING IF AMPLIFIER


Figure 7-22


Figure 7-23


All resistor values are in ohms

Figure 7-24

## NARROW BAND 60MHz RF AMPLIFIER

The NE510/511 may be used for narrow band amplifiers with center frequencies well above 100 MHz . As an example, an amplifier in the common collector-common base configuration, Figure 7-23, was designed with the following design objectives:
a. Power Gain-maximize
b. Center frequency- 60 MHz
c. Bandwidth ( 3 dB ) -0.5 MHz
d. Power supply -+6 volts
e. Input impedance- 50 ohms
f. Output impedance- 50 ohms

The $Y$ parameters for 60 MHz , as read from the curves in the Appendix, are as follows:

$$
\begin{aligned}
& Y_{11}=0.36+j 1.5=1.54 \angle 76.5^{\circ} \\
& Y_{22}=.03+j 1.1=1.1 \angle 88.5^{\circ} \\
& Y_{21}=3.6+j 9.9=10.5 \angle 160^{\circ} \\
& Y_{12}=j 0.02=0.02 \angle-90^{\circ}
\end{aligned}
$$

With the help of the Linvill technique input and output networks to achieve maximum power gain were calculated. The bandwidth of the amplifier is determined by the output network, since the input network has a relatively broad bandwidth.
The following parameters were measured on a breadboard amplifier:

1) power gain-30dB
2) bandwidth (3dB) -0.5 MHz
3) noise figure -7 dB
4) maximum output swing-300 millivolts RMS across 50 ohms
Because of the very small feedback capacitance of the amplifier, tuning is easily accomplished and input adjustments have very little effect on the output impedance matching and vice versa.

## MODULATORS

Returning to the curve of transadmittance of the 510 versus the differential input voltage, Figure 7-10, it may be seen that if a modulating signal instead of an AGC voltage is applied to the control input, the transconductance of the output transistor and the
output current vary in a like manner. Figure $7-24$ is a modulator circuit. This circuit has been operated with a carrier frequency of 50 MHz and a modulating bandwidth of 4 MHz . A modification of the circuit of $7-24$ is the balanced modulator circuit of Figure 725. The constant current generator is modulated by the RF input. When the balance

BALANCED MODULATOR (SUPPRESSED CARRIER)


Figure 7-25


Figure 7-26


Figure 7-27
resistor is properly adjusted and with no modulation input, no carrier will be present at the output. When a modulation signal is impressed, the collector RF currents of the differential pair of transistors will be unbalanced and a RF signal will be present at the output, the phase of which will depend upon whether the modulation input is positive or negative.

## RF OSCILLATOR/CONVERTER

The 510/511 may be used as an RF oscillator/converter, Figure 7-26, to frequencies as high as 100 MHz . Transistor Q1 in conjunction with a tuned transformer T1 constitutes a variable frequency oscillator of the Hartley type. The base of transistor Q1 is biased through the secondary of transformer T1. Transistor Q3 has its current modulated by the incoming signal from the transformer T3 and obtains its bias through the secondary of T3. T2 is a transformer turned to filter out all but the desired IF frequency. Transistor Q2 acts as a common base, tuned IF amplifier.
Conversion is accomplished in the nonlinear operating region of the base emitter junction of transistors Q1 and Q2. When there is no input signal to transistor Q3, only harmonics of the local oscillator fundamental frequency are generated and no signal can appear at the output because of tuned filter transformer T2. When the current in transistor Q3 is modified by the incoming signal, beat frequencies are generated between the local oscillator frequency and the
incoming signal frequencies and their sum and difference frequencies appear in the currents of transistor Q2. Transformer T2 selects the desired sum or difference frequency for amplification in an IF amplifier.

## DOUBLY BALANCED MODULATOR

The 511 is ideally suited for application as a doubly balanced modulator. A circuit of this type provides double sideband suppressed carrier amplitude modulation. Its output consists of the sum and difference frequencies of the two input signals and their related harmonics. For example, when the inputs are a carrier ( $f_{c}$ ) and a modulating signal ( $f_{m}$ ) the major output is as follows:
$f_{\text {out }}=k\left(f_{c}-f_{m}\right)+k\left(f_{c}+f_{m}\right)$
The output will also contain small amounts of the carrier, modulating signal and their harmonics. However, when the circuit is properly balanced, their effects are minimal.

A circuit example is given in Figure 7-27. The design was done for operation with $\pm 12 \mathrm{~V}$ power supplies with the modulation input referenced to ground to permit direct coupling of the modulation signal for the best low frequency response. If the power supplies are not suitable for some applications, the input signal coupling techniques may be altered; capacitive coupling employed, and power supplies modified. For example, the negative supply input may be grounded, the modulation input may be capacitively coupled and biased at +4 V
leaving the remainder of the circuit configuration unchanged. The lower half of a 511 is merely a current source. It may be replaced with a current source constructed from a discrete transistor or if differential modulation input is available, a resistor.

Re and the modulation balance potentiometer are selected to provide the desired dynamic range capabilities of the modulation input. The voltage developed by the emitter currents across the two RE's and the modulation balance potentiometer should be approximately equal to the modulating signal peak-to-peak amplitude minus 100 mV . Modulating signals exceeding this level will cause distortion. The modulation balance potentiometer is adjusted for minimum modulation signal in the output. In addition to this potentiometer, a carrier balance potentiometer is shown. It should be adjusted to minimize the presence of the carrier in the output. The circuit of Figure 7-28 is a variation of the circuit for Figure 7-27. It eliminates all potentiometers. Carrier and modulation feedthough will not be as small as the circuit of Figure 2-27, but will be quite useful where circuit adjustments must be kept at a minimum. The capacitor between the emitters of Q2 and Q6 should be selected to have a low reactance at the lowest modulating frequency.

## DEMODULATOR

The 511 may be used in demodulator applications also. As an example, the FM stereo demodulator circuit of Figure 7-29 is pre-


Figure 7-28


Figure 7-30
sented. The demodulator FM information is applied to the base of Q3. The collector current of Q3 is switched alternately, by the 38 KHz sub-carrier local oscillator, from the left output load to the right output load. Transistors Q4 and Q5 are driven out of phase with transistors Q1 and Q2 from the 38 KHz local oscillator so as to cancel the 38 KHz component in the outputs. The separation is optimized by applying a small portion of the input signal to the emitter Q6
to cancel unwanted out-of-channel information. For maximum separation, the 38 KHz sub-carrier local oscillator signal should have a minimum second harmonic content. Ideally its waveform should be square with a $50 \%$ duty cycle and have an amplitude of approximately 1 V peak-topeak.
Although doubly balanced modulators are not normally used for audio applications, this type of circuit with a few minor
modifications may prove extremely useful. The isolation amplifier with remotely selected inputs is shown in Figure 7-30. The level adjust/mixing control ( $R_{A}$ ) may be located in a far location and the distance is limited only by the noise $(60 \mathrm{~Hz})$ which may be picked up. Feedthrough from the OFF channel is negligible. Bandwidth is limited only by the capacitive load on the output.
Applications occasionally arise where it is required to select, with a logic signal, one of

## STEREO DEMODULATOR



All resistor values are in ohms


Figure 7-29
two inputs to an analog system; for example, sense amplifiers for magnetic tape or disc readout or other memory systems. The circuit of Figure 7-31 illustrates a 511 application which will perform this function. Differential input transistor pairs, Q1 and Q2 or Q4 and Q5 are selected by turning on current source transistor Q3 or Q6. The bias diode of the 511 is used in its reverse breakdown mode to couple the logic input signal through a standard gate to the level of the current source bases in such a manner that the level at the base of Q3 swings through the fixed voltage level present at the base of Q6 when the logic input goes from a "O" to a "1."

## DIGITAL TO ANALOG <br> CONVERTER

The 511, an extremely versatile device, is readily connected as a dual switched current source. When a number of 511's are connected as current sources, with each current properly scaled, a digital to analog converter may be constructed, as in Figure 7-32. The currents are scaled such that:

$$
I_{n}=\frac{I_{1}}{2^{n-1}}
$$

and are summed in a very low impedance provided by the virtual ground present at the inverting input of the operational amplifier.


BLOCK DIAGRAM-D/A CONVERTER
(4-BIT-16 LEVEL)


Figure 7-32

## DETAIL OF CURRENT SOURCE SWITCH FOR DIGITAL <br> TO ANALOG CONVERTER



All resistor values are in ohms

Figure 7-33

The sum of the currents at the input of the operational amplifier is presented at its output as a positive voltage proportional to the input current. The type of conversion, successive approximation or ripple counter, etc., is controlled by the conversion logic. $\bar{A}$ is the most significant bit (MSB) and $\overline{\mathrm{N}}$ is the least significant bit (LSB). The calibrate potentiometer is adjusted for the desired maximum output when all of the current switches are ON. The zero set is adjusted for a zero output level when all of the current sources are turned off.

The detail of the current switches is shown in Figure 7-33. The diodes CR1 through CR4 are necessary to ensure that the current switches may be adequately driven by typical DTL/TTL gates. The bias resistors, $\mathrm{R}_{\mathrm{b}}$, are selected to provide a current in the bias compensating diodes equal to $75 \%$ of the current in the most significant of the two current sources of each 511.

## ANALOG MULTIPLEXER

Many applications arise where digitally controlled analog switching is required. The circuit of Figure 7-34 illustrates a design using an integrated circuit which is capable of selecting one of two analog signals by digital means. The 511 is connected such that a logical " 0 ", at the control input, permits the associated analog input signal to appear at the common collector resistor while the other analog input signal is rejected. The block diagram of Figure 7-35 shows the connection of four of the circuits of Figure 7-34 to form an eight channel analog multiplex switch. A Signetics 8250, binary to octal decoder, is used to convert a three line binary address to a one of eight signal and present a logic " 0 " to the appropriate 511 switch. The channel capability may be increased by the use of additional 511's and 8250 's with the $D$ (inhibit) input of the 8250 's being used to control the groups of eight.

Analog signals of up to 200 KHz may be switched without amplitude degradation. The bandwidth may be extended to 2 MHz when the collector load resistor is replaced with the input of a common base amplifier, Figure 7-36, thereby reducing the effects of the total parasitic circuit capacitances when many collectors are connected in parallel.
For critical applications, the binary information should be applied to the 8250 inputs simultaneously. For applications where a 50 to 100 nanosecond switching transient may be tolerated in the output, the 8250 inputs may be derived from ripple through counters. In order to eliminate gain differences, from input to input, and minimize the dc shift at the output, the bias and emitter resistors should be matched at $1 \%$ or better. The circuits presented in this memo are but a few of the many possible. The component values shown are not necessarily optimum and should be modified to fit each specific

application. In the application of the 511, the user is cautioned to maintain short leads and maintain input/output isolation as the circuit transistors have gains in excess of unity at frequencies as high as 500 MHz . The user should also note that the isolation contact substrate must always be connected to the most negative point of the circuit. Further information is presented in the Appendix.

## BALANCED MODULATOR

The MC1496 is a monolithic transistor array arranged as a balanced modulatordemodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50 dB at 10 MHz are typical with no external balancing networks required.

Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

## THEORY OF OPERATION

As Figure 7-37 suggests the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals $\mathrm{V}_{\mathrm{C}}$ and $\mathrm{V}_{\mathrm{s}}$.
To accomplish this the differential pairs Q1Q2 and Q3-Q4, with their cross coupled collectors, are driven into saturation by the zero crossings of the carrier signal $\mathrm{V}_{\mathrm{c}}$. With

COMMON BASE AMPLIFIER


Figure 7-36

ANALOG MULTIPLEXER


Figure 7-35


All resistor values are in ohms

## SINGLE SUPPLY BIASING



Figure 7-38
a low level signal, $\mathrm{V}_{\mathrm{S}}$, driving the third differential amplifier Q5-Q6, the output voltage will be a full wave multiplication of $V_{C}$ and $V_{\text {S }}$. Thus for sine wave signals, $V_{\text {out }}$ becomes:
$V_{\text {out }}=E_{x} E y\left[\cos \left(\omega_{x}+\omega_{y}\right) t+\cos \left(\omega_{x}-\omega_{y}\right) t\right]$
From equation 7-21 the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals.

## BIASING

Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single ended or dual supplies.
Internally provided with the device are two current sources driven by a temperature compensated bias network. Since the transistor geometries are the same and since $V_{B E}$ matching in monolithic devices is excellent, the currents through Q7 and Q8 will be identical to the current set at pin 5. Figure 7-38 and 7-39 illustrate typical biasing arrangements from split and single ended supplies respectively.


Figure 7-39

## MODULATOR FREQUENCY SPECTRUM



Figure 7-40

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.
The transistors are connected in a cascode fashion. Therefore sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2 volts is sufficient in most applications.
Biasing is achieved with simple resistor divider networks as shown in Figure 7-39. This configuration assumes the presence of symmetrical supplies. Explaining the dc biasing technique is probably best accomplished by an example. Thus, the initial assumptions and criteria are set forth:

1. Output swing greater than 4 volts $p-p$.
2. Positive and negative supplies of 6 volts are available.
3. Collector current is 2 mA . It should be noted here that the collector output current is equal to the current set in the current sources.
As a matter of convenience the carrier signal ports are referenced to ground. If desired the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at dc ground, the quiescent operating point of the outputs should be at one half the total positive voltage or 3 volts for this case. Thus a collector load resistor is selected which drops 3 volts at 2 mA or 1.5 k ohm. A quick check at this point reveals that with these loads and current levels the peak to peak output swing will be greater than 4 volts. It remains to set the current source level and proper biasing of the signal ports.

The voltage at pin 5 is expressed by
$V_{\text {bias }}=V_{B E}=500 \times \mathrm{Is}$
where $I_{s}$ is the current set in the current sources.

For the example $V_{B E}$ is 700 mV at room temperature and the bias voltage at pin 5 becomes 1.7 volts. Because of the cascode configuration both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence the remaining voltage of the negative supply $(-6 v+1.7 \mathrm{v}=$ -4.3 v ) is split between these transistors by biasing the signal transistor bases at -2.15 volts.
Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that suffi-
cient dc voltage is applied to each bias point to avoid collector saturation over the expected signal wings.

## BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs the output, as mentioned, contains the sum and difference frequencies while attentuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 7-40.
Gain of the 1496 is set by including emitter degeneration resistance located as $R_{E}$ in Figure 7-41. Degeneration also allows the

maximum signal level of the modulation to be increased. In general linear response defines the maximum input signal as
$\mathrm{V}_{\mathrm{S}} \leq 15 \cdot \mathrm{R}_{\mathrm{E}}$ (Peak)
and the gain is given by
$A_{v s}=\frac{R_{L}}{R_{E}+2 r_{e}}$
This approximation is good for high levels of carrier signals. Table 7-2 summarizes the gain for different carrier signals.

As seen from Table 7-2 the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed the modulation level can be increased if $R_{E}$ is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 7-40) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.

## AM MODULATOR

The basic current of Figure 7-41 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown the carrier null circuit is changed from Figure 7-41 to have a wider range so that wider control is achieved. All connections are shown in Figure 7-42.

## AM DEMODULATION

As pointed out in equation 7-21, the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is $0^{\circ}$ phase difference as shown in Figure 7-43.
Amplifying and limiting of the AM carrier is accomplished by the ULN2209. Providing 55 dB of gain, the 2209 also provides symmetrical limiting above $400 \mu$ volts. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then de-

| CARRIER INPUT <br> SIGNAL (VC) | APPROXIMATE <br> VOLTAGE GAIN | OUTPUT SIGNAL <br> FREQUENCY(S) |
| :---: | :---: | :---: |
| Low-level dc | $\frac{R_{L} V_{C}}{2\left(R_{E}+2 r_{E}\right)\left(\frac{K T}{q}\right)}$ | $f_{M}$ |
| High-level dc | $\frac{R_{L}}{R+2 r_{e}}$ | $f_{M}$ |
| Low-level ac | $\frac{R_{L} V_{C}(r m s)}{2 \sqrt{2}\left(\frac{k T}{q}\right)\left(R_{E}+2 r_{e}\right)}$ | $f_{C} \pm f_{M}$ |
| High-level ac | $\frac{0.637 R_{L}}{R_{E}+2 r_{e}}$ | $f_{c} \pm f_{M .} 3 f_{C} \pm f_{M}$, |

## Table 7-2 VOLTAGE GAIN \& OUTPUT

 SPECTRUM vs INPUT SIGNALmodulated by the syncronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 743. Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.

## PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned the out-
put of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 7-44. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become dc while the undesired sum component is filtered out. The dc component is related to the phase angle by the graph of Figure 7-45. At 90 degrees the cosine becomes zero, while being at maximum positive or maximum negative at $0^{\circ}$ and $180^{\circ}$ respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion


Figure 7-42


Figure 7-43


Figure 7-44


Figure 7-45
gain rather than a loss for greater resolution. Used in conjunction with a phase locked loop for instance, the balanced modulator provides a very low distortion FM demodulator.

## FREQUENCY DOUBLER

Very similar to the phase detector of Figure $7-44$, a frequency doubler schematic is shown in Figure 7-46. Departure from Figure 7-44 is primarily the removal of the low pass filter. The output then contains the sum component which is twice the frequency of the input since both input signals are the same frequency.


Figure 7-46

## sECTION 25 COnsumer circuits

## SIGNETICS ENTERTAINMENT IC'S



## HOME ENTERTAINMENT IC'S

Figure 8-1

## INTRODUCTION

The ever increasing voracity of the consumer electronics marketplace has led to a host of integrated circuits which replace discrete devices and simplify the old methods of doing things. For instance home entertainment systems now enjoy the use of integrated power amplifiers, pre-amplifiers, and IF systems on a single chip. More recent advancements have added the Dolby circuit and the CD-4 four channel stereo decoder in monolithic form. The following chapter will cover in detail the numerous benefits of using the new generation of consumer I.C.'s.

## POWER AMPLIFICATION

Optimized for high quality and low distortion the 540 power driver is designed to drive a pair of complementary output transistors.
It features low standby current, 100 mA output capability, low bias current, external current and power limiting, wide power bandwidth and a power supply operating range from $\pm 5 \mathrm{~V}$ to $\pm 25 \mathrm{~V}$.
The 540 power driver is in essence a transconductance amplifier with an extremely linear output current swing of $\pm 100 \mathrm{~mA}$ with a transconductance of 3.3 Amps/Volt. The input stage converts the differential input voltage into current and the remaining circuitry is basically a current amplifier in a class B configuration. Operating in class B allows the device to drive large currents with
a minimum of internal power dissipation while using current gain rather than voltage gain increases bandwidth.

## COMPENSATION

Most designs utilizing the 540 should be limited to gains higher than 40 dB for simplicity of compensation. At this gain level a simple capacitance to ground and a small lead network in the feedback path provide excellent stability and wide bandwidth.

## OPEN LOOP FREQUENCY RESPONSE



Figure 8-2

Because the 540 does possess many op amp features the compensation techniques for lower gains are also of interest. In order to
simplify the precedure the current gain or transconductance is related to voltage gain. The output impedance of the 540 is 5 kohms in parallel with 100 pF . Therefore, the equivalent open loop voltage gain is equal to
(Equation 8-1)

$$
A_{0}=S_{m} \times R_{o}=3.3 \times 5 \times 103=16.5 \mathrm{k}
$$

The frequency response is given in Figure 82. Two methods of compensation can be used although one method allows only the inverting configuration. Figure $8-3$ shows the lower gain configurations, which is valid for both inverting or noninverting configurations. As shown, by increasing the load capacitance the amplifier becomes more stable. Table 8-1 relates the necessary compensation capacitance to the required gain. Changes in bandwidth and slew rate are also given.

## CIRCUIT FOR GAINS LESS THAN 100



All resistor values are in ohms
Figure 8-3

| ${ }^{\text {A CL }}$ | $\begin{gathered} \text { GBP. } \\ (\mathrm{MHz}) \end{gathered}$ | SLEW RATE ( $\mathbf{V} / \mu \mathbf{s}$ ) | POWER BANDWIDTH <br> (KHz) | $\begin{aligned} & C_{L^{1}} \\ & (\mu F) \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{C}_{\mathrm{L}} \\ (\mathrm{pF}) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | 1. | 0.3 | 4.8 | 0.5 | 50,000 |
| 5 | 2.5 | 0.75 | 12 | 0.2 | 20,000 |
| 10 | 5 | 1.5 | 24 | 0.1 | 10,000 |
| 50 | 25 | 7.5 | 120 | 0.02 | 2,000 |
| 100 | 50 | 15 | 240 | 0.01 | 1,000 |
| 200 | 100 | 30 | 480 | 0.005 | 500 |

Table 8-1 540 Gain/Bandwidth Relationships

For closed loop gains of 2 the 540 has characteristics similar to the 741 with the exception of $\pm 100 \mathrm{~mA}$ output capability and little parametric change with capacitance loads up to $50,000 \mathrm{pF}$. Such applications as coaxial line drivers and capacitance bridge drivers come to mind immediately and benefit greatly from this feature.
Another method of compensation applies only to the inverting amplifier configuration as illustrated by Figure 8-4. By placing high frequency attenuation across the input terminals the loop gain is reduced sufficiently to avoid oscillations even at unity gain.


Since signal levels are low at these points the slew rate and associated bandwidth are very good as illustrated by the Bode plots of Figure $8-5$. The peaking exhibited by the gain of 100 configuration is less than 2 dB while the 3 dB bandwidth is 850 kHz . More severe peaking is exhibited by the unity gain amplifier suggesting that the overall phase shift is increasing, but the 3dB bandwidth is over 2 MHz .


Figure 8-5
Gain settings other than those shown require increasing values of capacitance as the gain approaches 0 . The approximate values can be calculated from the expression
(Equation 8-2)

$$
\mathrm{C}=\frac{0.01 \mu \mathrm{Fd}}{\mathrm{RF}_{\mathrm{F}} \text { (kohms) }} \mu \mathrm{Fd}
$$

where $R_{\text {series }}=560 \mathrm{hms}$ and $R_{F}$ is expressed in kohms.
Although 56 ohms was found to be adequate in most cases, slightly less resistance may be beneficial at unity gain while higher values will be satisfactory at higher gains. The formula of Equation 8-2 is only approximate and will depend upon the series resistance used and the capacitance loading present at the amplifier output.

## POWER OUTPUT STAGES

The 540 was designed specifically to drive complementary output transistors for very high output currents. Figure 8-6 illustrates the necessary connections with Figure 8-7 providing a printed circuit pattern and loading diagram.

As shown, typical operational amplifier feedback techniques are used to set the ac gain at the desired point ( 40 dB in this case). Resistor R8 is returned to ground thru a $50 \mu \mathrm{fd}$ capacitor.

At low frequencies the capacitive reactance becomes large causing the amplifier gain to roll off to unity at dc. This is done to prevent dc voltages such as offset voltage from becoming amplified to the level where they might be detrimental to the speaker system.

The selection of power transistors is dictated primarily by the output current capability of the 540 which is $\pm 100 \mathrm{~mA}$. Total harmonic distortion is a direct function of output current also. As seen from the distortion curves in the data sheet the reflected impedance from the emitter followers seen by the 540 should be as high as possible if minimum harmonic and intermodulation distortion is to be realized. Transistor types having betas greater than 50 at 3 amps of current are excellent choices. Such transistor types as the 2N3055, or the 2N5877 npn types and the 2N3789 or 2N5879 pnp types are good choices because their betas are specified at 4 amps and they are relatively inexpensive.


Figure 8-6


At high frequencies additional phase shifts up to 90 degrees can be contributed by the output transistors. Total phase margin in these cases reduces to less than 45 degrees which can cause instability. Miller capacitors of 500 pF should be added from base to collector as shown in Figure 8-6. Close physical leads should be incorporated to assure low lead inductance.

## POWER LIMITING

Power limiting is achieved by placing a resistor network around the output stage as shown in Figure 8-6. R1 and R6 are current sensing resistors with R3 and R4 being voltage sensing resistors. It is the purpose of R2 and R5 to establish a voltage just below the $V_{B E}$ of the current limiter transistor. Only a small additional current through the output devices is necessary to increase the voltage drop sufficiently to activate the current limiters. However, as long as a load is present at the output, the voltage across resistors R3 and R4 will be reduced proportionally to the voltage developed across the load resistor allowing higher currents to be developed only under safe load limits. Typical $\mathrm{V}_{\mathrm{BE}} / \mathrm{I}_{\mathrm{B}}$ curves for the limiter devices can be found in the data sheet. Power dissipation internally to the 540 can become quite high. Especially with maximum power supply voltages it is a good idea to use a clip on heat sink. For example at $\pm 25$ volts the device quiescent current is 20 mA maximum. Therefore internal dissipation is 1 W in excess of package ratings without the use of a clip on radiator.


Figure 8-8

## HIGH POWER AMPLIFIER

Figure 8-8 shows a hook-up of the 540 driving an output stage capable of swinging 95 volts peak-to-peak. Given a 160 hm load the output rms power is then greater than 72 W .

The extended voltage range is achieved by driving the load from a high current output stage which has voltage gain and which is operating from a higher supply voltage. Q1 and Q2 provide current and power limiting for the output stage. Output stage gain is
calculated from the ratio of R1 and R2 such that
(Equation 8-3)

$$
\mathrm{R} 1=\frac{\mathrm{V}_{\text {OUT }}(\text { MAX })}{\mathrm{V}_{\text {OUT }}(540)} \cdot \mathrm{R} 2
$$

This voltage gain is sufficient to amplify the peak 540 output voltage (which depends upon the 540 supply voltage) to the maximum possible output voltage (dependent upon output stage supplies).
Current limiting levels are described by
(Equation 8-4)

$$
R 4=R 8=\frac{750 \mathrm{mV}}{I_{\text {PEAK }}}
$$

By establishing a voltage and current combination to generate the necessary turn on voltage, power limiting is achieved. Power limiting is fixed by the relationship
(Equation 8-5)

$$
\frac{R 5}{2 R 3}=\frac{R_{L}}{R 4} \text { and } \frac{R 6}{2 R 7}=\frac{R_{L}}{R 8}
$$

When defining values of R3, R5, R6 and R7 the current should be approximately 4 mA . This allows sufficient base drive to Q1, and Q2 to assure that full limiting takes place.
The output voltage is defined as 0 volts when the bias current is calculated. Thus for a 50 volt supply the current becomes
(Equation 8-6)

$$
I_{B}=\frac{V_{\text {SUPPLY }}}{R 3+R 5}=\frac{50}{12 \mathrm{k}+56}=4.16 \mathrm{~mA}
$$

A voltage due to this current is developed across resistors R3 and R7. This voltage must be less than 750 mV and is usually selected to be between 300 and 400 mV . As long as the normal load is seen by the amplifier the voltage across the load subtracts from the current limiter VBE voltage. This increases the output current of the amplifier until peak current is reached at full output voltage corresponding to full power.

## SINGLE SUPPLY AMPLIFIERS

When one polarity supply is all that is available, the 540 can be rebiased to perform normally. For instance the 12 volt supply found in automobiles is used by the circuit of Figure 8-9. For proper operation the 540 differential inputs must see bipolar supplies. To achieve this the inputs are returned to one half of the available supply or 6 volts. All circuitry is otherwise basic with the exception of the load. The amplifier output will be 6 volts dc since the amplifier has a dc gain of one. The load must be ac coupled in order to block this voltage from
the speaker. The supply current of the 540 is sensed with a 39ohm resistor for output transistor drive. This method assures that the maximum output swing is equal to the supply voltage less only the saturation voltage of the output transistors. The maximum drive current for the output devices is established by the 56ohm resistor in series with $50 \mu$ Fd capacitor from the 540 output to ground. The 5600hm resistor in parallel with 5000 pF provides an output voltage reference as well as high frequency stabilization.

## HAMMER DRIVER

The 540 can also be used as a driver for relays, solenoids, motors, or any other mechanical devices. Figure 8-10 demonstrates some typical connections. The load can either be push pull or (as in the conventional hook-up) single ended. In the push pull connection the load is driven in either the positive, negative, or both arms of the output. Depending on the input pulse polarity, either output can be selected. In addition, the output can be gated off by applying a voltage via a current limiting resistor to either pin 5 or 6 between pins 1 and 10.

The current required for these limiters is approximately 1 mA for pin 1 and $100 \mu \mathrm{~A}$ for pin 5.

In such applications the required input signal is defined by the maximum load voltage divided by the closed loop gain.



## DESCRIPTION

The NE541 High Voltage Power Amplifier has been designed primarily for use with audio equipment. Figure $8-11$ shows the typical circuit configuration for evaluation of the following parameters.

The amplifier is basically a class AB1 type giving very high current gain (typically 90 dB or better within the audio frequency spectrum of 20 Hz to 20 kHz ). The high gain of the amplifier permits relatively small signal levels from a preamp stage to be used. If the amp stage uses a large feedback factor, the linearity of the preamp can be improved. The NE541 should operate with closed loop gains of 30 dB or higher to permit wide band operation with relatively high capacitive loads at its output. Therefore, a preamp whose output is $200-300 \mathrm{mVrms}$ will result in output levels of $10-20 \mathrm{Vrms}$ from the NE541.

The NE541 always requires some capacitance on its output. The device has been designed with some positive feedback which aids in the high slew rate and high gain capability. The output capacitance maintains the stability of the device.
The NE541 has built-in short circuit protection. A sensing resistor in series with the output drivers turns on a base current shunt when the output current goes too high. This limit is set to approximately 100 mA typically, but will have variations due to processing and manufacturing tolerances. In addition to the built-in short circuit protection, the current can be limited by use of external circuitry as shown in Figure 8-12.
The wide band operation of the device as seen in Figure 8-13 plus the nominal low offset voltages inherent to the amplifier (VOS and los) will permit the usage of the device in several other areas, such as instrumentation amplifiers, servo drivers and power regulators.

Several input configurations can be incorporated to add either bass or treble boost to the system. These configurations should be evaluated by the designer to best fit his needs. For high power systems additional speaker compensation can be included.

## FM DETECTOR-LIMITER

The ULN2111 was designed primarily for FM and TV sound IF applications. This circuit is comprised of a three stage limiting amplifier with a voltage gain of 60 dB and a balanced quadrature phase detector as shown in Figure 8-17.
Comprised of three identical differential amplifier stages, the amplifier-limiter is directly coupled thru emitter followers. The direct coupling is possible by using an


Figure 8-12


## BASIC OPERATING EQUATIONS

Lower 3dB

$$
f=\frac{0.16}{R_{f} C_{f}}
$$

Bass Emphasis

$$
\mathrm{e}_{\text {in }}^{\text {pin } 6}:=\frac{10 k}{R_{\text {in }}}\left(\frac{1+\mathrm{S} 1}{1+\mathrm{S} 2}\right)
$$

where: S1 = jwC1R1

$$
S_{2}=j w C 1(R 1+R 2)
$$

Amplifier Gain (Midband)

$$
A C L=20 \log _{10} \frac{10 k+R_{f,}}{R_{f}} R_{f} \text { in } k \Omega
$$

$$
\text { Loop gain } \approx 90 \mathrm{~dB}-\mathrm{ACL}
$$


internally generated voltage reference formed by a series diode string, dc level shifting between stages, and overall dc negative feedback.

To provide for flexibility in the driving of different phase-shift networks, two limiter outputs are available. One provides the fully limited output voltage of 1.4 V peak to peak which is applied directly to the coincidence detector. A second low voltage output supplies the same signal at an attenuation of -20dB.

FM detection is accomplished with the balanced product detector shown in Figure 818. As has been pointed out in the phase detector discussions of chapter 7 the bal-


Figure 8-15
anced product detector produces an output dependent upon the phase of the two input signals. By phase shifting, with a simple LC network, one signal from the other by $90^{\circ}$, the carrier signal becomes non-existent and the audio modulation is recovered. For any level of the inputs V1 and V2 of Figure 8-18 the output voltage becomes
(Equation 8-7)

$$
V_{0}=\frac{V_{R}}{t} \int_{0}^{t} U 1(t) U 2(t) d t
$$

(Equation 8-8)
where

$$
U_{1}=\tanh \frac{V_{1}(t)}{2 k T / q}
$$


(Equation 8-9)

$$
\mathrm{U} 2=\tanh \frac{\mathrm{V} 2(\mathrm{t})}{2 \mathrm{kT} / \mathrm{q}}
$$

(Equation 8-10)
and

$$
V_{R}=\frac{I_{0} R}{2}
$$

Equation 8-7 shows that the output is proportional to the product of the two input functions $U(t)$.

The U function accounts for any symmetrical limiting in the base-emitter junctions and can be approximated for linear opera-

SCHEMATIC OF ULN2111


All resistor values in ohms
Figure 8-17

tion and hard-limiting by the input voltage itself or by switching function, respectively.

There are two modes of operation: high level switching and low level switching. The frequency-transfer characteristics for each operating mode are given by:
(Equation 8-11)

$$
\frac{V_{0}}{V_{R}}=\frac{2}{\pi} \arctan a(\text { high level) }
$$

(Equation 8-12)

$$
\frac{V_{0}}{V_{R}}=\frac{2}{a}\left(\frac{\left|V_{1}\right|_{0}}{2 k T / q}\right) \frac{a}{1+a^{2}} \text { (low level) }
$$

(Equation 8-13)
where

$$
A=2 Q \frac{\Delta F}{F_{0}}=\begin{aligned}
& \text { normalized frequency } \\
& \text { deviation }
\end{aligned}
$$

and
$|\mathrm{V} 1|_{0}$ is the magnitude of V 1 at the center frequency.

Equation 8-17 and 8-18 are plotted in Figure 8 -19. For low level operation, the amplitude of the bell-shaped response of the tuned circuit provides the response fall-off on either side of the center frequency, and the familiar S-shaped transfer function is obtained. The peak-to-peak separation of the source is directly related to the 3 dB bandwidth of the tuned circuit. For high-level operation and within a large range of frequency deviations, the amplitude response of the network transfer function is eliminated, and the response is directly that of the phase-shift properties of the LC network.
The conversion efficiency, $V_{F}$ defined as the slope of the transfer characteristic at the center frequency, can be shown to be:
(Equation 8-14)

$$
V_{F}=\left(\frac{d V_{0}}{d a}\right)_{a=0}=\frac{2}{\pi} V_{R} \tanh \frac{\left|V_{1}\right|_{0}}{2 k T / q}
$$

Figure 8-20 shows the measured values of the conversion efficiency as a function of the magnitude of the driving voltage V1, at the center frequency 4.5 MHz .

## DEFINITIONS

In order to properly utilize the design advantages offered by the ULN2111 it is necessary to clarify those quantities used in design evaluations.

Center Frequency-the fm modulated carrier frequency designated by $f_{o}$.
Frequency Deviation-the amount of frequency change of the carrier designated $\Delta f$
Network Selectivity-the $Q$ of the tuned circuit used for phase shifting $\left(Q=\frac{\text { fo }}{B W}\right.$ and should be greater than 10) BW

Conversion Efficiency-the slope of the fm " S " curve specified by ( dV OUT $/ \mathrm{d} \theta$ ) $=$ VOLTS per radian.

Normalized Deviation-For simple LC networks the quantity $2 \mathrm{Q} \frac{\Delta \mathrm{F}}{\text { fo }}$ is designated by the letter a.

## GENERAL CONSIDERATIONS

The ULN2111 is very versatile and easy to use. Only a few general requirements are needed.

1. As with any integrated circuit, especially those operating at high frequencies, the power supply at pin 13 should be bypassed with a ceramic disc of the $05 . \mu \mathrm{fd}$ value range.
2. Amplifier gain is 60 dB at high frequencies. This can be troublesome unless
good high frequency layout techniques are practiced. Ground planes are very helpful and physical separation of inputs and outputs is mandatory.
3. A dc path less than $300 \Omega$ should be provided between pins 4 and 6.
4. Decoupling capacitor leads at pins 5, 6, and 12 should be as short as possible.
5. The maximum ac load current can be increased by adding an external resistor between pins 1 and 7 . The minimum value for this resistor is $800 \Omega$, giving a minimum load current of 4 mA RMS.
6. A dc path less than $100 \Omega$ shall be provided between pins 2 and 12. No other biasing provisions are required.

CALCULATED TRANSFER CHARACTERISTICS FOR HIGH AND LOW LEVEL CASES


Figure 8-19

MEASURED CONVERSION EFFICIENCY OF THE MONOLITHIC FM DETECTOR


Figure 8-20

## PERFORMANCE

In an FM detector and limiter, the major figures of merit include recovered audio amplitude, dynamic range, and total harmonic distortion.

Audio recovery is affected primarily by the resonant LC network and the injection level at the detector input.

To obtain a proper value for audio recovery, specific characteristics of the S curve are recommended. A choice of slope of the $S$ curve gives a specified value for $d V / d F$, which is the basic expression of audio recovery. A choice of a peak-to-peak separation desired and a choice of peak-to-peak voltage required at the nodes of the $S$ curve determine the $Q$ of the LC resonant network and injection level.
The peak-to-peak separation is usually defined by the service for which the system is intended. This value is 550 kHz for $F M$ and 150 kHz for TV. An approximation of the circuit $Q$ can be made by the equation:
(Equation 8-15)

$$
Q=\frac{F_{0}}{\Delta f}
$$

where $f_{0}$ is the center frequency and $\Delta f$ is the 3 dB attenuation bandwidth. For TV service, the value of circuit $Q$ is approximately

$$
Q=\frac{4.5 \times 106}{150 \times 10^{3}}=30
$$

Although the desired circuit $Q$ is fairly low (indicating a high-L network), it is desirable to use a high-C network. The input to the detector introduces some variable capacitance. This can be minimized through the use of at least 100 pF as the $C$ part of the resonant circuit. Inductor choice, along with this capacitance value, yields a network with a Q somewhat higher than desired. This can be reduced by using a paralleled resistor across the network.

Figure 8-21 shows the transfer characteristic for a simple LC network, while Figure 822 shows the ULN2111 FM Detector and Limiter used for TV interfacing.

Typical driving capabilities of the ULN2111 at 4.5 MHz are shown in Figure $8-23$.

ULN2111A Driving Capabilities at $f_{0}=$ 4.5 MHz

| Fig. | $\mathbf{R}_{L}(\Omega)$ | $\Delta \mathbf{f}=\mathbf{7 . 5} \mathbf{k H z}$ | $\Delta \mathbf{t}=\mathbf{2 4 k H z}$ | Remarks |
| :---: | :---: | :---: | :---: | :---: |
| A | 2000 | 220 | 650 | No Clipping |
| B | 200 | 130 | 400 | No Clipping |
| C | 200 | 220 | 650 | Clipping at <br> $V_{0}=500 \mathrm{Vrms}$ |

## TRANSFER CHARACTERISTICS FOR A SIMPLE LC NETWORK

> OUTPUT = $f$ (NORMALIZED DEVIATION) (The units along the vertical axis are arbitrary units.) Linear mode: Operation of the FM detector with no limiting after the phase shift network.

NOTES

1. $V_{F}$ defines the slope of the FM transfer characteristic, at origin:

$$
V_{t}=\frac{d V_{\text {out }}}{d a} \text { at } a=0
$$

$V_{F}$ is primarily a function of bias current in the detector and injection voltage.
$V_{F}$ will decrease with decreasing $V_{C C}$ or $V_{i n j}$.
2. $a=$ normalized frequency deviation:
$A=\frac{20 \Delta F}{F_{0}}$
$a=1$ for peak deviation
Figure 8-21

## TV INTERFACING



All resistor values are in ohms
Figure 8-22


Figure 8-23

The final component required is a small decoupling capacitor placed between the network and the low amplifier output. To insure linear detector operation, the reactance of this capacitor should be substantially large, as compared to the impedance of the tuned circuit at resonance.

The voltage developed across the simple tank circuit is applied to the other two balanced gates of the coincidence detector through emitter follower Q1, which provides a capability for monitoring the LC network tuning without any appreciable loading effects. It also reduces, to a great degree, the capacitance reflected to a tuned circuit, leading to a negligible shift in the tuning as a function of incoming signal strength.

When designing the LC network it is necessary to provide the following requirements:

1. Capacitively drive the network from low impedance (pins 9 or 10).
2. Pins 2 and 12 should see a dc path less than 100 ohms.
3. The required $\mathrm{V}_{2}$ (Figure 8-18) must be supplied at pin 12 by the network.
4. The phase of the network at fo must be $\pi / 2$ or an odd multiple thereof.
5. To minimize output distortion a maximum normalized deviation (a) of less than .3 should be used.

Figure 8 -24 gives the recommended networks for use at 10.7 MHz and 4.5 MHz .

|  | COMPONENT VALUE |  |
| :--- | :---: | :---: |
|  | TV 4.5MHz | Fm $\mathbf{1 0 . 7 M H z}$ |
| L Inductance | $7-14 \mu \mathrm{H}$ | $1.5-3 \mu \mathrm{H}$ |
| L Nominal Q | 50 | 50 |
| (unloaded) |  |  |
| L DCResistance | $50 \Omega$ | $50 \Omega$ |
| CA $_{\text {A }}$ | 3 pF | 4.7 pF |
| CB $^{\text {R1 }}$ | 120 pF | 120 pF |
| Network Q | 20 k | 3.0 K |
|  | 30 | 20 |

The other factor governing audio output is the injection value at the input to the detector. The optimum value is 60 mVrms at the resonant frequency of the network. Figure 8-20 shows a normalized plot of $V_{\text {inj }}$ as a function of $\mathrm{V}_{\mathrm{f}}$, where $\mathrm{V}_{\mathrm{f}}$ represents a normalized output for any single LC network. Note that the output ( $\mathrm{V}_{\mathrm{f}}$ ) has a linear relationship to $\mathrm{V}_{\text {inj }}$ up to approximately 50 mV . Above this value, the function breaks into a curve, then flattens out, indicating that the detector is in a switching mode.
Figures $8-25$ and $8-26$ demonstrate the detector operation in the linear (low injection) mode and the switching (high injection) mode. Note that in the linear mode, a greater portion of the Scurve is linear, thus producing lower distortion than in the switching mode. For best operation, the low injection mode is recommended where $V_{\text {inj }}$ is set
as high as possible. The optimum injection value is 60 mVrms .


Figure 8-24

## FM TRANSFER CHARACTERISTICS LOW Vij OPERATION



Figure 8-25

## FM TRANSFER CHARACTERISTICS HIGH Vij OPERATION



Figure 8-26

## Introduction

The phase locked loop (PLL) has been used for many years in consumer equipment. Due to the nature of FM STEREO MULTIPLEX SYSTEMS, where prime importance is the channel separation, discrete systems lacked the tracking ability over wide temperature and voltage ranges to be done economically.
The development of the monolithic PLL and improvements in IC processing has made the Phase Locked Loop FM Stereo Multiplexer Decoder a reality.

## Major Advantages

The economic advantages in using the PLL multiplex decoding system are not only cost reduction, by eliminating peripheral components, but the man hour cost reduction by eliminating turning coils, thereby eliminating tedious alignment procedures.
The cost advantages are extremely signifcant and are in addition to the following:

- 45 dB Channel Separation
- Automatic Stereo/Mono Switching
- Stereo Indicator Lamp Driver With Current Limiting
- High Impedance Input-Low Impedance Outputs
- 70dB SCA Rejection (Subsidiary Carrier Authorization)
- One Adjustment for Complete Alignment
- 10 V to 16 V Supply Voltage Range


## FM Stereo Multiplex Subcarrier and Pilot

The two (2) basic signals differentiating an FM stereo multiplex signal from an FM monaural signal are the 19 kHz pilot and the 38 kHz subcarrier. The frequency and phase relationship of these signals is well defined.
Earlier systems had to reconstruct the 38 kHz subcarrier by using the 19 kHz pilot. This system required frequency multipliers and selective filters (coils). Since maximum channel separation is directly related to proper phasing, alignment procedures were extremely critical and therefore expensive. In addition, long term stability and performance were degraded due to component aging, and temperature.
Use of the PLL as the multiplex decoder eliminated these short comings since the phase accuracy of the 38 kHz signal is limited only by the loop gain of the system and the free running oscillator stability. Both of these parameters are easily controlled, providing easy, rapid adjustment and excellent long term stability.


## General Description

The $\mu \mathrm{A} 758$ is a monolithic Phase Locked Loop FM Stereo Multiplex decoder using the 16-LEAD Dip AA Package. This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The $\mu \mathrm{A} 758$ operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust a potentiometer to set oscillator frequency. No external coils are required. The $\mu A 758$ is suitable for all line-operated and automotive FM Stereo Receivers.

Referencing Figure 8-27
The upper row of blocks comprises the PLL which regenerates the 38 kHz subcarrier, necessary for multiplex signal demodulation. The basic 76 kHz generator is voltage controlled, and is divided by 2 to insure a $50 \%$ duty cycle 38 kHz internally generated signal. This symmetry is necessary for maximum left/right channel separation and SCA rejection (band centered at 67 kHz ). Dividing the 38 kHz by 2 generates the 19 kHz signal necessary to lock on to the incoming pilot signal. A second 19 kHz signal is generated which is in quadrature to the first internally generated 19 kHz signal and in phase with the pilot. This second 19 kHz is mixed in a quadrature (synchronous) phase detector to operate the stereo switch and lamp driver circuitry.
When a stereo signal is present, the stereo
switch enables the stereo demodulator and when a stereo signal is not present the demodulator is disabled allowing the system to reach optimum noise performance.

## Functional Operation

To aid in understanding the system operation, the $\mu \mathrm{A} 758$ equivalent circuit has been broken down into subsections as follows. Reference Figure 8-28.

I Buffer Amplifier and Bias Supplies
II Demodulator
III Stereo Switch and Lamp Driver
IV Voltage Controlled Oscillator
V Frequency Dividers
VI Pilot Phase and Amplitude Defectors
SIGNETICS LINEAR INTEGRATED CIRCUITS • $\mu \mathbf{A} 758$


## I Buffer Amplifier and Bias

 Supplies (Figure 8-29)The zener diode Z , and its associated transistors generate a 6 V internal voltage reference source. From this 6 V reference, additional bias levels are established via resistors R3, R4, and R5. In addition transistor Q7 acts as the control source for several current mirrors; Q11 in the Buffer Amplifier, Q43 and Q44 in the Stereo Switch and Lamp Driver (III) and Q67 and Q73 in the Voltage Controlled Oscillator (IV).

The input Buffer Amplifier (Q8, Q9) level shifts the composite multiplex input signal to 2 levels each in phase with each other.

Transistors Q10 - Q13 amplify this same signal by the ratio of:

$$
A=\frac{R_{14}}{R_{13}}
$$

This amplified signal, the gain of which is independent of supply voltage variation, is fed to the Pilot Phase and Amplitude Detectors (VI).

## II Demodulator (Figure 8-30)

The basic demodulator, Q25-Q30, is a fully balanced detector similar to standard phase locked loop types. The addition of resistors R29, R30, and R31 introduces a small offset to allow a small multiplex signal in the collector of Q30. This signal compensates the cross talk components inherent to the synchronous switching demodulation process.
Switching to the left and right channels is accomplished through Q25 and Q26 when the 38 kHz drive is present at their bases. This occurs when Q33 is "ON." When Q33 is off, a dc bias is placed at the bases of Q25 and Q26 through resistors R32 and R33, this automatically converts the system to monophonic operation.
Supply voltage rejection is accomplished at the demodulator outputs by converting the audio to current supplies in Q23 and Q24. The voltage developed across pnp transistors is
$\mathrm{V}_{\mathrm{e}}=\left(\mathrm{V}^{+}+\mathrm{V}_{\text {mod }}\right)-\left(\mathrm{V}_{\mathrm{be}}+\mathrm{V}_{\mathrm{D} 1}+\left[\mathrm{R}_{22} \mathrm{i}_{\mathrm{ac}}\right]+\mathrm{V}_{\text {mod }}\right)$
where $\mathrm{V}_{\mathrm{be}}=$ base-emitter voltage across Q22 and Q23
$\mathrm{V}_{\text {mod }}=$ modulation on the power line
$\mathrm{V}_{\mathrm{D} 1}=$ diode drop in D21
$\left(\text { R22 }^{2}\right)_{\text {iac }}=$ voltage drop due to current in the demodulator
Simplifying the above reduces to
(Equation 8-16)

$$
V_{e}=V^{+}-\left(V_{b e}+V_{D 1}+R 22 i_{a c}\right)
$$

The output voltage developed is



Figure 8-30
(Equation 8-17)

$$
V_{\text {out }}=\left(\frac{V_{e}}{R 21}\right) R_{\text {ext }}
$$

where $R_{\text {ext }}=$ external resistor
The output voltage at pins 4 and 5 are provided through 1.3 k resistors driven by Emitter Followers Q21 and Q24.

## III Stereo Switch and Lamp Driver

 (Figure 8-31)The pilot amplitude detector differential voltage is sensed by the differential amplifier Q41 and Q42. This pair in conjunction with their load resistors (R41, R42) control amplifiers Q45, Q46. Positive feedback action is achieved through Q47, R50, Q50 and R46 (which turns off Q44).

The turn on threshold is the differential input voltage required to overcome the offset voltage in R43 times the current summation of IR44 and IR45. When the lamp is ON, Q44 is off and the differential voltage across R43 is reduced by the amount (l $\mathrm{R}_{45} \times$ R43), which means a lower turn off voltage is required. This voltage difference is referred to as the switch hysteresis.
Transistors Q48 senses the current across R51 which therefore controls the maximum current in the Stereo Indicator Lamp.
(Equation 8-18)

$$
I_{\max }=\frac{V_{\mathrm{be}} \mathrm{Q} 48}{\mathrm{R} 151}
$$

## IV Voltage Controlled Oscillator

(Figure 8-32)
The basic oscillator Q71 - Q79 is an RC relaxation type which generates a positive low duty cycle, 76 kHz output. The frequency is established by equations $8-19$ and 8 20.

The control voltage from the phase detector into the transconductance amplifier Q61 Q69 converts the differential error to a bidirectional single ended current drive to the oscillator.
Voltage on the capacitor is compared with the set voltages by the differential input stage Q71, Q72. This feeds Q74, Q75. The output of Q75 drives a PNP inverter, Q76, (whose action eliminates power supply modulation as described in the demodulator section of this note), when these set limits are reached the direction of charge reverses.


Figure 8-31


Figure 8-32

Lower set voltage is set by R79, R80, and the regulated 6 V supply. The upper set voltage $\left(\mathrm{V}_{\mathrm{H}}\right)$ involves two (2) additional resistors R77 and R78 and is established when Q76 turns on Q77. Both set levels are referenced to the regulated 6 V supply and are therefore dependent only on resistor ratios. (Proper design layout should also eliminate temperature variations.)

Capacitor charging is through Q78 and R8 and discharging through the external fixed resistor.

Equations 8-19 and 8-20 of Figure 8-33 are first order expressions for the change and discharge periods.

Q79 supplies a positive output pulse necessary to operate the 38 kHz dividers.

## V Frequency Dividers

## (Figure 8-34)

Transistors Q91 through Q94 form a simple divide-by-two circuit which converts the pulse output from the 76 kHz oscillator to a 38 kHz square wave (reference 5 ).

The divider changes state during the positive excursion of the input pulse supplied from the emitter of Q79 in the oscillator. Initially, when the input is low, Q91 and Q92 are OFF and we may arbitrarily assume Q93 is ON and Q94 is OFF.

As the potential on the input rises, Q91 starts conduction before Q92 because the emitter of Q91 is at a lower potential than the emitter of Q92. (The emitter of Q91 is connected through R95 to the collector of Q93 which is in saturation, whereas the emitter
of Q92 is at the $V_{B E(O N)}$ potential of Q93). Since Q91 is ON, the current from both R92 and R93 flows through the emitter of Q91 into R95. As this current increases, the rising voltage at the emitter of Q91 turns Q94 ON which removes base drive to Q93 and turns it OFF, thus producing a change of state in the divider. Even though the relative potentials at the emitters of Q91 and Q92 are now reversed, current continues to flow in Q91 for the duration of the positive input because Q92 is held OFF by Q91. When the input returns to a low potential,

Q91 turns OFF. The divider remains in its present state until driven by the next positive going input.

Oppositely phased 38 kHz outputs to the demodulator are taken from the collectors of Q93 and Q94. Transistors Q95 and Q96 are used to drive the two 38 kHz dividers.

The 38 kHz Quadrature Divider has an identical configuration to the 76 kHz divider. A change of state occurs with each positive excursion of the 38 kHz input signal from the emitter of Q96.


19 kHz outputs to pilot amplitude and phase detectors.
Figure 8-34

The 38 kHz In-Phase divider contains a bistable pair, Q113 and Q114, steered by inputs into Q111 and Q112, (a 38 kHz input from the collector of Q95, and 19 kHz inputs from the bases of Q103 and Q104). If the 19 kHz input to the base of Q111 is high when the 76 kHz divider turns Q95 ON, Q111 conducts and removes drive to Q114, changing the state of the bistable pair, Q113 and Q114. The bistable remains in this state until the next 38 kHz turn on of Q95 which, this time, turns Q112 ON, removes drive to Q113 and resets the bistable pair. The resulting 19 kHz output from Q113 and Q114 is at 90 degrees to the Quadrature Divider output with no ambiguity in phasing.

## Pilot Phase and Amplitude Detectors

The pilot phase detector and pilot amplitude detector as shown in Figure 8-35 are synchronous, balanced chopper types which develop differential output signals across external filters. Back-to-back NPN transistor pairs are used for each switch to insure minimum drop regardless of signal polarity without reliance on inverse NPN beta characteristics.
The chopper transistors (Q121 through Q124), in the phase detector are driven from the 38 kHz Quadrature Divider through transistors Q125 and Q126. The input signal is supplied from lead 12 through resistors R125 and R126. A differential output is developed across the loop filter, comprised of resistors R123 and R124 and the external R-C network between leads 13 and 14.
The pilot amplitude detector (Q131 through Q136), has an identical configuration to the phase detector. Since it operates with drive which is in phase with the pilot signal 90 degrees from the drive to the phase detector), its output is proportional to the amplitude of the pilot component of the multiplex signal. The differential output at leads 9 and 10 is filtered by the external capacitor on these two leads.
A reference 19 kHz square wave signal is taken from the collector of drive transistor Q136 through resistor R137 to lead 11. It has the same phasing as the pilot contained in the multiplex input signal.

## STEREO PREAMPLIFIERS

## Introduction

Stereo preamplifiers have come into greater and greater demand with the increased usage of tape recorders. With stereophonic recording systems, the need increased to have multiple devices in the same package to insure greater thermal tracking and packing density, without sacrificing performance.



The NE542, LM381, LM382, LM387 all qualify as low noise dual preamplifiers. The LM381 and LM382 are 14 pin dual in line devices, while the NE542 and LM387 are 8 pin dual in line devices.

All of the above devices have greater than 100 dB open loop gain and $(15-20) \mathrm{MHz}$ gain bandwidth products. In selecting the proper "low noise" preamplifier several factors must be considered.

1 Frequency shaping characteristic required.
II Closed loop response with respect to a system reference level.
III Response of the record/playback head.
IV System distortion requirements.
$\checkmark$ Response of the tape used.

The following will deal with items I, II, IV.
When approaching the design criteria of Item 2, the designer should be concerned with the open loop device characteristics.

These characteristcs will aid in determining the maximum boost available, knowing that a specific loop gain (open loop gain minus closed loop gain) will be necessary to keep the system distortion low and maintain the output impedance of the "Iow noise" preamplifier constant over the required operating frequency range.

## EQUALIZATION CRITERIA RIAA Equalization

Recording music in the medium of plastic discs is similar to that of magnetic tape in that neither system exhibits a linear amplitude vs frequency response. Compensation is therefore necessary with records as it was with tape. The standard equalization is known as the RIAA curve and is shown in Figure 8-36, with its corner or turn over frequencies.

Many phono cartridges do not require preamplification. The ceramic and crystal types produce voltage larger than 100 mV .

STANDARD RIAA EQUALIZATION CURVE


Figure 8-36

Magnetic types, however, produce small voltages in the neighborhood of 5 mV and require preamplification.

RIAA standards call for a maximum recording velocity of $21 \mathrm{~cm} / \mathrm{sec}$ for stereo discs. This worst case velocity describes a bound for the preamplifier gain because the input signal at this velocity is maximum. The maximum undistorted output voltage of the PA239 is 1.25 volts rms. This voltage divided by the output voltage of the cartridge at $21 \mathrm{~cm} / \mathrm{sec}$ velocity defines the highest gain permissible without distortion. This maximum is assumed to be 40 dB at 1 kHz for the following example. As seen from Figure 836 , the RIAA curve accounts for 20 dB base boost from 50 Hz to 500 Hz and 20 dB of treble out from 2122 Hz to 21 kHz .

## NAB TAPE EQUALIZATION

Recording and playback characteristics of magnetic tape and record/playback heads are not flat but exhibit a loss at high frequencies and a boost at lower frequencies. To obtain an overall flat frequency response and improved signal to noise ratio, the audio signals are equalized by boosting the higher frequencies in amplitude before recording. Playback amplifiers must exhibit bass boost to remove the effects of pre-emphasis for an overall flat response.

Known as the NAB equalization curve, the standard deemphasis employs attenuation from the turnover frequency of 50 Hz to the turnover frequency of 3180 Hz for $71 / 2 \mathrm{lps}$ recording. The slower recording speed of 3.75 lps employs turnover frequencies of 50 Hz and 1326 Hz . These curves are shown in Figure 8-37. A reference level of $800 \mu \mathrm{~V}$ head sensitivity at 1 kHz is also used by the NAB.


## STEREO PREAMPLIFICATION

The voltage level appearing at the output of tape playback heads and some phono car-
tridges are too small to be useful without a large amount of low noise preamplification. In addition to providing low noise amplification, the preamplifier should possess enough open loop gain so that the RIAA and NAB equalization curves can be produced in the feedback networks of the amplifier.

The following paragraphs describe the characteristics and applications of the 542, LM381/382 and the PA239. These devices provide a matched pair of amplifiers which have been specifically designed to minimize amplifier noise and maximize signal to noise ratio.

## 542 DEVICE DESCRIPTION

The NE542 is a dual low noise amplifier with 104 dB open loop gain produced by two stages of voltage gain followed by one stage of current gain.

In the design of low noise devices special attention must be focused on the input stage. If differential topography is used, the stage should be designed so that one of the differential transistors is turned off. This reduces the noise contribution by a factor of 1.4 since only one transistor is producing noise. Current sources and mirrors cannot be used for biasing loads because active elements will contribute more noise.

Implementing these observations, the first gain stage of the 542 is pictured with the complete schematic by Figure 8-38.

Although the differential input configuration degrades the noise performance slightly, using differential inputs has the advan-
tages of higher input impedance, allowing smaller capacitors and larger resistors to be used to achieve the RIAA and NAB curves.

The second stage is a common-emitter amplifier (Q5) with a current source load (Q6). The Darlington emitter-follower Q3Q4 provides level shifting and current gain to the common-emitter stage (Q5) and the output current sink (Q7). The voltage gain of the second stage is approximately 2000 making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15 MHz . The compensation is adequate to preserve stability to a closed loop gain of 10 .

## BIASING

The non-inverting input has been internally biased from a 1.4 Volt internal voltage source. Following the zero differential rule of amplifiers, the output voltage will be set by the resistor feedback network (R4 and R5) of Figure 8-39.
The base of Q2 requires $0.5 \mu \mathrm{~A}$ bias current. Hence R5 should pass $5 \mu \mathrm{~A}$ minimum for stability, for an output dc voltage of $\frac{V_{C C}}{2}$ the values of R4 and R5 are:
(Equation 8-19)
$R 5=\frac{2 V_{B E}}{10 I_{B}}=240 \mathrm{KMax}$.
(Equation 8-20)
$R 4=\left(\frac{V_{C C}}{2.8-1}\right)_{R 5}$


Figure 8-38

DC amplifier gain is defined by the ratio of R4 and R5. Open loop ac gain can be regained by adding a shunt capacitor across R5. The low frequency 3 dB corner is then defined by the capacitor-resistor break point.

## LM381/382 Device <br> Description

To achieve low noise performance, special consideration must be taken in the design of the input stage. First, the input should be capable of being operated single ended; since both transistors contribute noise in a differential stage degrading input noise by the factor $\sqrt{2}$.

Secondly, both the load and biasing elements must be resistive; since active components would each contribute as much noise at the input device.
The basic input stage, Figure $8-40$, can operate as a differential or single ended amplifier. For optimum noise performance Q2 is turned OFF and feedback is brought to the emitter Q1.

In applications where noise is less critical, Q1 and Q2 can be used in the differential configuration. This has the advantage of higher impedance at the feedback summing point, allowing the use of larger resistors and smaller capacitors in the one control and equalization networks.

The schematic diagram of Figure 8-40 is divided into the first and second voltage gain stages, the current gain stage, and the bias regulator.

The second stage is a common-emitter amplifier (Q5) with a current source load (Q6). The Darlington emitter-follower Q3Q4 provides level shifting and current gain to the common-emitter stage (Q5) and the output current sink (Q7). The voltage gain of the second stage is approximately 2000. making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15 MHz . The compensation is adequate to preserve stability to a closed loop gain of 10. Compensation for unity gain closure may be provided with the addition of an external capacitor in parallel with C1.

Three basic compensation schemes are possible for this amplifier; first stage pole, second stage pole and pole-splitting. First stage compensation will cause an increase in high frequency noise because the first stage gain is reduced, allowing the second stage to contribute noise. Second stage


Figure 8-39


All resistor values are in ohms
Figure 8-40
compensation causes poor slew rate (power bandwidth) because the capacitor must swing the full output voltage. Pole-splitting overcomes both these deficiencies and has the advantage that a small monolithic compensation capacitor can be used.

The output stage is a Darlington emitterfollower (Q8, Q9) with an active current sink (Q7). Transistor Q10 provides short-circuit
protection by limiting the output to 12 mA .

## Biasing

Figure 8-41 shows an ac equivalent circuit of the LM381. The non-inverting input, Q1, is referenced to a voltage source two $\mathrm{V}_{\mathrm{BE}}$ above ground. The output quiescent point is established by negative dc feedback


Figure 8-41

## SINGLE ENDED INPUT BIASING



Figure 8-42
through external divider R4/R5 (Figure 839).

For bias stability, the current through R5 is made ten times the input current of Q2 $(\approx 0.5 \mu \mathrm{~A})$. Then, for the differential input, resistors R5 and R4 are:
(Equation 8-21)

$$
\begin{aligned}
& \mathrm{R} 5=\frac{2 \mathrm{~V}_{\mathrm{BE}}}{10 \mathrm{I}_{\mathrm{Q} 2}}=\frac{1.2}{5 \times 106}=240 \mathrm{k} \Omega \mathrm{MAX} . \\
& \mathrm{R} 4=\left(\frac{\mathrm{V}_{\mathrm{CC}}-1}{2.4}\right) \mathrm{R} 5
\end{aligned} \quad \text { (Equation 8-22) }
$$

When using the single ended input, Q2 is turned OFF and dc feedback is brought to the emitter of Q1 (Figure 8-41). The impedance of the feedback summing point is now two orders of the magnitude lower than the base of Q2 ( $\approx 10 \mathrm{k} \Omega$ ).
Therefore, to preserve bias stability, the impedance of the feedback network must be decreased. In keeping with reasonable resistance values, the impedance of the feedback voltage source can be $1 / 5$ the summing point impedance.
The feedback current is less than $100 \mu \mathrm{~A}$ worst case. Therefore, for single ended input, resistors R5 and R4 are:
(Equation 8-23)

$$
R 5=\frac{V_{B E}}{5 \mathrm{IFB}}=\frac{0.6}{5 \times 10^{4}}=1200 \Omega \mathrm{MAX} .
$$

(Equation 8-24)

$$
\mathrm{R} 4=\left(\frac{\mathrm{V}_{\mathrm{CC}}-1}{1.2}\right) \mathrm{R5}
$$

The circuits of Figures 8-39 and 8-42 have an ac and dc gain equal to the ratio R4/R5. To open the ac gain, capacitor C 2 is used to shunt R5 (Figure 8-43). The ac gain now approaches open loop. The low frequency 3 dB corner, $\mathrm{f}_{\mathrm{o}}$, is given by:
(Equation 8-25) $\mathrm{f}_{0}=\frac{\mathrm{A}_{0}}{2 \pi \mathrm{C} 2 \mathrm{R} 4}$ where: $\mathrm{A}_{0}$ open loop gain

## LM381 OPEN LOOP CONFIGURATION



Figure 8-43

## NAB Tape Preamplifier

Design of a preamplifier begins by determining the gain and output signal amplitudes in reference to the standard $800 \mu \mathrm{~V}$ input signal level. For the following design example, we will use the 542 to achieve a 100 mV output level at 1 kHz following the 7 $1 / 2 \mathrm{lps}$ NAB equalization curve. The graph of Figure 8-37 has been calibrated both in absolute gain for this example and relative gain for general use.
From the given parameters, the closed loop gain becomes 32 dB at the highest frequency of interest. The NAB response is achieved by adding frequency selective ac feedback as depicted by Figure 8-44. Resistors R4 and R5 select the dc gain as defined by Equations 8-19 and 8-20. Placing a value of 200 K upon R5, Equation $8-20$ yields a value of 680 K ohms.

NAB RESPONSE AMPLIFIER


All resistor values are in ohms
Figure 8-44
The lower corner frequency is determined next by the reactance of C4 and R4 such that:
(Equation 8-26)

$$
f_{1}=\frac{.159}{C 4 R 4}
$$

Solving for C 4 yields a value of $.0047 \mu \mathrm{fd}$.
The upper corner frequency, $f_{2}$, is similarly fixed by the reactance of C4 and R7.
(Equation 8-27)

$$
f_{2}=\frac{.159}{C 4 R 7}
$$

Then solving Equation 8-27 for R7 defines a value of 11 k ohms.
Midband gain is now fixed by the relationship.
(Equation 8-28)

$$
A=\frac{R 6+R 7}{R 6}
$$

Solving for the 1 kHz gain of 42 dB using 11 k for R7 yields a value of 88 ohms for R6. The final calculation of the low frequency cut off of the preamp determines the size of C 2 .
(Equation 8-29)

$$
\mathrm{C} 2=\frac{.159}{\text { fCuTOFF R6 }}
$$

## Typical Applications

In addition to the previous detailed design examples, the following general amplifier configurations (see Figures 8-45 through 855) are presented. The choise of design and the device used is a function of the desired complicity and overall performance.


Figure 8-45


Figure 8-46


All resistor values are in ohms
Figure 8-47


|  | C2 | CF | RF | R1 |
| :---: | :---: | :---: | :---: | :---: |
| $7-1 / 21 \mathrm{PS}$ | 750 pF | .033 | 1.5 K | $22 \Omega 1$ |
| $3-3 / 4 \mathrm{IPS}$ | 750 pF | .047 | 2.4 K | $33 \Omega 2$ |

Figure 8-49


All resistor values in ohms
Figure 8-50


## CASSETTE PREAMPLIFIER SINGLE CHANNEL


*600s resistor used as a
terminator when using a
voltage generator instead of the magnetic head.

Figure 8-52

CASSETTE PREAMPLIFIER USING LM382 and NE532

NOTE

1. $10 \mathrm{k} / / .0033 \mathrm{CKT} \mathrm{A}$
2. $10 \mathrm{k} / / 39 \mathrm{k}+.0083$ CKTB
3. NE532 used as unity gain inverting amplifier for correlation only.


| FREQ | GAIN(dB) <br> CKT A | $\phi$ (deg) <br> CKT A | GAIN(dB) <br> CKT B | $\phi$ (deg) <br> CKT B |
| :---: | :---: | :---: | :---: | :---: |
| 20 Hz | +68 | -15 | +68 |  |
| 40 Hz | +76.1 | -76 | +76 | -77 |
| 80 Hz | +79.4 | -135 | +79.3 | -134 |
| 100 Hz | +79.8 | -147 | +79.7 | -148 |
| 200 Hz | +79.7 | -187 | +79.5 | +177 |
| 400 Hz | +77.6 | +157 | +76.9 | +155 |
| 800 Hz | +74.6 | +144 | +73.3 | +149 |
| 1 kHz | +73.9 | +144 | +72.4 | +150 |
| 2 kHz | +71.8 | +134 | +70.6 | +152 |
| 4 kHz | +69.2 | +110 | +69.4 | +145 |
| 8 kHz | +63.9 | +76 | +67.4 | +132 |
| 10 kHz | +61.5 | +65 | +66.5 | +126 |
| 20 kHz | +54 | -4.0 | +62.2 | +107 |



Figure 8-53
frequency in cycles per second


Figure 8-55

## CONSTANT FLUX RESPONSE

Equalization criteria discussed earlier has made reference to RIAA Equalization for plastic discs (records) and for NAB Equalization for magnetic tapes. The NAB characterization should be carried further to discuss the Constant Flux Response.

The earlier discussion encompassed the voltage gain (in dB) vs frequency response of NAB amplifiers. In this section we will deal with the Constant Flux Response.

The Constant Flux Response accounts for the frequency characteristics of the record/ playback heads of the tape (or cassette) machine employed and the effects of tape speed on Standard NAB Constant Flux Response.

Figure 8-56 indicates the circuitry for using two (2) IC's for a NAB response amplifier Specific care should be taken to terminate the input only when using a voltmeter. When using the magnetic head, the terminating resistor should be removed.


| Frequency | Response | Frequency | Response |
| :---: | :---: | :---: | :---: |
| 20 Hz | -8.6 dB | 1.5 kHz | +0.9 dB |
| 25 | 7.0 | 2 | 1.45 |
| 30 | 5.8 | 2.5 | 2.1 |
| 40 | 4.1 | 3 | 2.75 |
| 50 | 3.0 | 4 | 4.1 |
| 60 | 2.3 | 5 | 5.4 |
| 70 | 1.8 | 6 | 6.6 |
| 75 | 1.6 | 7 | 7.7 |
| 80 | 1.4 | 7.5 | 8.2 |
| 90 | 1.2 | 8 | 8.6 |
| 100 | 1.0 | 9 | 9.5 |
| 150 | 0.45 | 10 | 10.35 |
| 200 | 0.2 | 11 | 11.1 |
| 250 | 0.1 | 12 | 11.8 |
| 300 | -0.1 | 13 | 12.5 |
| 400 | $\pm 0$ | 14 | 13.1 |
| 500 | +0.1 | 15 | 13.6 |
| 600 | 0.1 | 16 | 14.2 |
| 700 | 0.2 | 17 | 14.7 |
| 750 | 0.2 | 18 | 15.2 |
| 800 | 0.2 | 19 | 15.6 |
| 900 | 0.3 | 20 | +16.1 |
| 1 kHz | +0.4 dB |  |  |

## NOTES

Reproducer amplifier output for a constant flux in the core of an ideal reproducing head. NAB Standard reproducing characteristics for $17 / 8$ and $33 / 4$ ips tape speeds.

| Frequency | Response | Frequency | Response |
| :---: | :---: | :---: | :---: |
| 20 Hz | -8.8 dB | 1.5 kHz | +2.2 dB |
| 25 | 7.2 | 2 | 3.4 |
| 30 | 5.9 | 2.5 | 4.6 |
| 40 | 4.2 | 3 | 5.7 |
| 50 | 3.2 | 4 | 7.7 |
| 60 | 2.4 | 5 | 9.4 |
| 70 | 1.9 | 6 | 10.8 |
| 75 | 1.7 | 7 | 12.1 |
| 80 | 1.6 | 7.5 | 12.6 |
| 90 | 1.3 | 8 | 13.2 |
| 100 | 1.1 | 9 | 14.15 |
| 150 | 0.6 | 10 | 15.0 |
| 200 | 0.4 | 11 | 15.8 |
| 250 | 0.2 | 12 | 16.6 |
| 300 | 0.15 | 13 | 17.2 |
| 400 | $\pm 0$ | 14 | 17.9 |
| 500 | +0.1 | 15 | 18.5 |
| 600 | 0.3 | 16 | 19.0 |
| 700 | 0.5 | 17 | 19.6 |
| 750 | 0.55 | 18 | 20.0 |
| 800 | 0.6 | 19 | 20.5 |
| 900 | 0.8 | 20 | +21.0 |
| 1 kHz | +1.0 dB |  |  |

NOTES
Reproducer amplifier output for a constant flux in the core of an ideal reproducing head.
NAB Standard reproducing characteristic for $71 / 2$ and 15 -ips tape speeds

## NAB Standards

According to the NAB Standard, an ideal magnetic reproducing system consists of an ideal reproducing head, lossless magnetic ring, head gaps are short and straight, long wave length flux paths so controlled that no low frequency contours are present and head material losses are negligible. The system employs a reproducing amplifier whose voltage conforms to the frequency response of Fig. 8-55 with a constant flux vs frequency in the head core. Because of several reasons, the flux in the core of an ideal head is not necessarily the same as the surface flux on the tape. Since most of the above effects are not easily measured, the NAB Standard is based on an ideal headcore flux, rather than surface induction.

The voltage vs frequency curve is to be uniform with frequency except where modified by the equalization time constants T1 \& T2. The curve expressed in decibels is:
(Equation 8-30)
$N_{d B}=20 \log 10 W T 1^{*} \sqrt{\frac{1+(W T 2)^{2}}{1+(W T 1)^{2}}}$
where $W=2 \pi f$, with $f$ in Hz .
T1 \& T2 are time constants given below:

| Tape Speed | T1 | T2 |
| :---: | :---: | :---: |
| $15 \mathrm{ips}^{\star \star}$ | $3180 \mu \mathrm{sec}$ | $50-\mu \mathrm{sec}$ |
| 7.5 ips | $3180 \mu \mathrm{sec}$ | $50-\mu \mathrm{sec}$ |
| 3.75 ips | $3180 \mu \mathrm{sec}$ | $90-\mu \mathrm{sec}$ |
| 1.875 ips | $3180 \mu \mathrm{sec}$ | $90-\mu \mathrm{sec}$ |

Head Gap Losses:
The approximate head-gap losses vs frequency may be calculated using the expression:
(Equation 8-31)
Gap loss $=-20 \log 10 \frac{\operatorname{Sin}\left(180^{\circ} d / \lambda\right)}{\pi d / \lambda}$
where,
$d=$ the null wavelength,
$\lambda=$ the wavelength of the frequency at which the gap is calculated.

Null wavelength is determined by finding the recorded wavelength at which the reproducing-head output voltage reaches a distinct minimum of at least 20 dB below maximum output. This measurement may be made using speeds of one-half and onequarter the normal speed, using a tunedvoltmeter with no greater than one-third octave bandwidth. To reach a $20-\mathrm{dB}$ null, the head gap edges must be sharp, straight, and parallel.

## NOTES

*WT is

$$
\begin{aligned}
& \omega=\text { Omega } \\
& \tau=\text { Tau }
\end{aligned}
$$

* ips = inches per second


NOTE
Refer to schematic of Figure 13

## CASSETTE PREAMP LM382 \& LM387 (NAB) CONSTANT FLUX RESPONSE



NOTE
Refer to schematic of
Figure 14 \& 15

TAPE PREAMP LM387
CONSTANT FLUX RESPONSE


Figure 8-58


Figure 8-60

| FILTER BANDWIDTH |  |  | 1Vrms |  | 2 Vrms |  | THD + NOISE <br> No Pre-filter |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{aligned} & \text { Left } \\ & \% \end{aligned}$ |  |  |  |  |
| ${ }^{\text {f }} \mathrm{Hz}$ ) |  | $\mathrm{fH}_{(\mathrm{Hz})}$ |  | Right $\%$ | $\begin{aligned} & \text { Left } \\ & \% \end{aligned}$ | $\begin{gathered} \text { Right } \\ \% \end{gathered}$ |  |
|  |  |  |  |  |  |  | Signal 1 Vrms |
| 500 | 400 | 2500 | . 28 | . 28 | . 29 | . 27 | 2.5\% |
| 1k | 900 | 4k | . 28 | . 26 | . 32 | . 28 | 2.5\% |
| 10k | 9900 | 40k | 1.3 | 1.4 | . 68 | . 7 | 2.4\% |

Test Conditions: $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$
ST1700A THD Analyser oscillator signal coupled to reproduce head through constant flux loop. Output signal fed back to ST1700 through Kronhite 3203 filter.

Table 8-4 CASSETTE PREAMP 'THD'
MEASUREMENTS WITH REPRO HEAD
MEASUREMENTS WITH REPRO HEAD

| Freq <br> (Hz) | Output |  |  |
| :---: | :---: | :---: | :---: |
|  | Left <br> dBM | Right <br> dBM |  |
| 20 |  | -35 |  |
| 40 | -27.5 | -26 |  |
| 80 | -18 | -18 |  |
| 100 | -16 | -16 |  |
| 200 | -12 | -12 |  |
| 400 | -10 | -10.5 | "0" dB reference level |
| 800 | -8 | -8 | $@-10 \mathrm{dBm}$ |
| 1 k | -7 | -7 |  |
| 2 k | -2.5 | -2.2 |  |
| 4 k | +2 | +3.2 | +9 |
| 8 k | +8 | +10.8 |  |
| 10 k | +9.5 | +11.8 |  |
| 12 k | +11.2 | +12.3 |  |
| 14 k | +12 | +12.5 |  |
| 16 k | +12.6 | +13 |  |
| 20 k | +13 |  |  |

Test Conditions:
HP651A Test Oscillator 6000hm output coupled through constant flux loop to reproduce head. Output recorded from preamp across 10k load ac. V.M.

Table 8-5 CASSETTE PREAMP CONSTANT FLUX RESPONSE

| Freq. $\mathbf{H z}$ | $\mathbf{1 2 5} \mu$ Vrms <br> (-76dBm) <br> input |  | $245 \mu$ Vrms <br> $(-70 d B m)$ <br> input |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Left <br> $\%$ | Right <br> $\%$ | Left <br> $\%$ | Right <br> $\%$ |
| 100 | .37 | .5 | .47 | .7 |
| 500 | .35 | .35 | .19 | .23 |
| 1 k | .42 | .43 | .22 | .23 |
| 5 k | .54 | .54 | .26 | .28 |
| 10 k | .73 | .75 | .37 | .38 |
| Figure 8-63 |  |  |  |  |

Test Conditions:
Preamp input terminated in $600 \Omega$. Signal fed from ST1700A Analyser to input.
THD measured at output across $10 \mathrm{k} \Omega$ load.
Table 8-6 'THD' MEASUREMENT

## INTEGRATED CIRCUITS FOR CITIZENS BAND TRANSCEIVERS Introduction

Recent advancements in integrated circuits have made it possible to greatly simplify the design of citizens band transceivers. A complete multi-channel radio can be built using integrated circuits for all the required functions with the exception of the RF power output stage. A simplified block diagram of such a transceiver is shown in Figure 8-64.

This applications report will further describe a typical version of such a transceiver using several newly developed integrated circuits.

The growing popularity of CB radio is making it necessary to improve the performance characteristics of the CB receiver. The crowded channel and noise problems inherent in this type of communication system demand high performance system design. A dual conversion receiver is desirable to aid in meeting this goal.

## RF AMPLIFIER/1ST MIXER

The RF amplifier and 1st mixer used in this radio are implemented using an SD6000. The SD6000 is a dual enhancement mode MOSFET integrated RF amplifier/mixer intended for use up to 150 MHz . The advantages of using MOSFETs in receiver "front end" designs have been realized for several years by manufacturers of FM and television tuners. Using a linear device such as a MOSFET, it is possible to achieve improvements in cross-modulation, intermodulation distortion and in general a much wider dynamic range than possible using conventional bipolar transistors.


The SD6000 is ideally suited for this application for several reasons. The RF section is essentially a low noise, high gain dual gate MOSFET. The relatively high input impedance of this device makes it convenient to use high $Q$ tuned circuits which reduce the possibility of out of band spurious responses. The AGC range of the RF amplifier is greater than 50 dB at 27 MHz and because of the low parasitic capacitances associated with this device there is no skewing of the center frequency of the tuned circuits as a function of AGC voltages. The RF amplifier input circuit can be roughly approximated as shown below in Figure 8-65.
L1 consists of 24 turns of \#32 wire tapped 4 turns from the ground side on a MicroMetals T44-10 core. This gives an inductance of $1.6 \mu \mathrm{~h}\left(\mathrm{X}_{\mathrm{C}}=270 \Omega @ 27 \mathrm{MHz}\right)$ and an unloaded Q of 150 .
The input circuit can be further simplified as shown in Figure 8-66.


Figure 8-66

$C_{P}$ is made up of the D-MOS input, and a fixed parallel capacitor. The required $C_{P}$ is given by

$$
C_{P}=\frac{1}{W^{2} L}
$$

Cp at 27 MHz is therefore equal to 22 pf. A portion of $\mathrm{C}_{p}$ is made tunable in this design. This would not be necessary in a design using a slug tuned inductor. It should be noted that the position of the tap is such that the reflected antenna impedance does not match the RF amplifier input impedance. This was done intentionally to improve the large signal ( 2 Vrms ) handling capability of this receiver. The MOS front end has sufficient gain to compensate for this loss.

The bandwidth of the RF input circuit can be found knowing the total parallel resistance ( $\mathrm{R}_{\mathrm{p}}$ ) and parallel capacitance

$$
\mathrm{BW}_{-3 \mathrm{~dB}}=\frac{1}{2 \pi \mathrm{RC}}
$$

At 27 MHz the RF input bandwidth is approximately 4 MHz . In a more optimum design this could be made narrower by tapping the input coil closer to ground.
The design of the RF output circuit is very similar to that of the input. The only difference is a different value of fixed capacitance to take into account the RF amplifier output and mixer input capacitance.

Dual gate Signetics D-MOS transistors are exceptionally stable RF devices because of their low feedback capacitance (typically .02pf). This makes it possible to achieve high gain without the need for neutralization. Low feedback is also the reason for a wide dynamic AGC range.

The second dual gate MOSFET is the SD6000 which is designed for mixer applications. It is a relatively large geometry device with a wide square law region. This design overcomes the bias problems inherent in most MOSFETs when used as mixers. In other MOSFETs biasing in the square law region is only possible over a narrow range of drain current. In the SD6000 mixer the conversion gain is essentially constant from 5 to 10 mA drain current thus simplifying the bias circuit design.

The 1st oscillator is injected into gate 2 and the RF signal into gate 1. Injecting the oscillator into gate 2 provides the highest isolation between the oscillator and RF input. This isolation is important to prevent radiation of the oscillator signal through the receiver antenna.

The mixer is biased to operate in the most linear portion of the forward transconductance curves. Figures 8-67 and 8-68 show the transconductance curves for the SD6000 are linear in a relatively wide operating region. Non-linearities in these curves indicate that third order (and higher) terms would be present if the device was biased in these regions. These higher order terms contribute only to undesired responses. As the transconductance curves become linear, the higher order terms disappear and conversion gain increases. Figure 8-67 shows that the gate 1 transconductance curves is almost a straight line for gate 2 bias voltage between 2.0 and 6.0 volts. Figure 868 shows a linear region for gate 2 transconductance with gate 1 bias from 2.5 to 3.5 volts.



By definition the transconductance, gm is the partial derivative of drain current, $i_{d}$, with respect to the input voltage $\mathrm{e}_{\mathrm{s}}$. The total drain current of the mixer can be expressed by

$$
i_{d}=g m 1 V_{g 1}+g m 2 V_{g 2}
$$

where $\mathrm{gm} 1=$ transconductance gate 1 to drain. gm2 $=$ tranconductance gate 2 to drain.

From Figure 8-67 the gate 1 tranconductance, gm1 can be expressed as:

$$
\begin{aligned}
& \mathrm{gm} 1=-17.6+8.2\left(\mathrm{~V}_{\mathrm{g} 2}+\mathrm{V}_{\mathrm{g} 2}\right) \text { (mmhos) } \\
& \text { for } \mathrm{V}_{\mathrm{g} 2}=2 \mathrm{~V} \text { to } 6 \mathrm{~V}
\end{aligned}
$$

From Figure 8-68 we get the following expression for gm2

$$
\begin{aligned}
& \mathrm{gm} 2=-23.7+10.2\left(\mathrm{~V}_{\mathrm{g} 1}+\mathrm{V}_{\mathrm{g} 1}\right) \text { (mmhos) } \\
& \text { for } \mathrm{V}_{\mathrm{g} 1}=2.5 \mathrm{~V} \text { to } 3.5 \mathrm{~V}
\end{aligned}
$$

If the dc bias points are chosen, for example $V_{g 1}=3.5$ and $V_{g 2}=3.5$, the following expressions are derived from gm1 and gm2 using the previous equations

$$
\begin{aligned}
& \mathrm{gm} 1=11.1+8.2 \mathrm{~V}_{\mathrm{g} 2} \text { (mmhos) } \\
& \mathrm{gm} 2=8.9+10.2 \mathrm{~V}_{\mathrm{g} 1} \text { (mmhos) }
\end{aligned}
$$

Substituting these equations into the expression for the total drain current, $i_{d}$, we get

$$
\mathrm{i}_{\mathrm{d}}=11.1 \mathrm{~V}_{\mathrm{g} 1}+8.9 \mathrm{~V}_{\mathrm{g} 2}+18.4 \mathrm{~V}_{\mathrm{g} 1} \mathrm{~V}_{\mathrm{g} 2}
$$

The last term in this equation is the one that will contain the IF frequency we desire. If we let $V_{g 1}$ and $V_{g 2}$ equal a sinusoidal voltage, $V_{g 1}$ is the input signal voltage and $V_{g 2}$ is the local oscillator, we obtain

$$
\begin{aligned}
& V_{\mathrm{g} 1}=E_{\mathrm{s}} \sin \omega \mathrm{LO}+\omega_{\mathrm{s}} \mathrm{t} \\
& \mathrm{~V}_{\mathrm{g} 2}=\mathrm{E}_{\mathrm{LO}} \sin \omega \mathrm{Lot}
\end{aligned}
$$

Substituting $V_{g 1}$ and $V_{g 2}$ into the equation for $\mathrm{i}_{\mathrm{d}}$ gives

$$
\begin{aligned}
i_{d}= & 18.4 E_{S} E_{L O} 1 / 2 \cos \left(\omega L O+\omega_{S}\right) t+1 / 2 \cos \\
& \left(\omega L O-\omega_{S}\right) t
\end{aligned}
$$

The ( $\omega$ LO $-\omega_{S}$ ) term is the 10.7 MHz IF we
want. Dividing both sides of the equation by $\mathrm{E}_{\mathrm{s}}$ we obtain

$$
\begin{aligned}
\frac{i_{d}}{E_{s}} & =g m_{\mathrm{c}}=9.2 \mathrm{E}_{\mathrm{LO}}(\text { peak }) \\
& =13 \mathrm{ELO}_{\mathrm{LO}}(\mathrm{rms}) \mathrm{mmhos}
\end{aligned}
$$

This exercise shows that relatively high conversion gains can be achieved using the SD6000. It can be seen that the conversion transconductance will also be a function of the local oscillator level.

In actual practice, good performance can be achieved with both gates biased at the same dc voltage. The bias voltage is chosen to give a drain current of 5 to 10 mA .

For bias stability, some form of dc feedback should be incorporated to reduce the drain current variations that would occur in production where variations in the device threshold voltages will be encountered. In the SD6000, the mixer and RF amplifier substrates and RF amplifier source are connected internally so precautions must be taken to assure that the RF amplifier source voltage is less than or equal to the mixer source voltage. In this design the RF amplifier source is grounded so it can never be positive with respect to the mixer source. Figure 8-69 shows a simplified bias circuit of the RF amplifier.


This bias circuit provides dc feedback without using a source resistor. R3 is made large enough so that there is a significant voltage drop across it with normal operating drain current $(10-15 \mathrm{~mA})$. This voltage drop means a lower drain to source voltage (VDS). A lower $V_{D S}$ does not affect the RF amplifier gain since the transconductance is constant with VDS from 5 to 20 volts. If variations in threshold voltage were to cause a higher drain current, the voltage drop across R3 would increase thereby decreasing the gate 1 voltage derived from R1 and R2. This decreased gate 1 voltage tends to decrease
the drain current and will result in a stable operating point.
The mixer is biased using the same technique with the addition of a bypassed source resistor to provide even greater stability.

The mixer output is coupled through a 10.7 MHz IF transformer to a 10.7 MHz crystal filter. The output of the filter is terminated with a 2.2 k resistor in parallel with the TCA440 input ( $2 \mathrm{~K} / 5 \mathrm{pf}$ ).

## 1st IF/2nd Mixer/2n IF

A block diagram of the TCA440 is shown in Figure 8-70.

This integrated circuit is intended for AM receivers up to 50 MHz . It has several features making it well suited for citizens band receiver applications. The RF stage (in this case the 1st IF) is a differential amplifier with an AGC control range of approximately 38 dB . Its output is internally coupled to a mulitplicative push-pull mixer (balanced). This mixer produces few harmonics and provides suppression of the RF and oscillator frequencies. The internal oscillator frequency is fixed at 10.245 MHz by a parallel resonant crystal. This gives a mixer output frequency of 455 kHz for the 2 nd IF.

The mixer output is filtered by a single tuned IF transformer, ceramic filter, and a second single tuned transformer and applied to the 4 stage 2nd IF amplifier in the TCA440. This 2nd IF has an AGC control range of 62 dB . The two independent AGC control loops in the TCA440 provide a very wide operating dynamic range ( 100 dB ). Although a 455 kHz 2nd IF frequency is used in this design, the TCA440 IF stages will operate from 0 to 2 MHz .

## Audio Processing

The circuit shown in Figure 8-71 shows how the NE571 may be used as a dc volume control. The frequency response of the circuit is approximately 300 Hz to 3 kHz and the dynamic control range is greater than 60 dB . Figure $8-72$ shows the dc control voltage vs gain.

The output of the NE571 dc volume control drives a TBA810S audio power amplifier. The TBA 810 provides a 6 watt (@14.4V 4 ) output with low harmonic and cross-over distortion. In addition, the circuit has a thermal limiting circuit which simplifies the heat sink design.

## Frequency Synthesizer

The purpose of the frequency synthesizer is to provide the necessary signals to drive the receiver's first mixer, second mixer, and transmitter power amplifier. In a 40 channel,


Figure 8-70


Figure 8-71
dual conversion CB transceiver, it is necessary to generate 81 discrete frequencies. By using phase locked loop frequency synthesis, this can be accomplished using only one crystal.
The SM5104/5/7/9 is a "first generation" CMOS integrated circuit synthesizer. A block diagram of the SM5104 is shown in Figure 873.

This circuit operates from a single power supply using low power CMOS technology. It contains a reference oscillator, a 28 or 29 divider chain, a binary input programmable divider, and phase detector circuits.

There are several ways this circuit can be used in the transceivers. The methods described here will be limited to dual conversion systems using 10.695 MHz 1st IF and 455 kHz 2nd IF. These frequencies were


Figure 8-72
chosen because low cost filters are readily available. A simplified block diagram of a CB transceiver is shown in Figure 8-74.
The basic frequency synthesizer using a PLL is shown in Figure 8-74.
In this circuit, the output frequency is an integer multiple of the reference frequency. ( $f_{\text {out }}=N f_{\text {reff }}$ ). This is the simplest form the loop can assume but in most cases, not the most practical. The major problem with this type of PLL is that the programmable counters must operate at the output frequency (in the CB case, up to 27 MHz ). There are several commonly used methods to lower the frequency into the programmable counter.

Frequency synthesis by prescaling is shown in Figure 8-76.
In this system, the frequency into the programmable counter is lowered by a factor of $P$. The disadvantage of this system is that the reference frequency must also be prescaled by the factor $P$. This lowers the "effective" reference frequency and slows the loop response.

Frequency synthesis by 2 modulus prescaling solves the problem of high programmable divider frequency and slow loop response but requires more complex logic in addition to a high frequency 2 modulus divider. The cost of this system is slightly greater than that of Figure 8-76 but the performance is equal to that of Figure 8-75. A block diagram of this system is shown in Figure 8-77.

The most common synthesizer configuration used in CB transceivers is prescaling by mixing down. This method is shown below in Figure 8-78.
This system offers the optimum performance but requires a second stable frequency source for mixing down. This system can be easily implemented using the SM5104. The system block diagram is shown in Figure 8-79.
This is a practical circuit configuration but has several minor disadvantages. The major problems are that it requires four external active tuned circuits, the x3 multiplier, offset mixer, transmit offset oscillator and mixer. It also requires the use of 2 crystals. Despite these drawbacks, this general configuration is widely used in currently available CB transceivers.

With the introduction of "second generation" synthesizers such as the NE575, many of the previously described shortcomings are resolved. The NE575 will generate the required frequencies for a dual or single conversion CB transceiver using only one crystal. Figure 8-80 shows the functional block diagram of the NE575.


Figure 8-73


Figure 8-74

PLL FREQUENCY SYNTHESIZER


## SYNTHESIS BY 2 MODULUS PRESCALING



Figure 8-77

## SYNTHESIS BY MIXING DOWN



Figure 8-78


Figure 8-79

## Audio Compressor

The purpose of the transmit audio compressor is to amplify the signal from the microphone to the level required to drive the modulator. It also provides an automatic level control (ALC) circuit. The ALC circuit has a transfer function which makes its output voltage constant with a wide range of input levels. It is generally desirable to have an audio compressor which provides an output level which drives the modulator to close to $100 \%$ modulation with very low input levels and does not exceed $100 \%$ with large inputs.
There are two major overmodulation problems that show up in many CB transceivers currently available. One is the audio compressor's ability to handle a wide dynamic range of microphone input levels. The current popularity of "power mics" makes it necessary for the compressor to limit the modulation index to less than 100\% with very large inputs. The second overmodulation problem that may arise relates to the audio compressor's attach time. Active compressor circuits take a finite time to respond to a sudden change in input level.

The NE571 provides an economical solution to the above mentioned problems. Figure 881 shows how this ALC circuit may be implemented.

The gain of this circuit is

$$
\begin{aligned}
& K=\frac{R 1 R 2 I_{B}}{2 R 3 V_{I N}(A V G)} \text { where } I 3=140 \mu \mathrm{~A} \\
& \text { and } \frac{V_{I N}}{V_{\text {IN }}(A V G)}=\frac{\pi}{2 \sqrt{2}} \\
& \text { for sinc waves }
\end{aligned}
$$

$R_{x}$ is included to limit the maximum gain of the compressor. This is to prevent high modulation levels at very low input levels (such as background noise). The maximum gain

$$
\mathrm{K}_{\max }=\frac{\frac{\mathrm{R} 1+\mathrm{R}_{\mathrm{X}}}{1.8} \times \mathrm{R} 2 \times \mathrm{I}_{\mathrm{B}}}{2 \mathrm{R} 3}
$$

The output voltage may be set to the desired level

$$
V_{\text {out }}=\frac{R 1 R 2 I_{B}}{2 R 3} \frac{V_{\text {IN }}}{V_{\text {IN }}(A V G)}
$$

The other important design equations for this circuit are:

$$
\begin{aligned}
& \text { I ALC time constant }\left(\tau=R 1 \times C_{\text {Rect }}\right) \\
& \text { II Distortion }=\frac{.1 \mu f}{C_{\text {Rect }}} \times \frac{1 \mathrm{KHz}}{\text { freq }} \times 2 \% \\
& \text { III } V_{\text {out }}(\mathrm{dc})=\left[1+\frac{R_{\mathrm{dc} 1}+R_{\mathrm{dc} 2}}{R 4}\right] 1.8 \mathrm{~V}
\end{aligned}
$$



Figure 8-80


## Transmit RF

Development work is currently taking place to try and solve some of the typical problems encountered in the RF section of CB transceivers. The major emphasis is towards reducing the cost of the output circuitry (elimination of the modulation transformer) and reduce spurious outputs.

The transmit oscillator signal, generated by the PLL, will drive a low level FET modulator. The modulator output then drives a linear RF power amplifier. The RF power amplifier will be implemented using a power D-MOS FET. The advantages of a MOSFET power amplifier are high transconductance, no thermal run-away, no second breakdown, and reduction in harmonic output.

Detailed information on this section of the CB transceiver will be made available as soon as the development work is completed.

## CITIZENS' BAND RECEIVER TCA440/SD6000



Figure 8-82



## INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high performance is required, one has to resort to complex discrete circuitry with many expensive, well matched components. This paper describes a new integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion ( $<.1 \%$ ), high signal to noise ratio $(90 \mathrm{~dB}$ ), and wide dynamic range ( 110 dB ).

## CIRCUIT BACKGROUND

The NE570 Compandor was specifically designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal to noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 8-89 graphically shows what a compandor can do for the signal to noise ratio of a restricted dynamic range channel. The input level range of +20 to -80 dB is shown undergoing a 2 to 1 compression where a 2 dB input level change is compressed into a 1 dB output level change by the compressor. The original 100 dB of dynamic range is thus compressed to a 50 dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45 dB .
The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. It is hoped that these features will make the circuit as widely used in audio systems as it will be in telecommunications systems.

## BASIC CIRCUIT HOOKUP AND OPERATION

Figure 8-90 shows the block diagram of one half of the chip (there are two identical
channels on the I.C.). The full wave averaging rectifier provides a gain control current, $I_{\mathrm{G}}$, for the variable gain ( $\Delta \mathrm{G}$ ) cell. The output of the $\Delta G$ cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output dc bias.


The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 volt reference denoted $V_{\text {ref. }}$ The noninverting input of the op amp is tied to $V_{\text {ref, }}$, and the summing nodes of the rectifier and $\Delta G$ cell (located, at the right, of $R_{1}$ and $R_{2}$ ) have the same potential. The THD trim pin is also at the $\mathrm{V}_{\text {ref }}$ potential.

Figure 8-91 shows how the circuit is hooked up to realize an expandor. The input signal, $\mathrm{V}_{\mathrm{in}}$, is applied to the inputs of both the rectifier and the $\Delta G$ cell. When the input signal drops by 6 dB , the gain control current will drop by a factor of 2 , and so the gain will drop 6dB. The output level at $V_{\text {out }}$ will thus drop 12dB, giving us the desired 2 to 1 expansion.
Figure 8-92 shows the hookup for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The $\Delta G$ cell is set up to provide ac feedback only, so a separate dc feedback loop is provided by the two $R_{d c}$ and $C_{d c}$. The values of $R_{d c}$ will determine the dc bias at the output of the op amp. The output will bias to:

$$
V_{\text {out }} d c=1+\frac{R_{d c 1}+R_{d c 2}}{R_{4}} V_{\text {ref }}=\left(1+\frac{R_{d c} t o t}{30 K}\right) 1.8 \mathrm{~V}
$$

The output of the expandor will bias up to: $V_{\text {out }} d c=1+\frac{R_{3}}{R_{4}} V_{\text {ref }}=\left(1+\frac{20 \mathrm{~K}}{30 \mathrm{~K}}\right) 1.8 \mathrm{~V}=3.0 \mathrm{~V}$
The output will bias to 3.0 V when the internal resistors are used. External resistors may be placed in series with $R_{3}$, (which will affect the gain), or in parallel with $R_{4}$ to raise the dc bias to any desired value.



## CIRCUIT DETAILS-RECTIFIER

Figure 8-93 shows the concept behind the full wave averaging rectifier. The input current to the summing node of the op amp, $\mathrm{V}_{\mathrm{in}} / \mathrm{R}_{1}$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by $\mathrm{R}_{5}, \mathrm{Cr}$, which set the averaging time constant, and then mirrored with a gain of 2 to become IG, the gain control current.


Figure 8-93
Figure 8-94 shows the rectifier circuit in more detail. The op amp is a one stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of $Q_{1}$ ), which is shown grounded, is actually tied to the internal $1.8 \mathrm{~V} \mathrm{~V}_{\text {ref. }}$. The inverting input is tied to the op amp output, (the emitters of $Q_{5}$ and $Q_{6}$ ), and the input summing resistor $R_{1}$. The single diode be-

tween the bases of $Q_{5}$ and $Q_{6}$ assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices $Q_{5}$ and $Q_{6} . Q_{6}$ will conduct when the input swings positive and $Q_{5}$ conducts when the input swings negative. The collector currents will be in error by the $\alpha$ of $\mathrm{Q}_{5}$ or $\mathrm{Q}_{6}$ on negative or positive signal swings, respectively. IC's such as this have typical npn $\beta$ 's of 200 and pnp $\beta^{\prime}$ 's of 40 . The $\alpha$ 's of .995 and .975 will produce errors of $.5 \%$ on negative swings and $2.5 \%$ on positive swings. The $1.5 \%$ average of these errors yields a mere -13 dB gain error.
At very low input signal levels the bias current of $Q_{2}$, (typically 50 nA ), will become significant as it must be supplied by $\mathrm{Q}_{5}$. Another low level error can be caused by dc coupling into the rectifier. If an offset voltage exists between the $V_{\text {in }}$ input pin and the base of $Q_{2}$, an error current of $\mathrm{V}_{\text {os }} / R_{1}$ will be generated. A mere 1 mv of offset will cause an input current of 100 nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the $\beta$ of the pnp $Q_{6}$ will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to $250 \mu \mathrm{~A}$. If necessary, an external resistor may be placed in series with $R_{1}$ to limit the current to this value. Figure 8-95 shows the rectifier accuracy vs input level at a frequency of 1 kHz .
At very high frequencies, the response of the rectifier will fall off. The rolloff will be more pronounced at lower input levels due to the increasing amount of gain required to switch between $Q_{5}$ or $Q_{6}$ conducting. The
rectifier frequency response for input levels of $0 \mathrm{dBm},-20 \mathrm{dBm}$, and -40 dBm is shown in Figure 8-96 The response at all three levels is flat to well above the audio range.


## VARIABLE GAIN CELL

Figure 8-97 is a diagram of the variable gain cell. This is a linearized two quadrant transconductance multiplier $1,2 . \mathrm{Q}_{1}, \mathrm{Q}_{2}$ and the op amp provide a predistorted drive signal for the gain control pair, $Q_{3}, Q_{4}$. The gain is controlled by $\mathrm{IG}_{\mathrm{G}}$ and a current mirror provides the output current.
The op amp maintains the base and collector of $Q_{1}$ at ground potential ( $V_{\text {ref }}$ ) by controlling the base of $\mathrm{Q}_{2}$. The input current $\mathrm{l}_{\text {in }}$ $\left(=V_{i n} / R_{2}\right)$ is thus forced to flow through $Q_{1}$ along with the current $I_{1}$, so $I_{c}=I_{1}+I_{\text {in }}$. Since $l_{2}$ has been set at twice the value of $I_{1}$, the current through $Q_{2}$ is $I_{2}-\left(l_{1}+l_{\text {in }}\right)=l_{1}-l_{\text {in }}=$ Ic2. The op amp has thus forced a linear current swing between $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$, by providing the proper drive to the base of $\mathrm{Q}_{2}$. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the nonlinearity of the differential pair $\mathrm{Q}_{1}, \mathrm{Q}_{2}$ under large signal conditions.
The key to the circuit is that this same predistorted drive signal is applied to the gain control pair $Q_{3}$ and $Q_{4}$. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical, regardless of the magnitude of the currents. This gives us:

$$
\frac{I_{1}}{I_{2}}=\frac{I_{C} 4}{I_{C 3}}=\frac{I_{1}+I_{\text {in }}}{I_{1-1} I_{\text {In }}}
$$

plus the relationships $\mathrm{IG}_{\mathrm{G}}=\mathrm{I}_{\mathrm{C}}=\mathrm{I}_{\mathrm{C} 4}$ and $\mathrm{l}_{\text {out }}$ -=IC4-Iс3 will yield the multiplier transfer function,

$$
I_{\text {out }}=\frac{I_{G}}{I_{1}} I_{\text {in }}=\frac{V_{\text {in }}}{R_{2}} \frac{I_{G}}{I_{1}}
$$

this equation is linear and temperature insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in 2nd harmonic distortion. Figure $8-98$ gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8 dBm level. At a nominal operating level of 0 dBm , a 1 mv offset will yield $.34 \%$ of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about $1 / 2 \mathrm{mv}$. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been


IOUT $=\frac{I_{G}}{I_{1}} \quad \mathrm{I}_{\mathrm{N}}=\frac{\mathrm{I}_{\mathrm{G}} V_{\mathrm{IN}_{\mathrm{N}}}}{\mathrm{I}_{2} \mathrm{R}_{2}}$
Figure 8-97
provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 8-99 shows the simple trim network required.


## THD TRIM NETWORK



Figure 8-99

Figure 8-100 shows the noise performance of the $\Delta \mathrm{G}$ cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20 kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20 dB of gain reduction. At high gains, the signal to noise ratio is 90 dB , and the total dynamic range from maximum signal to minimum noise is 110 dB .
Control signal feed-through is generated in the gain cell by imperfect device matching and mismatches in the current sources $I_{1}$ and $I_{2}$. When no input signal is present, changing IG will cause a small output signal. The distortion trim is effective in nulling out any control signal feed-through, but in general, the null for minimum feed-through will be different than the null in distortion. The control signal feed-through can be trimmed independently of distortion by tying a current source to the $\Delta \mathrm{G}$ input pin. This effectively trims $\mathrm{I}_{1}$. Figure 8 -101 shows such a trim network.



## OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1 MHz bandwidth. Figure 8-102 shows the basic circuit. Split collectors are used in the input pair to reduce $\mathrm{g}_{\mathrm{m}}$, so that a small compensation capacitor of just 10pf may be used. The output stage, although capable of output currents in excess of 20 mA ., is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.


## RESISTORS

Inspection of the gain equations in Figure 891 and $8-92$ will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hookups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 8103 shows the effects of the temperature on the diffused resistors which are normally used in integrated circuits, and the ion implanted resistors which are used in this circuit. Over the critical $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ temperature range, there is a 10 to 1 improve-
ment in drift from a 5\% charge for the diffused resistors, to a $.5 \%$ change for the implemented resistors. The implanted resistors have another advantage in that they can be made $1 / 7$ the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.


## APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

## BASIC EXPANDOR

Figure 8-104 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and the $\Delta \mathrm{G}$ cell inputs are tied to $\mathrm{V}_{\text {in }}$ so that the gain is proportional to the average value of $\left(V_{i n}\right)$. Thus, when $V_{\text {in }}$ falls 6 dB , the gain drops 6 dB and the output drops 12 dB . The exact expression for the gain is

$$
\text { Gain exp. }=\frac{2 R_{3} V_{\text {in }} \text { (ave) }}{R_{1} R_{2} I_{B}} ; I_{B}=140 \mu \mathrm{~A}
$$

The maximum input that can be handled by the circuit in Figure 8-104 is a peak of 3 V . The rectifier input current can be as large as $\mathrm{I}=3 \mathrm{~V} / \mathrm{R}_{1}=3 \mathrm{~V} / 10 \mathrm{~K}=300 \mu \mathrm{~A}$. The $\Delta \mathrm{G}$ cell input current should be limited to $1=$ $2.8 \mathrm{~V} / \mathrm{R}_{2}=2.8 \mathrm{~V} / 20 \mathrm{~K}=140 \mu \mathrm{~A}$. If it is necessary to handle larger input voltages than $0 \pm$ 2.8 V pk , external resistors should be placed in series with $R_{1}$ and $R_{2}$ to limit the input current to the above values.
Figure 8-104 shows a pair of input capacitors $\mathrm{C}_{\text {in1 }}$ and $\mathrm{C}_{\text {in2. }}$. It is not necessary to use both capacitors if low level tracking accuracy is not important. If $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ are tied together and share a common capacitor, a small current will flow between the $\Delta \mathrm{G}$ cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.
The output of the expandor is biased up to 3 V by the dc gain provided by $\mathrm{R}_{3}, \mathrm{R}_{4}$. The output will bias up to

$$
V_{\text {out }} d c=\left(1+\frac{R_{3}}{R_{4}}\right) \quad V_{\text {ref }}
$$

For supply voltages higher than $6 \mathrm{~V}, \mathrm{R}_{4}$ can be shunted with an external resistor to bias the output up to $1 / 2 \mathrm{Vcc}$.
Note that it is possible to externally increase $R_{1}, R_{2}$, and $R_{3}$, and to decrease $R_{3}$ and $R_{4}$. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ may be increased; if a larger output is required, $\mathrm{R}_{3}$ may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the $\pm 300 \mu \mathrm{~A}$ peak current restriction).


## BASIC COMPRESSOR

Figure 8-105 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6 dB , the output can rise only 3 dB . The 3dB increase in output level produces a 3 dB increase in the gain in the $\Delta G$ cell, yielding a $6 d B$ increase in feedback current to the summing node. Exact expression for gain is
Gain (comp.) $=\left[\frac{R_{1} R_{2} I_{B}}{2 R_{3} V_{\text {in }} \text { (ave) }}\right]^{1 / 2}$


The same restrictions for the rectifier and $\Delta G$ cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and $\Delta G$ cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no dc feedback path around the op amp through the $\Delta \mathrm{G}$ cell, one must be provided externally. The pair of resistors $R_{d c}$ and the capacitor $\mathrm{C}_{\mathrm{dc}}$ must be provided. The op amp output will bias up to

$$
V_{\text {out }} d c=\left(1+\frac{2 R_{d c}}{R_{4}}\right) V_{\text {ref }}
$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the $\pm 300 \mu \mathrm{~A}$ peak current restriction). If the input signal is small, a large output can be produced by reducing $R_{3}$ with the attendant decrease in input impedance, or by increasing $R_{1}$ or $R_{2}$. It would be best to increase $R_{2}$ rather than $R_{1}$ so that the rectifier input current is not reduced.

## DISTORTION TRIM

Distortion can be produced by voltage offsets in the $\Delta \mathrm{G}$ cell. The distortion is mainly even harmonics, and drops with decreasing
input signal. (Input signal meaning the current into the $\Delta G$ cell.) The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 8-106 is suitable, as would be any other capable of delivering $\pm 30 \mu \mathrm{~A}$ into $100 \Omega$ resistor tied to 1.8 V .

## THD TRIM NETWORK



Figure 8-106

## LOW LEVEL MISTRACKING

The compandor will follow a 2 to 1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of $<100$ na that produces errors at low levels. The magnitude of the error can be estimated. For a full scale rectifier input signal of $\pm 200 \mu \mathrm{~A}$, the average input current will be $127 \mu \mathrm{~A}$. When the input signal level drops to a $1 \mu \mathrm{~A}$ average, the bias current will produce a $10 \%$ or 1 dB error in gain. This will occur at 42 dB below the maximum input level.

It is possible to deviate from the 2 to 1 transfer characteristic at low levels as shown in the circuit of Figure 8-107. Either
$R_{a}$ or $R_{b}$, (but not both), is required. The voltage on $C_{\text {rect }}$ is $2 \times V_{\text {be }}$ plus $V_{\text {in }}$ ave. For low level inputs $V_{\text {in }}$ ave is negligible, so we can assume 1.3 V as the bias on $\mathrm{C}_{\text {rect. If }} \mathrm{R}_{\mathrm{a}}$ is placed from $\mathrm{Crect}^{\text {to }}$ gnd we will bleed off a current $I=1.3 \mathrm{~V} / \mathrm{R}_{\mathrm{a}}$. If the rectifier average input current is less than this value, there will be no gain control input to the $\Delta \mathrm{G}$ cell, so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3 \mathrm{~V} / \mathrm{R}_{\mathrm{a}}$ and the expandor output will become active. For large input signals, $R_{a}$ will have little effect. The result of this is that we will deviate from the 2 to 1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 8-108 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through $R_{a}$ will be a function of temperature because of the two $\mathrm{V}_{\text {be }}$ drops, so the low level tracking will drift with temperature. If a negative supply is available, it would be desirable to tie $R_{a}$ to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the $\mathrm{V}_{\text {be }}$ temperature drift.
$R_{b}$ will supply an extra current to the rectifier equal to ( $\left.\mathrm{V}_{\mathrm{cc}}-1.3 \mathrm{~V}\right) \mathrm{R}_{\mathrm{b}}$. In this case, the expandor transfer characteristic will deviate towards 1 to 1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor this would lead to a lack of compression at low levels. Figure 8-109 shows some typical transfer curves. An $\mathrm{R}_{\mathrm{b}}$ value of approximately 2.5 Meg would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

## EXPANDOR WITH LOW LEVEL MISTRACKING



Figure 8-107


Figure 8-108


Figure 8-109

## RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100 nA . This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the $\Delta G$ cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 8-110 Figure $8-111$ shows the rectifier performance with and without current cancellation.

## ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant 10 KxCrect . Figure $8-112$ shows how the gain will change when the input signal undergoes a 10,20 , or 30 dB change in level.


RECTIFIER PERFORMANCE WITH Ib COMPENSATION


Figure 8-111
The attack time is much faster than the decay, which is desirable in most applications. Figure 8-113 shows the compressor attack envelope for a +12 dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors, defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to $t=.15$ in the figure. The CCITT recommends an attack time of $3 \pm$ 2 ms , which suggests an RC product of 20 ms . Figure $8-114$ shows the compressor output envelope when the input level is suddenly reduced 12 dB . The output, initially at a level of 4 units, drops 12 dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of $13.5 \pm 9 \mathrm{~ms}$. This corresponds to $t=$ .675 in the figure, which gain suggests a 20 ms RC product. Since $\mathrm{R}_{1}=10 \mathrm{~K}$, the CCITT recommendations will be met if $\mathrm{Crect}^{\text {rec }}$ $=2 \mu \mathrm{f}$.

There is a trade off between fast response and low distortion. If a small $\mathrm{C}_{\text {rect }}$ is used to get very fast attack and decay, some ripple
will appear on the gain control line and produce distortion. As a rule, a $1 \mu \mathrm{f}$ Cect will produce $.2 \%$ distortion at 1 kHz . The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where $\mathrm{C}_{\text {rect }}=2 \mu \mathrm{f}$, the ripple would cause $.1 \%$ distortion at 1 kHz and $.33 \%$ at 300 hz . The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of Crect.


COMPRESSOR ATTACK ENVELOPE +12dB STEP


Figure 8-113


## FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure $8-115$ shows a typical circuit which requires $1 / 2$ of an NE570/571, $1 / 2$ of an LM339 quad comparator, and a pnp transistor. For small signals, the $\Delta \mathrm{G}$ cell is nearly off, and the circuit runs at unity gain as set by $\mathrm{R}_{8}, \mathrm{R}_{7}$. When the output signal tries to exceed a + or -1 volt peak, a comparator threshold is exceeded. The pnp is turned on and rapidly charges $\mathrm{C}_{4}$ which activates the $\Delta \mathrm{G}$ cell. Negative feedback through the $\Delta \mathrm{G}$ cell reduces the gain, and the output signal level. The attack time is set by the RC product of $R_{18}$ and $C_{4}$, and the release time is determined by $\mathrm{C}_{4}$ and the internal rectifier resistor, which is 10 K . The circuit shown attacks in less than 1 ms and has a release time constant of 100 ms . R9 trickles about $.7 \mu \mathrm{~A}$ through the rectifier to prevent $\mathrm{C}_{4}$ from becoming completely discharged. The gain cell is activated when the voltage on pin 1 or 16 exceeds two diode drops. If $C_{4}$ were allowed to completely discharge, there would be a slight delay before it recharged to $>1.2 \mathrm{~V}$ and activated limiting action.
A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two pnp transistors. The resistor networks $\mathrm{R}_{12}, \mathrm{R}_{13}$ and $\mathrm{R}_{14}$, $\mathrm{R}_{15}$, which set the limiting thresholds, could be common between channels. To gang the stereo channels together llimiting in one channel will produce a corresponding gain
change in the second channel to maintain the balance of the stereo image), then pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one pnp transistor and one capacitor $\mathrm{C}_{4}$ need be used. The release time will then be the product $5 \mathrm{KxC}_{4}$ since two channels are being supplied current from $\mathrm{C}_{4}$.

## USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 is not adequate for some applications. The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.
Figure 8-116 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8 V . This is easily accomplished by tying it to either pin 8 or 9 , the THD trim pins, since these pins sit at 1.8 V . An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about $10 \mu \mathrm{~V}$ in 20 kHz BW ). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply, ( $+\mathrm{V}_{\mathrm{cc}}$ and ground), it must have an input common mode range down to less than 1.8 V .


## N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate $600 \Omega$ input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.
Figure 8-117 shows the implementation of an N2 compressor. The input level of .245 V rms is stepped up to 1.41 Vrms by the $600 \Omega$ : $20 \mathrm{~K} \Omega$ matching transformer. The 20 K input resistor properly terminates the transformer. An internal $20 \mathrm{~K} \Omega$ resistor $\left(R_{3}\right)$ is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4 K output resistor and the $4 \mathrm{~K} \Omega$ : $600 \Omega$ output transformer. The .275V RMS output level

## FAST ATTACK, SLOW RELEASE HARD LIMITER




Figure 8-117
requires a 1.41 V op amp output level. This can be provided by increasing the value of $R_{2}$ with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for $\mathrm{R}_{2}$.

$$
\begin{gathered}
R_{2}=\frac{\text { Gain2 }_{2} R_{3} V_{\text {in }} \text { ave }}{R_{1} I_{B}}=\frac{12 \times 2 \times 20 \mathrm{~K} \times 1.27}{10 \mathrm{~K} \times 140 \mu \mathrm{~A}} \\
=36.3 \mathrm{~K}
\end{gathered}
$$

The external resistance required will thus be $36.3 \mathrm{~K}-20 \mathrm{~K}=16.3 \mathrm{~K}$.

The Bell compatible low level tracking characteristic is provided by the low level trim
resistor from Crect to Vcc. As shown in Figure 9-108 this will skew the system to a 1:1 transfer characteristic at low levels. The $2 \mu f$ rectifier capacitor provides attack and release times of 3 ms and 13.5 ms respectively , as shown in Figures 8-97 and 8-98. The R-C-R network around the op amp provides dc feedback to bias the output at dc.

An N2 expandor is shown in Figure 8-118. The input level of 3.27 Vrms is stepped down to 1.33 V by the $600 \Omega: 100 \Omega$ transformer, which is terminated with a $100 \Omega$ resistor for accurate impedance matching. The output impedance is accurately set by the $150 \Omega$ output resistor and the $150 \Omega$ : $600 \Omega$ output
transformer. With this configuration the 3.46 V transformer output requires a 3.46 V op amp output. To obtain this output level, it is necessary to increase the value of $R_{3}$ with an external trim resistor. The new value of $R_{3}$ can be found with the expandor gain equation.

$$
\begin{aligned}
R_{3}=\frac{R_{1} R_{2} I_{B} \text { Gain }}{2 V_{\text {in }} \text { ave }} & =\frac{10 \mathrm{~K} \times 20 \mathrm{~K} \times 140 \mu \mathrm{~A} \times 2.6}{2 \times 1.20} \\
& =30.3 \mathrm{~K}
\end{aligned}
$$

An external addition to $\mathrm{R}_{3}$ of 10 K is required, and this value can be selected to accurately set the high level gain.
A low level trim resistor from $\mathrm{C}_{\text {rect }}$ to $\mathrm{V}_{\mathrm{CC}}$ of about 3 Meg provides matching of the Bell low level tracking curve, and the $2 \mu$ f value of Crect provides the proper attack and release times. A 16 K resistor from the summing node to ground biases the output to 7 V dc.

## VOLTAGE CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage controlled amplifier (VCA). Figure 8-119 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of $-6 \mathrm{~dB} / \mathrm{V}$. Trim networks are shown to null out distortion and dc shift, and to fine trim gain to 0 dB with zero volts of control voltage.

Op amp $A_{2}$ and transistors $Q_{1}$ and $Q_{2}$ form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of $150 \mu \mathrm{~A}$, ( 15 V and $\mathrm{R}_{20}=100 \mathrm{~K}$ ), is attenuated a factor of two $(6 \mathrm{~dB})$ for every volt increase in

N2 EXPANDOR


Figure 8-118

## VOLTAGE CONTROLLED ATTENUATOR



Figure 8-119
the control voltage. Capacitor $\mathrm{C}_{6}$ slows down gain changes to a 20 ms time constant ( $C_{6} \times R_{1}$ ) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R18 assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R18 18 draws excess current out of the rectifier. After approximately 50 dB of attenuation at a $-6 \mathrm{~dB} / \mathrm{V}$ slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9 volts of control voltage. $\mathrm{A}_{1}$ should be a low noise high slew rate op amp. R $\mathrm{R}_{13}$ and $\mathrm{R}_{14}$ establish approximately a zero volt bias at $A_{1}$ 's output.

With a zero volt control voltage, $\mathrm{R}_{19}$ should be adjusted for OdB gain. At 1 V (-6dB gain) Rg should be adjusted for minimum distortion with a large $(+10 \mathrm{dBm})$ input signal. The output dc bias ( $\mathrm{A}_{1}$ output) should be meas-
ured at full attenuation $(+10 \mathrm{~V}$ control voltage) and then $\mathrm{R}_{8}$ is adjusted to give the same value at OdB gain. Properly adjusted, the circuit will give typically less than . $1 \%$ distortion at any gain with a dc output voltage variation of only a few millivolts. The clipping level $(140 \mu \mathrm{~A}$ into pin 3,14$)$ is $\pm 10 \mathrm{~V}$ peak. A signal to noise ratio of 90 dB can be obtained.
If several VCA's must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with $Q_{2}$ to control the other channels. The transistors should be maintained at the same temperature for best tracking.

## AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 8-120. This circuit hookup is very similar to the basic compressor shown in Figure 8-105, except that the rectifier input is tied to the
input rather than the output. This makes gain inversely proportional to input level so that a 20 dB drop in input level will produce a 20 dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of $\pm 1 \mathrm{dbm}$ for an input range of +14 to -43 dbm at 1 khz . Additional external components will allow the output level to be adjusted. Some relevant design equations are:

Output level $=\frac{R_{1} R_{2} I_{B}}{2 R_{3}}\left(\frac{V_{\text {in }}}{V_{\text {in }}(\text { avg })}\right) ; I_{B}=140 \mu \mathrm{~A}$
Gain $=\frac{R_{1} R_{2} I_{B}}{2 R_{3} V_{\text {in }}(\text { avg })}$ where
$\frac{V_{\text {IN }}}{V_{\text {IN }}(\text { avg })}=\frac{\pi}{2 \sqrt{2}}=1.11$ (for sine wave)

If ALC action at very low input levels is not desired, the addition of resistor $R_{X}$ will limit the maximum gain of the circuit.

$$
\text { Gain max. }=\frac{\frac{R_{1}+R_{X}}{1.8 V} \times R_{2} \times I_{B}}{2 R_{3}}
$$

The time constant of the circuit is determined by the rectifier capacitor, Crect, and an internal 10K resistor.

$$
\tau=10 \mathrm{~K} \mathrm{C}_{\mathrm{rect}}
$$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation.

$$
\mathrm{THD}=\left(\frac{1 \mu \mathrm{f}}{\mathrm{C}_{\text {rect }}}\right)\left(\frac{1 \mathrm{KHz}}{\text { freq. }}\right) \times .2 \%
$$

## VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than $2: 1$ can be achieved by the circuit shown in Figure 8-121. Rotation of the dual potentiometer causes the circuit hookup to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is $1: 1$, has neither compression or expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1, up to $1: 2$ expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 8-122.

## HI FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.
A major problem with the simple NE570 compressor (Figure 8-105) is the limited op amp gain at high frequencies. For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about $.6 \mathrm{v} / \mu \mathrm{s}$. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

## AUTOMATIC LEVEL CONTROL



Figure 8-120


Figure 8-121


Figure $8-123$ is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 8-123 is that the rectifier capacitor ( $\mathrm{C}_{9}$ ) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 8-104 and 8-105) become longer at low signal levels. The time constant is not simply 10 KxC rect, but is really

$$
\left(10 \mathrm{~K}+2\left(\frac{.026 \mathrm{~V}}{I_{\text {rect }}}\right)\right) \times \mathrm{C}_{\text {rect }}
$$

When the rectifier input level drops from 0 dBm to -30 dBm , the time constant increases from $10.7 \mathrm{KxC}_{\text {rect }}$ to $32.6 \mathrm{KxC}_{\text {rect. }}$ In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded the output will attempt to swing rail to rail. This compressor is limited to approximately a 7 V peak to peak output swing by the brute force clamp diodes $D_{3}$ and $D_{4}$. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.


The time it takes for the compressor to recover from overload is determined by the rectifier capacitor $\mathrm{C}_{9}$. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of $1 \mu$ f seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard. The compressor in Figure 8-123 contains a high frequency pre-emphasis circuit ( $C_{2}, R_{5}$ and $\left.C_{8}, R_{14}\right)$, which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could
make the pre-emphasis variable and further reduce breathing
The expandor to complement the compressor is shown in Figure 8-124. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0 dBm . Trim networks are shown for distortion (THD) and dc shift. The distortion trim should be done first, with an input of 0 dBm at 10 kHz . The dc shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.


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## sECTION 26 PHASE IOCKED IOOPS

## INTRODUCTION

Phase Locked Loop (PLLs) are a new class of monolithic circuits developed by Signetics, but they are based on frequency feedback technology which dates back 40 years.

A phase locked loop is basically an electronic servo loop consisting of a phase detector, a low pass filter and a voltage controlled oscillator. Its controlled oscillator phase makes it capable of locking or synchronizing with an incoming signal. If the phase changes, indicating the incoming frequency is changing, the phase detector output voltage increases or decreases just enough to keep the oscillator frequency the same as the incoming frequency, preserving the locked condition. Thus, the average voltage applied to the controlled oscillator is a function of the frequency of the incoming signal. In fact, the low pass filter voltage is the demodulated output when the incoming signal is frequency modulated (provided the controlled oscillator has linear voltage-to-frequency transfer characteristic). The synchronous reception of radio signals using PLL techniques was described (Ref. 1) in the early thirties. You may have heard of the "homodyne" receiver.

The first widespread use of the phase lock, however, was in TV receivers to synchronize the horizontal and vertical sweep oscillators to the transmitted sync pulses. Lately, narrowband phase locked receivers have proved to be of considerable benefit in tracking weak satellite signals because of their superior noise immunity. Applicaitons such as these were implemented primarily in discrete component form and involved considerable complexity even after the advent of transistors. This complexity made PLL techniques impractical or uneconomical in the majority of systems.

The development of complete, single-chip phase locked loops has changed this situation considerably. Now, a single packaged device with a few external components will offer the user all the benefits of phase locked loop operation, including independent center frequency and bandwidth adjustment, high noise immunity, high selectivity, high frequency operation and center frequency tuning by means of a single external component.

Signetics makes three basic classes of single-chip PLL circuits: the general purpose PLL, the PLL with an added multiplier and the PLL tone decoder.
The $560 \mathrm{~N}, 562 \mathrm{~N}$ and 565 are general purpose phase locked loops containing an oscillator, phase detector and amplifier. When locked to an incoming signal, they provide two outputs: a voltage proportional
to the frequency of the incoming signal (FM output) and the square wave oscillator output which, during lock, is equal to the incoming frequency. All general purpose devices are optimized to provide a linear frequency-to-voltage transfer characteristic.

The 561 N contains a complete PLL as those above, plus the additional multiplier or quadrature phase detector required for AM demodulation. In addition to the standard FM and oscillator outputs, it also provides an output voltage which is proportional to the amplitude of the incoming signal (AM output). The 561 N is opitmized for highly linear FM and AM demodulation.
The 567 is a special purpose phase locked loop intended solely for use as a tone decoder. It contains a complete PLL including oscillator, phase detector and amplifier as well as a quadrature phase detector or multiplier. If the signal amplitude at the locked frequency is above a minimal value, the driver amplifier turns on, driving a load as much as 200 mA . It, thus, gives an output whenever an inband tone is present. The 567 is optimized for both center frequency and bandwidth stability.
The 566 is not a phase locked loop, but a precision voltage-controllable waveform generator derived from the oscillator of the 565 general purpose loop. Because of its similarity to the 565 and because it lends itself well to use in, and in conjunction with, phased locked loops, it has been included in this section.

Table 9-1 summarizes the characteristics of Signetics phase locked loop products.

A considerable quantity of detailed specifications and publications information for these products is included in the Linear Spec. Handbook. Because many readers are likely to be unfamiliar with the terminology and operating characteristics of phase locked loops, a glossary of terms and a general explanation of PLL principles are included here with a detailed discussion of the action of the individual loop elements.

The tradeoff and setup section will assist the reader in some of the considerations involved in selecting and applying the loop products to meet system requirements. A brief summary of measurement techniques has been presented to aid the user in achieving his performance goals.

Detailed descriptions have been provided for each of the loop products. The user can supplement the suggested connection diagrams with his own schemes.
Perhaps the best way to become familiar with the many uses of phase locked loops is
to actually study the various application circuits provided. These circuits have been drawn from many sources-textbooks, users, Signetics' applications engineers and the 1970 Signetics-EDN Phase Locked Loop contest. Every effort has been made to provide usable, workable circuits which may be copied directly or used as jumpingoff points for other imaginative applications.
The section on interfacing will aid the user in driving different forms of logic from PLL outputs and the section on expanding loop capabilities will show how to achieve improved performance in certain difficult applications.

## PHASED LOCKED LOOP TERMINOLOGY

The following is a brief glossary of terms encountered in PLL literature.

Capture Range ( $2 \omega c$ )-Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes. The range over which the loop can acquire lock is termed capture range. The capture range is sometimes called the Lock-in Range.(The latter refers to how close a signal must be to the center frequency before acquisition can occur. It is thus one-half the capture range of $\omega \mathrm{c}$.)
Current Controlled Oscillator ( CCO )-An oscillator similar to a VCO in which the frequency is determined by an applied current.

Damping Factor ( $\zeta$ )-The standard damping constant of a second order feedback system. In the case of the PLL, it refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.
Free-Running Frequency ( $f_{0}, \omega_{0}$ )-Also called the Center Frequency, this is the frequency at which the loop VCO operates when not locked to an input signal. The same symbols ( $f_{0}, \omega_{0}$ ) used for the freerunning frequency are commonly used for the general oscillator frequency. It is usually clear which is meant from the context.

Lock Range ( $2 \omega \mathrm{~L}$ )-The range of input frequencies over which the loop will remain in lock. It is also called the Tracking Range or Hold-In Range. (The latter refers to how far the loop frequency can be deviated from the center frequency and is one-half the lock range or $\omega \mathrm{L}$.)
Loop Gain $\left(K_{v}\right)$-The product of the dc gains of all the loop elements, in units of (sec)-1.

| USER'S QUICK-LOOK GUIDE TO SIGNETICS PLLs |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | UPPER FREQUENCY (MHz) | MAXIMUM LOCK RANGE (\%fo) | FM DISTORTION | OUTPUT <br> SWING $\pm 5 \%$ DEVIATION (volts p-p) | CENTER FREQUENCY STABILITY (ppm $/{ }^{\circ} \mathrm{C}$ ) | FREQUENCY DRIFT WITH SUPPLY VOLTAGE (\%/volt) | INPUT RESISTANCE | AM OUTPUT AVAILABLE | TYPICAL SUPPLY CURRENT (mA) | SUPPLY VOLTAGE RANGE (volts) |
| NE560 | 30 | 40\% | . $3 \%$ | 1 | $\pm 600$ | . 3 | 2K** | No | 9 | +16 to +26 |
| NE561 | 30 | 40\% | . $3 \%$ | 1 | $\pm 600$ | . 3 | 2K** | Yes | 10 | +16 to +26 |
| NE562 | 30 | 40\% | .5\% | 1 | $\pm 600$ | . 3 | 2K** | No | 12 | +16 to +30 |
| NE564 | 50 | 40\% | .5\% | . 1 | $\pm 400$ | . 3 | 3K | No | 30 | +4.5 to +12 |
| NE565 | . 5 | 120\% | . $2 \%$ | . 15 | $\pm 200$ | . 16 | 5K | No | 8 | $\pm 5$ to $\pm 12$ |
| SE565 | . 5 | 120\% | .2\% | . 15 | $\pm 100$ | . 08 | 5K | No | 8 | $\pm 5$ to $\pm 12$ |
| NE567 | . 5 | 14\% | 5\%* | . 20 | $35 \pm 60$ | . 7 | 20K** | Yes* | 7 | $\pm 4.5$ to +9 |
| SE567 | . 5 | 14\% | 5\%* | . 20 | $35 \pm 60$ | . 5 | 20K** | Yes* | 6 | + 4.5 to +9 |
| NE566 | . 5 |  | .2\% | 30\%/V*** | $\pm 200$ | . 16 |  |  | 7 | +10 to +26 |
| SE566 | . 5 |  | .2\% | 30\%/V*** | $\pm 100$ | . 08 |  |  | 7 | +10 to +26 |
| * The 567 AM and FM outputs are available, but are not optimized for linear demodulation. <br> ** Input biased internally. <br> *** Figure shown is VCO gain in percent deviation per volt. |  |  |  |  |  |  |  |  |  |  |

Table 9-1

Loop Noise Bandwidth (BL)-A loop property related to damping and natural frequency which describes the effective bandwidth of the received signal. Noise and signal components outside this band are greatly attenuated.

Low Pass Filter (LPF)-A low pass filter in the loop which permits only dc and low frequency voltages to travel around the loop. It controls the capture range and the noise and out-band signal rejection characteristics.

Natural Frequency ( $\omega n$ )-The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane. May be determined experimentally as the modulation frequency for which an underdamped loop gives the maximum output and at which phase error swing is the greatest.

Phase Detector Gain Factor ( $K_{d}$ )-The conversion factor between the phase detector output voltage and the phase difference between input and VCO signals in volts/radian. At low input signal amplitudes, the gain is also a function of input level.
Phase Detector (PD)-A circuit which compares the input and VCO signals and produces an error voltage which is dependent upon their relative phase difference. This error corrects the VCO frequency during tracking. Also called Phase Comparator. A Multiplier or Mixer is often used as a phase detector.
Quadrature Phase Detector (QPD)-A phase detector operated in quadrature $\left(90^{\circ}\right.$ out of phase) with the loop phase detector. It is used primarily for AM demodulation and lock detection.


VCO Conversion Gain ( $K_{o}$ )-The conversion factor between VCO frequency and control voltage in radians/second/volt.
Voltage Controlled Oscillator (VCO)-An oscillator whose frequency is determined by an applied control voltage.

## THE PHASE LOCKED LOOP PRINCIPLE

The phase locked loop is a feedback system comprised of a phase comparator, a low pass filter and an error amplifier in the forward signal path and a voltagecontrolled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 9-1. Detailed analysis of the PLL as a feedback control system has been discussed in the literature (Ref. 2). Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. The parameters in the equations are somewhat different,
however, since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

## Loop Operation

A rigorous mathematical analysis of the system is quite cumbersome and will not be repeated here. However, from a qualitative point of view, the basic principle of PLL operation can be briefly explained as follows: With no signal input applied to the system, the error voltage $\mathrm{V}_{\mathrm{d}}$ is equal to zero. The VCO operates at a set frequency $\omega_{0}$, which is known as the free-running frequency. If an output signal is applied to the system. the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $\mathrm{V}_{\mathrm{e}}(\mathrm{t})$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified and applied to the control terminal of the VCO. In this manner, the control voltage $\mathrm{V}_{\mathrm{d}}(\mathrm{t})$ forces the VCO fre-
quency to vary in a direction that reduces the frequency difference between $f_{0}$ and the input signal. If the input frequency $\omega_{i}$ is sufficiently close to $\omega_{0}$, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference. This net phase difference $\theta_{0}$ is necessary to generate the corrective error voltage $V_{d}$ to shift the VCO frequency from its free-running value to the input signal frequency $\omega_{i}$ and, thus, keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the "lock range."

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multipler circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_{i} \pm \omega_{0}$ shown in Figure 9-1. When the loop is in lock, the VCO duplicates the input frequency so that the difference frequency component ( $\omega \mathrm{i}$ $\omega_{0}$ ) is zero; hence, the output of the phase comparator contains a dc component. The low pass filter removes the sum frequency component ( $\omega \mathrm{i}=\omega_{0}$ ) but passes the dc component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always dc, so the lock range is independent of the band edge of the low pass filter.

## Lock and Capture

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. Now, however, the difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to
be transmitted through the low pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal. The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency selective properties.
It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as the frequency range usually centered about the VCO initial free running frequency over which the loop can track the input signal once lock has been achieved.

When the loop is in lock, the difference frequency component on the output of the phase comparator (error voltage) is dc and will always be passed by the low pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

## The Capture Transient

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows: Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as
(Equation 9-1)

$$
\Delta \omega=\frac{\mathrm{d} \theta_{0}}{\mathrm{~d}_{\mathrm{t}}}
$$

where $\Delta \omega$ is the instantaneous frequency separation between the signal and VCO frequencies and $\theta_{0}$ is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL was opened, say between the low pass filter and the VCO control input, then for a given condition of $\omega_{0}$ and $\omega_{i}$ the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta \omega$. If $\omega_{i}$ and $\omega_{0}$ were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation. Now suppose that the feedback loop is closed by connecting the low pass
filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta \omega$ itself will become a function of time. If during this modulation process, the VCO frequency moves closer to $\omega_{i}(i . e .$, decreasing $\Delta \omega$ ), then $\mathrm{d} \theta_{0} / \mathrm{d}_{\mathrm{t}}$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from $\omega_{\mathrm{i}}, \mathrm{d} \theta / \mathrm{d}_{\mathrm{t}}$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure $9-2 a$. Because of its asymmetry, the beat note waveform contains a finite dc component that pushes the average value of the VCO toward $\omega$ i, thus increasing $\Delta \omega$. In this manner, the beat note frequency rapidly decreases toward zero, the VCO frequency drifts toward $\omega_{i}$ and the lock is established. When the system is in lock, $\Delta \omega$ is equal to zero and only a steady-state dc error voltage remains.
Figure 9-2b displays an oscillogram of the loop error voltage $\mathrm{V}_{\mathrm{d}}$ in an actual PLL system during the capture process. Note that as lock is approached, $\Delta \omega$ is reduced, the low pass filter attenuation becomes less and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called the pull-in time. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.
A specific case to illustrate this is shown in Figure 9-3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first order loop (no low pass filter) and the input toneburst frequency was within its lock and capture range.

## Effect of the Low Pass Filter

In the operation of the loop, the loop pass filter serves a dual function: First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the inteference-rejection characteristics; second, it provides a shortterm memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. The low pass filter bandwidth has the following effects on system performance:

## ASYNCHRONOUS ERROR BEAT FREQUENCY DURING the Capture process



Figure 9-2a


Figure 9-2b

## FAST CAPTURE EXHIBITED BY FIRST ORDER LOOP



Figure 9-3


Figure 9-4
a. The capture process becomes slower and the pull-in time increases.
b. The capture range decreases.
c. Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low pass filter.
d. The transient responce of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes undamped.

The last effect also produces a practical limitation on the low pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

## Linear Analysis for Lock Condition-Frequency Tracking

When the PLL is in lock, the non-linear capture transients are no longer present. Therefore, under lock condition, the PLL can often be approximated as a linear control system (see Figure 9-4) and can be analyzed using Laplace transform techniques. In this case, it is convenient to use the net phase error in the loop ( $\theta_{\mathrm{s}}-\theta_{0}$ ) as the system variable. Each of the gain terms associated with the blocks can be defined as follows:
$K_{d}=$ conversion gain of phase detector (volt/rad)
$F(s)=$ transfer characteristic of low pass filter
$A=$ amplifier voltage gain
$K \theta=V C O$ conversion gain (rad/sec/volt)

Note that, since the VCO converts a voltage to a frequency and since phase is the integral of frequency, the VCO functions as an integrator in the feedback loop.

The open loop transfer function for the PLL can be written as
(Equation 9-2)

$$
T(s)=\frac{K_{v} F(s)}{s}
$$

where $K_{v}$ is the total loop gain, i.e., $K_{v}=$ $K_{0} K_{d} A$. Using the linear feedback analysis techniques, the closed loop transfer characteristics $\mathrm{H}(\mathrm{s})$ can be related to the open loop performance as
(Equation 9-3)

$$
H(s)=\frac{T(s)}{1+T(s)}
$$

and the roots of the characteristic system polynomial can be readily determined by root locus techniques.
From these equations, it is apparent that the transient performance and frequency re-
sponse of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, $\mathrm{F}(\mathrm{s})$.
The simplest case is that of the first order loop where $F(s)=1$ (no filter). The closed loop transfer function then becomes
(Equation 9-4)

$$
T(s)=\frac{K_{v}}{s+K_{v}}
$$

This transfer function gives the root locus as a function of the total loop gain $\mathrm{K}_{\mathrm{v}}$ and the corresponding frequency response shown in Figure 9-5a. The open loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency modulated input signal. Since there is no low pass filter in this case, sum frequency components are also present on the phase detector output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

With the addition of a single pole low pass filter $F(s)$ of the form
(Equation 9-5)

$$
\mathrm{F}(\mathrm{~s})=\frac{1}{1+\tau 1 \mathrm{~s}}
$$

where $\tau 1=$ R1C, the PLL becomes a second order system with the root locus shown in Figure 9-5b. Here, we again have an open loop pole at the origin because of the integrating action of the VCO and another open loop pole at a position equal to $-1 / \tau 1$ where $\tau 1$ is the time constant of the low pass filter.
One can make the following observations from the root locus characteristics of Figure 9-5b.
a. As the loop gain $\mathrm{K}_{\mathrm{v}}$ increases for a given choice of $\tau 1$, the imaginary part of the closed loop poles increase; thus, the natural frequency of the loop increases and the loop becomes more and more undamped.
b. If the filter time constant is increased, the real part of the closed loop poles becomes smaller and the damping is reduced.
As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 9-5b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.


Figure 9-5a


Figure 9-5b


Figure 9-5c

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 9-5c. This type of filter has a transfer function
(Equation 9-6)

$$
F(\mathbf{s})=\frac{1+\tau_{2} \mathbf{S}}{1+\left(\tau_{1}+\tau_{2}\right) \mathbf{S}}
$$

where $\tau_{2}=$ R2C and $\tau_{1}=$ R1C. By the proper choice of R2, this type of filter confines the
root locus to the left half plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of $\tau_{1}$ and $\tau_{2}$. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first and second order loops and it provides an additional control over the loop transient response. If R2 $=0$, the loop
behaves as a second order loop and if R2 = $\infty$, the loop behaves as a first order loop due to a pole-zero cancellation. Note, however, that as first order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

In terms of the basic gain expressions in the system, the lock range of the PLL $\omega$ L can be shown to be numerically equal to the dc loop gain
(Equation 9-7)

$$
2 \omega \mathrm{~L}=4 \pi \mathrm{f}_{\mathrm{L}}=2 \mathrm{~K}_{\mathrm{v}}
$$

Since the capture range $\omega_{c}$ denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as

$$
2 \omega_{C}=4 \pi f_{C} \simeq 2 K_{V} \bullet F\left(j \omega_{C}\right)
$$

(Equation 9-8)
where $F\left(j \omega_{c}\right)$ is the low pass filter amplitude response at $\omega=\omega \mathrm{L}$. Note that at all times the capture range is smaller than the lock range. If the simple lag filter of Figure $9-5 b$ is used, the capture range equation can be approximated as

$$
2 \omega_{\mathrm{c}} \simeq 2 \sqrt{\frac{\omega \mathrm{~L}}{\tau 1}} \sqrt{\frac{\mathrm{~K}_{\mathrm{v}}}{\tau 1}}
$$

(Equation 9-9)

Thus, the capture range increased as the low pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 9-6 shows the typical frequency-tovoltage transfer characterisitcs of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 9-6a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches frequency $\omega_{1}$, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, $\mathrm{V}_{\mathrm{d}}$ varies with frequency with a slope equal to the reciprocal of VCO gain ( $1 / \mathrm{K}_{0}$ ) and goes through zero as $\omega_{i}=\omega_{0}$. The loop tracks the input until the input frequency reaches $\omega 2$, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back now, the cycle repeats itself, but it is inverted, as shown in Figure 9-6b. The loop recaptures the signal at $\omega_{3}$ and tracks it down to $\omega_{4}$. The total capture and lock ranges of the system are:

## TYPICAL PLL FREQUENCY- TO-VOLTAGE TRANSFER CHARACTERISTICS FOR INPUT FREQUENCY INCREASING AND DECREASING



Figure 9-6


$$
2 \omega_{\mathrm{C}}=\omega_{3}-\omega_{1} \text { and } 2 \omega_{\mathrm{L}}=\omega_{2}-\omega_{4}
$$

Note that, as indicated by the transfer characteristics of Figure 9-6, the PLL system has an inherent selectivity about the center frequency set by the VCO free-running frequency $\omega_{0}$. It will respond only to the input signal frequencies that are separated from $\omega_{o}$ by less than $\omega_{c}$ or $\omega_{\mathrm{L}}$, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

## PHASE LOCKED LOOP BUILDING BLOCKS

## Voltage Controlled Oscillator

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.
When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by $\mathrm{K}_{\mathrm{o}}$ (in radian/sec/volt).
(Equation 9-11)

$$
K_{0}=\frac{\Delta \omega_{0}}{\Delta V_{0}}
$$

Since the output voltage is the VCO voltage, we can get the loop output voltage as
(Equation 9-12)

$$
\Delta V_{0}=\frac{\Delta \omega_{0}}{K_{0}}
$$

The gain $K_{0}$ can be found from the data sheet by taking the change in VCO control voltage for a given percentage frequency deviation and multiplying by the center frequency. When the VCO voltage is changed, the frequency change is virtually instantaneous.

## Phase Detector

All Signetics phase locked loops use the same form of phase detector-often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 9-7.
The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has a collector resistance $R_{c}$ and whose differential gain at balance is the ratio of $R_{C}$ to the emitter resistance $r_{e}$ of Q1 and Q2.
(Equation 9-13)

$$
A_{d}=\quad \frac{R_{C}}{r_{e}}=\frac{R_{C}}{\frac{0.026}{l_{e} / 2}}=\frac{R_{C}}{0.0131_{e}}
$$

The switching stage formed by Q3 - Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by -1 . That is, when the base of $Q 4$ is positive, $R_{c 2}$ receives 11 and when the base of Q6 is positive, $R_{c} 2$ receives $I 2=11$. Since we have called this a multiplier, let us perform the multiplication to gain further insight into the action of the phase detector.

Suppose we have an input signal which consists of two added components: a component at frequency $\omega_{i}$ which is close to the free-running frequency and a component at frequency $\omega_{k}$ which may be at any frequency. The input signal is
(Equation 9-14)

$$
V_{i}+V_{k}=V_{i} \sin \left(\omega_{i} t+\theta_{i}\right)+V_{k} \sin \left(\omega_{k} t+\theta_{k}\right)
$$

where $\theta_{\mathrm{i}}$ and $\theta_{\mathrm{k}}$ are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is
(Equation 9-15)

$$
\frac{4}{\pi(2 n+1)} \sin \left[(2 n+1) \omega_{o} t\right]
$$

where $\omega_{0}$ is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationship and inserting the differential stage gain $A_{d}$, we get
(Equation 9-16)
$V_{d}=$

 $\left.-\sum_{n=0}^{\infty} \frac{v_{k}}{(2 n+1)} \cos \left[(2 n+1) \omega_{o} t+\omega k t+\theta_{k}\right]\right]$

Assuming the $\mathrm{V}_{\mathrm{k}}$ is zero, temporarily, if $\omega_{i}$ is close to $\omega_{0}$, the first term ( $n=0$ ) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock up by modulating the VCO. As $\omega_{0}$ is driven closer to $\omega \mathrm{i}$, this difference component becomes lower and lower in frequency until $\omega_{0}=\omega_{\mathrm{i}}$ and lock is achieved. The first term then becomes
(Equation 9-17)

$$
\frac{2 \mathrm{~A}_{d} \mathrm{~V}_{\mathrm{i}}}{\pi} \cos \theta_{\mathrm{i}}
$$

which is the usual phase detector formula showing the dc component of the phase detector during lock. This component must equal the voltage necessary to keep the VCO at $\omega_{0}$. it is possible for $\omega_{0}$ to equal $\omega_{i}$

momentarily during the lock up process and, yet, for the phase to be incorrect so that $\omega_{o}$ passes through $\omega_{i}$ without the lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega$ i $=\omega_{0}$ at $\mathrm{t}=0$.

If $n \neq 0$ in the first term, the loop can lock when $\omega_{\mathrm{i}}=(2 n+1) \omega_{0}$, giving the dc phase detector component
(Equation 9-18)

$$
\frac{2 \mathrm{~A}_{d} \mathrm{~V}_{\mathrm{i}}}{\pi(2 \mathrm{n}+1)} \cos \theta_{\mathrm{i}}
$$

showing that the loop can lock odd harmonics of the center frequency. The $(2 n+1)$ term in the denominator shows that the phase detector output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase detector during lock is (assuming $A_{d}$ is constant) also a function of the input amplitude $\mathrm{V}_{\mathrm{i}}$. Thus, for a given dc phase detector output $V_{d}$, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for $\theta_{i}$ between 0 and $180^{\circ}$, the lower $V_{i}$ becomes, the more reduced is the lock range.

Going to the second term, we note that during lock the lowest possible frequency is $\omega_{0}+\omega_{i}=2 \omega_{i}$. A sum frequency component is always present at the phase detector output. This component is usually greatly attenuated by the low pass filter capacitor connected to the phase detector output. However, when rapid tracking is required (as with high-speed FM detection or FSK-frequency shift keying), the requirement for a relatively high frequency cutoff in the low pass filter
may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that we have other frequencies represented by $V_{k}$ present. What is their effect for $V_{k} \neq 0$ ?

The third term shows that $V_{k}$ introduces another difference frequency component. Obviously, if $\omega_{k}$ is close to $\omega_{\mathrm{i}}$, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. Suppose lock has been achieved, however, so that $\omega_{0}=\omega_{\mathrm{i}}$. In order for lock to be maintained, the average phase detector output must be constant. If $\omega_{0}=\omega_{k}$ is relatively low in frequency, the phase $\theta_{i}$ must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since $\omega \mathrm{k}$ is often far removed from $\omega \mathrm{i}$. However, it has been stated that the phase $\theta_{i}$ can move only between 0 and $180^{\circ}$. Suppose the phase limit has been reached and $\mathrm{V}_{\mathrm{k}}$ appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If $\mathrm{V}_{\mathrm{k}}$ is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. We can reduce this effect by decreasing the cutoff frequency of the low pass filter so that the wo $-\omega_{k}$ is attentuated to a greater extent, which illustrates that noise immunity and out-
band frequency rejection is improved (at the expense of capture range since $\omega_{0}-\omega_{i}$ is likewise attenuated) when the low pass filter capacitor is large.
The third term can have a dc component when $\omega_{k}$ is an odd harmonic of the locked frequency so that $(2 n+1)\left(\omega_{0}-\omega_{j}\right)$ is zero and $\theta_{k}$ makes its appearance. This will have an effect on $\theta_{i}$ which will change the $\theta_{i}$ versus frequency $\omega \mathrm{i}$. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The $\theta_{\mathrm{k}}$ term will combine with the $\theta_{\mathrm{i}}$ term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude $V_{i}$ is large and the loop gain is large, the phase will be close to $90^{\circ}$ throughout the range of VCO swing, so this effect is often unnoticed.
The fourth term is of little consequence except that if $\omega_{k}$ approaches zero, the phase detector output will have a component at the locked frequency $\omega_{0}$ at the output. For example, a dc offset at the input differential stage will appear as a square wave of fundamental $\omega_{0}$ at the phase detector output. This is usually small and well attenuated by the low pass filter. Since many out-band signals or noise components may be present, many $\mathrm{V}_{\mathrm{k}}$ terms may be combining to influence locking and phase during lock. Fortunately, we need only worry about those close to the locked frequency.
The quadrature phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase $\theta_{i}$ is $90^{\circ}$, the quadrature phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature phase detector is given by:

$$
\mathrm{V}_{\mathrm{q}}=\frac{2 \mathrm{~A}_{\mathrm{q}} \mathrm{~V}_{\mathrm{i}}}{\pi} \sin \theta_{\mathrm{i}} \quad \text { (Equation 9-19) }
$$

where $V_{i}$ is the constant or modulated AM signal and $\theta_{i} \approx 90^{\circ}$ in most cases so that sine $\theta_{\mathrm{i}}=1$ and
(Equation 9-20)

$$
V_{q}=\frac{2 A_{q} V_{i}}{\pi}
$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

## FUNCTIONAL APPLICATIONS

## Low Pass Filter

The simplest type of low pass filter for the second order loop is a single pole RC type shown in Figure 9-5b. In all Signetics' loops, the resistor is internal and the capacitor is external. The inside resistor greatly im-
proves the center frequency stability of the loop with temperature variations. Fortunately, the capture range and loop damping are related to the square root of this internal resistor value, so variations in its absolute value have little effect on loop performance. The nominal value of the internal resistor for each loop is given in the circuit diagrams of the detailed circuit descriptions in this chapter. The typical tolerance on these integrated resistors is $\pm 20 \%$.

As a functional building block, the phase locked loop is suitable for a wide variety of frequency related applications. These applications generally fall into one or more of the following categories:
a. FM demodulation
b. Frequency synthesizing
c. Frequency synchronization
d. Signal conditioning
e. AM demodulation

## FM Demodulation

If the PLL is locked to a frequency modulated (FM) signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage, which forces the VCO to maintain lock with the input signal then becomes the demodulated FM output. The linearity of this demodulated signal depends solely on the linearity of the VCO control-voltage-to-frequency transfer characteristic.
It should be noted that since the PLL is in lock during the FM demodulation process, the response is linear and can be readily predicted from a root locus plot.

FM demodulation applications are numerous; however, some of the more popular are:

## BROADCAST FM DETECTION

Here, the PLL can be used as a complete IF strip, limiter and FM detector which may be used for detecting either wide or narrow
band FM signals with greater linearity than can be obtained by other means. For frequencies within the range of the VCO, the PLL functions as a self contained receiver since it combines the functions of frequency selectivity and demodulation. One increasingly popular use of the PLL is in scanning-receivers where a number of broadcast channels may be sequentially monitored by simply varying the VCO freerunning frequency.

## FM TELEMETRY

This application involves demodulation of a frequency modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67 kHz frequency modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure $9-8$ to a point between the FM discriminator and the deemphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial free background music.

## FREQUENCY SHIFT KEYING (FSK)

This refers to what is essentially digital frequency modulation. FSK is a means for transmitting digital information by a carrier which is shifted between two discrete frequencies. In this case, the two discrete frequencies correspond to a digital " 1 " and a digital " 0 ," respectively. When the PLL is locked to a FSK signal, the demodulated output (error voltage) shifts between two discrete voltage levels, corresponding to the demodulated binary output. FSK techniques are often used in modems (modulator-demodulators), intended for transmitting data over telephone lines.

SCA DECODER


Figure 9-8

## FREQUENCY SYNTHESIZER

Frequency Multiplication can be achieved with the PLL in two ways:
a. Locking to a harmonic of the input signal b. Insertion of a counter (digital frequency divider) in the loop

Harmonic locking is the simplest and can usually be achieved by setting the VCO freerunning frequency to a multiple of the input frequency and allowing the PLL to lock. A limitation on this scheme, however, is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.
A block diagram of the second scheme is shown in Figure 9-9. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input frequency so that the VCO is actually running at a
multiple of the input frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property, is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency component is dc and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental $F M$ on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture
range and a more underdamped loop transient response.

For the case of frequency fractionalization, both harmonic locking and frequency countdown could be used to generate, for instance, a frequency exactly $16 / 3$ the input. In this case, the circuit of Figure 9-10 could be used with the initial VCO frequency set to approximately $16 / 3$ the expected input frequency. The counter then divides the VCO frequency by 16 , and the input is locked to the 3rd harmonic of the counter output. Now the output can be taken as the VCO output and it will be exactly $16 / 3$ of the input frequency as long as the loop is in lock.

Frequency translation can be achieved by adding a mixer and a low pass filter stage to the basic PLL as shown in Figure 9-11. With this system the PLL can be used to translate the frequency of a highly stable but fixedfrequency reference oscillator by a small amount in frequency.

In this case, the reference input $f_{r}$ and the VCO output $f_{0}$ are applied to the inputs of

## BLOCK DIAGRAM OF FREQUENCY SYNTHESIZER USING FREQUENCY DIVIDER



Figure 9-9

## IMPLEMENTATION OF FREQUENCY SYNTHESIZER (565)



Figure 9-10

## FREQUENCY TRANSLATION OR "OFFSET" LOOP



Figure 9-11
the mixer stage. The mixer output is made up of the sum and the difference components of $f_{r}$ and $f_{0}$. The sum component is filtered by the first low pass filter. The translation or offset frequency $f_{\dagger}$ is applied to the phase comparator along with the $f_{r}-f_{0}$ component of the mixer output. When the system is in lock, the two inputs of the phase comparator are at identical frequency, that is,
(Equation 9-21)

$$
f_{0}-f_{R}=f_{1} \text { or } f_{0}=f_{R}+f_{1}
$$

## Frequency Synchronization

Using the phase locked loop system, the frequency of the less precise VCO can be phase locked with a low level but highly stable reference signal. Thus, the VCO output reproduces the reference signal frequency at the same per-unit accuracy, but at a much higher power level. In some applications, the synchronizing signal can be in the form of a low duty cycle burst at a specific frequency. Then, the PLL can be used to regenerate a coherent CW reference frequency locking onto this short synchronizing pulse. A typical example of such an application is seen in the phase locked chroma-reference generators of color television receivers.

In digital systems, the PLL can be used for a variety of synchronization functions. For example, two system clocks can be phase locked to each other such that one can function as a back up for the other; or PLLs can be used in synchronizing disk or tape drive mechanisms in information storage and retrieval systems. In pulse-code modulation (PCM) telemetry receivers or in repeater systems, the PLL is used for bit synchronization.

Other popular applications include locking to WWVB to generate an inexpensive laboratory frequency standard and synchronizing tape speed for playback of a tape recorded at an irregular speed.

## Signal Conditioning

By proper choice of the VCO free-running frequency, the PLL can be made to lock to any one of a number of signals present at the input. Hence, the VCO output reproduces the frequency of the desired signal, while greatly attenuating the undesired frequencies of sidebands present at the input.

If the loop bandwidth is sufficiently narrow, the signal-to-noise ratio at the VCO output can be much better than that at the input. Thus, the PLL can be used as a noise filter for regenerating weak signals buried in noise.

## AM Demodulation

AM demodulation may be achieved with PLL by the scheme shown in Figure 9-12. In this mode of operation, the PLL functions as a synchronous AM detector. The PLL locks on the carrier of the AM signal so that the VCO output has the same frequency as that of the carrier but no amplitude modulation. The demodulated AM is then obtained by multiplying the VCO signal with the modulated input signal and filtering the output to remove all but the difference frequency component. It may be recalled from the initial discussion that when the frequency of the input signal is identical to the freerunning frequency of the VCO, the loop goes into lock with these signals $90^{\circ}$ out of phase. If the input is now shifted $90^{\circ}$ so that it is in phase with the VCO signal and the two signals are mixed in a second phase comparator, the average dc value (difference frequency component) of the phase comparator output will be directly proportional to the amplitude of the input signal.

The PLL still exhibits the same capture range phenomena discussed earlier so that the loop has an inherent high degree of selectivity centered about the free-running VCO frequency. Because this method is essentially a coherent detection technique which involves averaging of the two compared signals, it offers a higher degree of noise immunity than can be obtained with conventional peak-detector-type AM demodulators.

## GENERAL LOOP SETUP AND TRADEOFFS

In a given application, maximum PLL effectiveness can be achieved if the user understands the tradeoffs which can be made. Generally speaking, the user is free to select the frequency, tracking or lock range, capture range and input amplitude.

## Center Frequency Selection

Setting the center frequency is accomplished by selecting one or two external
components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the difference between the incoming and free-running frequencies, the band edges of the capture range are always an equal distance (in Hz ) from the center frequency. Typically, the lock range is also centered about the freerunning frequency. Occasionally, the center frequency is chosen to be offset from the incoming so that detection or tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow band operation (reduced tracking speed).
All of Signetics' loops use a multiplier in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, $1 / 3$ or $1 / 5$ of the input signal. The tracking range, however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase detector discussion would suggest that the PLL cannot lock to subharmonics because the phase detector cannot produce a dc component if $\omega$ i is less than $\omega_{0}$.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at $f_{o}$. For example, a square wave of fundamental $f_{0} / 3$ will have a substantial component at $f_{o}$ to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven the resultant internal limiting generates harmonic frequencies). Locking to even harmonics or subharmonics is the least satisfactory since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the sym-


Figure 9-12
metrical to generate substantial even harmonic content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest $f_{0}$. This magnitude can be used to estimate the capture and lock range.

All of Signetics' loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature compensated over the entire military temperature range ( -55 to $+125^{\circ} \mathrm{C}$ ). To benefit from this inherent stability, however, the user must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the user may wish to trade some stability for lower cost external components.

## Tracking or Lock Range Control

Two things limit the lock or tracking range. First, any VCO can only swing so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase detector is proportional to the product of both the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. It often happens with low input amplitudes that even the full $\pm 90^{\circ}$ phase range of the phase detector cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. We must, therefore, give up some tracking capability and accept greater phase errors if the input signal is weak. Conversely, a strong input signal will allow us to use the entire VCO swing capability and keep the VCO phase (referred to the input signal) very close to $90^{\circ}$ throughout the range. Note that tracking range does not depend on the low pass filter. However, if a low pass filter is in the loop, it will have the effect of limiting the maximum rate at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0 or $180^{\circ}$. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the L.PF should have a high cutoff frequency. However, a high cutoff frequency LPF will atten-
uate the sum frequencies to a lesser extent so that our output contains a significant and often bothersome signal at twice the input frequency. (Remember that the multiplier forms both the sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present.) This sum frequency component can then be filtered out with an external low pass filter.

## Capture Range Control

There are two main reasons for making the low pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase detector output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase detector to drive the VCO towards the input frequency. If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

## Choice of Input Level

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the tracking (lock) and capture range becomes independent of signal amplitude.
Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase detector gain and will result in a lock range which becomes constant with amplitude as the phase detector gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

## Lock-Up Time and Tracking Speed Control

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applica-
tions. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speed.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.
a. Input phase
b. Low pass filter characteristic
c. Loop damping
d. Deviation of input frequency from center frequency
e. In-band input amplitude
f. Out-band signals and noise
g. Center frequency

Fortunately, it is usually sufficient to know how we can improve the lock-up time and what we must tradeoff to get faster lock-up. Suppose we have set up a loop or tone decoder and find that occasionally the lockup transient is too long. What can be done to improve the situation-keeping in mind the factors that influence lock?
a. Initial phase relationship between incoming signal and VCO - This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency away from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 9-13 gives a typical distribution of lockup times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at $t$ $=0$. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of pulse train and the transmitted tone phase-related to the same pulse train. Usually, however, the incoming phase cannot be controlled.
b. Low pass filter - The larger the low pass filter time constant, the longer will be the lock-up time. We can reduce lock-up time by decreasing the filter time constant, but in doing so, we sacrifice some of the noise immunity and out-band signal rejection which caused us to use a large filter in the first place. We must also accept a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specified the device bandwidth) a lower value of low pass capacitor automatically increases the bandwidth. We gain speed
only at the expense of added bandwidth. c. Loop damping-Loop damping for a simple time constant low pass filter is:
(Equation 9-22)


Damping can be increased not only by reducing $\tau$, as discussed above, but also by reducing the loop gain $\mathrm{K}_{\mathrm{v}}$. By using the loop gain reduction to control bandwidth or capture and lock range, we achieve better damping for narrow bandwidth operation. The penalty for this damping is that more phase detector output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.
d. Input frequency deviation from freerunning frequency-Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.
e. In-band input amplitude-Since input amplitude is one factor in the phase detector gain $K_{d}$ and since $K_{d}$ is a factor in the loop gain $K_{v}$, damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low pass capacitor can charge with the
reduced phase detector output (see d above).
f. Out-band signals and noise-Low levels of extraneous signals and noise have very little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.
g. Center frequency-Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies on the average will be detected before the lower frequencies. However, because of the wide variation due to initial phase, the reverse may be true for any single trial

## PLL MEASUREMENT TECHNIQUES

This section deals with user measurements of PLL operation. The techniques suggested are meant to help the user in evaluating the performance of his PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the user's test equipment may be limited, we have stressed the techniques which require a minimum of standard test items.

## Center Frequency

Center frequency measurements are easily


Figure 9-13
made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass and low pass filter capacitors. No input signal should be present. As the center frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor unless the capacity added by the measurement probe is much less than the timing capacitor value since the probe capacity will then cause a frequency error.
When the frequency measurement is to be converted to a dc voltage for production readout or automated testing, a calibrated phase locked loop can be used as a frequency meter (see Applications Section).

## Capture and Lock Range

Figure 9-14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at lower frequencies) $X-Y$ recorder. The sweep voltage is applied to the $X$ axis.
Figure 9-14b shows the type of trace which results. The lock range (also called hold-in or tracking range) is given by the outer lines on the trace, which are formed as the incoming frequency sweeps away from the center frequency. The inner trace, formed as the frequency sweeps toward the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope $(\Delta f / \Delta \mathrm{V})$ is the gain or conversion factor for the VCO
By using the sweep technique, the effect on center frequency, capture range and lock range of the input amplitude, supply voltage, low pass filter and temperature can be examined.
Because of the lock-up time duration and variation, the sweep frequency must be very much lower than the center frequency, especially when the capture range is below $10 \%$ of center frequency. Otherwise, the apparent capture and lock range will be a function of sweep frequency. It is best to start sweeping as slow as possible and, if desired, increase the rate until capture range begins to show an apparent reduction-indicating that the sweep is too fast. Typical sweep frequencies are in the range of $1 / 1000$ to $1 / 100,000$ of the center frequency. In the case of the 561 and 567, the quadrature detector output may be similarly displayed on the $Y$ axis, as shown in Figure 9-15, showing the output level

## CAPTURE AND LOCK RANGE MEASUREMENT SETUP



Figure 9-14a

CAPTURE AND LOCK RANGE OSCILLOGRAM


Figure 9-14b
versus frequency for one value of input amplitude.

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the dc voltage at the low pass filter or the ac beat frequency components at the low pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

## FM and AM Demodulation Distortion

These measurements are quite straightforward. The loop is simply setup for FM or AM (561 or 567) detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP 333A) can be used to measure distortion at the FM or AM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attentuates the sum


Figure 9-15
frequency component of the phase detector output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured. The same comment applies to the measurement of AM distortion on the 561.

When AM distortion is being measured, the carrier frequency offset becomes more important. The lowest absolute value of carrier voltage at the modulation valleys must be high enough to maintain lock at the frequency deviation present. Otherwise, lock will periodically be lost and the distortion will be unreasonable. For example, the typical tracking range as a function of input signal graph in the 561 data sheet gives a total $3 \%$ tracking range at 0.3 mVrms input. Thus, for a carrier deviation of $1.5 \%$, the carrier must not drop below 0.3 Vrms in the modulation valleys. Naturally, the AM amplitude must not be too high or the AM information will be suppressed.

## Natural Frequency ( $\omega_{\mathrm{n}}$ )

Expressions for the natural frequency in terms of the loop gains and filter parameters are given in Table 9-2.

## Expressions for $\omega_{\boldsymbol{n}}$ and $\zeta$ in Second Order Loop

The natural frequency ( $\omega_{n}$ ) of a loop in its final circuit configuration can be measured by applying a frequency modulated signal of the desired amplitude to the loop (Table $9-2$ shows that the natural frequency is a function of $K_{d}$, in turn a function of input amplitude). As the modulation frequency $\left(\omega_{\mathrm{m}}\right)$ is increased, the phase relationship between the modulation and recovered sine wave will go through $90^{\circ}$ at $S_{m}=\omega_{n}$ and the output amplitude will peak.

## Damping ( $\zeta$ )

As shown in Table 9-2 in the discussion on low pass filter, damping is a function of $\mathrm{K}_{\mathrm{o}}$, $K_{d}$ and the low pass filter. Since $K_{o}$ and $k_{d}$ are
functions of center frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency modulated within the lock range by a square wave. The low pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 9-16. Figure 9-17 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 9-18, which gives the transient phase error due to a step in input frequency.
Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency ( $\omega_{n}$ ) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB-down point will give the damping. Table 9-3 gives the approximate relationship.

## EXPRESSIONS FOR $\omega_{n}$ and $\zeta$ IN SECOND ORDER LOOP



Table 9-2

MEASUREMENT SETUP FOR DISPLAY OF LOOP TRANSIENT RESPONSE


Figure 9-16


UNDERDAMPED $\zeta \approx .5$

$\left[C_{\text {ext }}>C_{\text {crit, }} R_{\text {ext }}=0\right]$
Figure 9-17a

OVERDAMPED $\zeta \approx 10$

$\left[C_{\text {ext }}<C_{\text {crit, }} R_{\text {ext }}>0\right] \quad$ Figure 9-17c
Figure 9-17d

## ESTIMATING DAMPING FROM

 MODULATING FREQUENCY ( $\omega \mathrm{m}$ ) RESPONSE|  | PEAK AMPLITUDE <br> LOW FREQUENCY <br> AMPLITUDE | $\frac{\omega-3 \mathrm{~dB}}{\omega \mathrm{n}}$ |
| :---: | :---: | :---: |
| $\zeta$ | 6.0 dB | 1.8 |
| .3 | 3.2 dB | 2.1 |
| .5 | 2.2 dB | 2.5 |
| .7 | 1.3 dB | 4.3 |
| 1.0 | .5 dB | 10 |
| 5.0 |  |  |

## TRANSIENT PHASE ERROR AS

 AN INDICATION OF DAMPING

Figure 9-18

Table 9-3

## Noise Effects

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the $\pm 90^{\circ}$ permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

## Simplified Measurement Equipment

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have
these. A low-cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. (See the applications in this section.) Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to dc, the calibration may be done in steps. Moreover, Gardner* shows how loop measurements may be made by applying a constant frequency to the loop input and the modulating signal to the low pass filter terminal to simulate the effect of a FM input so that a FM generator may be omitted for many measurements.
*See references

## SIGNETICS MONOLITHIC PHASE LOCKED LOOPS

## Detailed Description of 560N, 561 N and $562 \mathrm{~N}, 564 \mathrm{~N}$

The $560 \mathrm{~N}, 561 \mathrm{~N}$ and 562 N phase locked loops are all derived from the same monolithic die with different metal interconnections. Each device contains the same VCO, phase detector and voltage regulator stage and, hence, the basic loop parameters are the same for all three circuits.

The 560 N is the most fundamental of the three circuits, having a block diagram equivalent to that shown in Figure 9-1. The actual circuit diagram is shown in Figure 919.

The VCO is a high frequency emittercoupled multivibrator formed by transistors Q11-Q14. It operates from a regulated 7.7V supply formed by 6.3 V supply formed by Zener diode CR1 (a reverse-biased baseemitter junction) in series with the 14 V regulated supply. The VCO frequency is thus immune from supply voltages variations. Four constant current sources formed by Q20, Q21, Q23, Q24, and biased by CR6 and CR7. supply operating current for the VCO. Voltage control of the frequency is achieved by a differential amplifier, Q22 and Q25. As the base voltage of Q22 increases with respect to the base voltage of Q25, additional current is supplied to the emitters of Q12 and Q13, increasing the charge and discharge current of the timing capacitor $\mathrm{C}_{0}$, increasing the VCO frequency. Reducing the base voltage of Q22 with respect to Q25 similarly reduces the VCO frequency. Two Zener diodes and two transistors, CR4, CR5, Q5 and Q10, respectively, provide level shifting which allows the VCO to be driven by the outputs of the phase detector.

The phase detector is a doubly-balanced multiplier formed by transistors Q6-Q9, Q17 and Q18. Signal input is made to the lower stage, biased at about 4 V by means of $2 \mathrm{k} \Omega$ base resistors. The upper stage is biased and driven directly by the VCO output taken from the collector resistors of Q12 and Q13. A differential output signal is available between the collectors of Q6 (and Q8) and Q7 (and Q9). An external network, together with the 6 k collector resistors, comprises the low pass filter. The phase detector is operated from regulated 14 V appearing at the emitter of Q27. A resistor in the collector of Q25 can be shunted with an external capacitor to

SCHEMATIC DIAGRAM OF 560N


Figure 9-19
form a de-emphasis filter. The deemphasized signal is buffered by emitter follower Q19 before being brought out.
The Track Range input, pin 7 on all three loops, allows the user to control the total current flowing through the frequency controlling differential amplifier Q22, Q25. This is done by controlling effective emitter resistance of Q29, the current source for Q22, Q25. Current may be added or subtracted at pin 7 to, respectively, reduce or increase the tracking range.

The 561, shown in Figure 9-20, contains all of the circuitry of the 560 and in addition, has a quadrature phase comparator. This enables it to be used as a synchronous AM detector. The quadrature phase detector consists of transistors Q1-Q4 and Q15, Q16 which are biased and driven in the same manner as the loop phase detector. However, the quadrature detector input is single ended rather than differential (as the loop
phase detector input) and the external $90^{\circ}$ phase shift network is required to provide the proper phase relations. The demodulated AM output is brought out at pin 1.

The 562, shown in Figure 9-21, is basically the same as the 560 except that the loop is broken between the VCO and phase comparator. This allows a counter to be inserted in the loop for frequency multiplication applications. Transistors Q1-Q4 provide low impedance differential VCO outputs (pins 3 and 4), and the upper stage phase detector inputs are brought out of the package (pins 2 and 15). A bias voltage is brought out through pin 1 to provide a convenient bias level for the upper stage of the phase detector.

## Interfacing

Connection of the Signetics 560 N and 561 N phase locked loops to external input and
output circuitry is readily accomplished; however, as with any electrical system, there are voltage, current and impedance limitations that must be considered.

The inputs of the phase comparators in the $560 \mathrm{~N}, 561 \mathrm{~N}$ and 562 N and the AM detector in the 561 N are biased internally from a +4 volt supply; therefore, the input signals must be capacitively coupled to the PLL to avoid interfering with this bias. These coupling capacitors should be selected to give negligible phase shift at the input frequency and impedance of the PLL. (The capacitive impedance at the operating frequency should be as small as possible, compared to the input resistance of the PLL.)
The input resistance of the phase comparator is $2000 \Omega$ single-ended, and $4000 \Omega$ when differentially connected. The input resistance of the AM detector is $3000 \Omega$. The signal input to the phase comparator may be ap-

## SCHEMATIC DIAGRAM OF 561N



Figure 9-20
plied differentially if there is a common mode noise problem; however, in most applications, a single-ended input will be satisfactory. When inputs are not used differentially, the unused input may be accoupled to ground to double the phase detector gain at low input amplitudes.
The amplitude of the input signal should beadjusted to give optimum results with the PLL. Signals of less than 0.2 mVrms may have an unsatisfactory signal-to-noise ratio; signals exceeding 25 mVrms will have reduced AM rejection (less than 30 dB ). The AM detector will handle input signals up to 200 mV peak-to-peak without excessive distortion, and will handle up to 2 V peak-topeak where distortion is not a factor.
Interfacing of the available outputs is best described by referring to the following diagrams. Figure 9-22 shows the PLL VCO output as a clock circuit for logic pulse synchronization. Figures 9-22a and 9-22b show the 560 N and 561 N , respectively, connected directly to the clock circuit; however,
this configuration may be limited by low voltage and the possibility of too large a capacitive load swamping the oscillator. Figures 9-22c and 9-22d show the PLL clock output for the 560 N and 561 N , respectively, using the $\mu$ A710 Voltage Comparator as a buffer amplifier to provide an output voltage swing suitable for driving logic circuits. The power supply for circuits utilizing the $\mu$ A710 is split ( +12 and -6 V dc ).

In Figure 9-23a the 560N is a FM demodulator used for the detection of audio information on frequency modulated carriers. Since the lower frequency limit of this type of information is approximately 1 Hz , capacitive coupling may be used. However, in some applications where carrier shifts occur at an extremely slow rate, direct coupling from the output to load is necessary. Figure $9-23 \mathrm{~b}$ shows an alternative FM detector output configuration which should be used if a different output is desirable. In this case, the output is removed at pins 14 and 15 . These pins are the terminals of the
low pass filter and are in the line containing the demodulated signal. The signal level (single-ended) is about one-sixth of that at pin 9 so that additional amplification may be required.

Additional receiving modes are illustrated in Figure 9-24 for the 561 N only. Figure 9-24a shows the 561 N output when used as an AM detector; note the straight capacitive coupling. Figure 9-24b shows the 561 N used as a continuous wave detector. Since this version of the circuit is for the detection of CW or AM signals, external circuitry must be incorporated for use with CW inputs. With a CW input applied, there will be a dc shift at the output of the AM detector, pin 1. This shift is small compared to the no signal dc level and may be difficult to detect in relation to power supply voltage changes. Therefore, a reference must be generated to track any power supply voltage variations and to compensate for internal PLL thermal drift. This is best accompanied by simulating a portion of the PLL internal structure.

SCHEMATIC DIAGRAM OF 562N


Figure 9-21

The 2N3565 npn transistor is used as a constant-current source. Its reference voltage is obtained from an internal PLL bias source at pins 12 and 13 , with the current level established by the 6.8 k resistor. The 6.2 k resistor and the 2.5 k potentiometer simulate the PLL output resistance. The differential amplifier, composed of two 2N3638 pnp transistors, amplifies the dc output and allows it to drive a npn transistor referenced to ground. This type of circuit may also be used as a tone detector or to sense that the PLL is locked to an incoming signal.
The 562 phase locked loop is especially designed for utilizing the output of the VCO. In this configuration, an amplifier-buffer has been added to the VCO to provide differential square wave outputs with a 4.5 V
amplitude (see block diagram Figure 9-25). This facilitates the utilization of the frequency stabilized VCO as a timing or clocking signal. The outputs (pins 3 and 4) are emitter-followers and have no internal load resistors; therefore, external $3 k$ to $12 k \Omega$ load resistors are required.
It is essential that the resistance from each pin to ground be equal in order to maintain output waveform symmetry and to minimize frequency drift. When locking the VCO output to the phase comparator (pins 3 to 2 for single-ended connection), capacitive coupling should be used. If a signal exceeding 2 V is to be applied, a $1 \mathrm{k} \Omega$ resistor should be placed in series with the coupling capacitor. This resistor may be part of the load resistance of $12 \mathrm{k} \Omega$, by using two resistors ( 1 k and 11 k ) to form the VCO load, as shown in

Figure 9-26.
The output from the VCO is a minimum of $3 V$ peak-to-peak, but has an average level of 12 Vdc ; that is, it oscillates from 10.5 to 13.5 V . To utilize this output with logic circuits, some means of voltage level shifting must be used. Figures 9-27 and 9-28 show two methods of accomplishing level shifting. These circuits will operate satisfactorily to 20 MHz .

The phase comparator inputs of the 562 N (pins 2 and 15) must be biased by connecting a $1 \mathrm{k} \Omega$ resistor from each pin to the 8 V bias supply available at pin 1 . Pin 1 should be capacitively bypassed to ground. The inputs to the phase comparator should be capacitively coupled.


## FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The equivalent circuit of the NE564 is shown in Figure 9-28a. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to 50 MHz . In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.
The output voltage of the PLL can be written as shown in the following equation:
(Equation 9-23)

$$
v_{o}=\frac{\left(f_{i n}-f_{0}\right)}{K_{v c o}}
$$

$\mathrm{K}_{\mathrm{vco}}=$ conversion gain of the VCO
$\mathrm{f}_{\mathrm{in}}=$ frequency of the input signal
$\mathrm{f}_{\mathrm{O}}=$ free running frequency of the VCO
The process of recovering FSK signals involves the conversion of the PLL output into digital, logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output due to the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 9-23 varies according to the frequency deviation of $f_{\text {in }}$ from $f_{0}$. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 9-23 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in fin itself may be less than the change in fo due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

## VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 - Q26 form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:
(Equation 9-24)

$$
\begin{aligned}
& f_{0}=\frac{1}{16 R_{c} C 1} \\
& R_{C}=R 19=R 20 \\
& C 1=\text { frequency setting external capacitor }
\end{aligned}
$$

Variation of $V_{d}$ changes the frequency of the oscillator. As indicated by Equation 9-24, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current $I_{R}$ with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

## Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied changing the current Q4 and Q15 which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

## Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.
As shown in the equivalent schematic, the dc retriever is formed by the transconductance amplifier Q42-Q43 with a capacitor at the output (pin 14). This forms an integrator whose output voltage is shown in the following equation:
(Equation 9-25)

$$
v_{0}=\frac{g m}{C 2} \int v_{\text {IN }} d t
$$

gm= transconductance of the amplifier C2 $=$ capacitor at the output (pin 14)
$\mathrm{V}_{\mathrm{IN}}=$ signal voltage at amplifier input
With proper selection of C 2 , the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q49 - Q50 with positive feedback being provided by Q47 - Q48. The hysteresis is varied by changing the current in Q52 with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

## Design Formula

Free running frequency of VCO is shown by the following equation:
(Equation 9-26)

$$
\begin{aligned}
f_{0} & =\frac{1}{16 R_{C} C 1} \text { in } \mathrm{Hz} \\
R_{\mathrm{C}} & =100 \Omega \\
\mathrm{C} 1 & =\text { external cap in farads }
\end{aligned}
$$

The loop filter diagram shown is explained by the following equation:
(Equation 9-27)

$$
\begin{gathered}
F(s)=\frac{1}{1+s R C 3} \\
R=R 12+R 13+1.3 k \Omega
\end{gathered}
$$

## LOOP FILTER



## FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5 V and 12 V are shown in Figures 9-29 and 9-30 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1\% or higher).

## FM DEMODULATOR WITH TTL COMPATIBLE OUTPUT SIGNAL

An FM demodulator with the output signal being a TTL signal can be obtained from the NE564 by connecting it as shown in Figure $9-31$. This operation requires the use of the dc retriever, the capacitance for which is connected at pin 14. The hysteresis of the Schmitt trigger can be adjusted by connecting a potentiometer at pin 15. The output signal appears at pin 16, which requires an external resistor. If necessary, the duty cycle of the output signal can be adjusted by applying a voltage at pin 14 (around 2.5 V ) and varying it. The connection for a similar application appears in Figure 9-32.


Figure 9-28a

## GATED PLL DEMODULATOR

The lock range adjust pin of the NE564 can be used to gate the PLL when it is operating in the demodulator mode. The circuit is connected as shown in Figure 9-33. The gating voltage which can be a TTL signal is applied to pin 2 . When this voltage is high, the loop is in lock and the demodulated output signal appears at pin 16. When the input to pin 2 is low, the loop is out of lock and the VCO will be at its center frequency. It is also possible to use pin 2 to adjust the loop gain so that a large capture range and small lock range can be obtained.

## MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in Figure 9-34. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 9-35. This curve will be appropriate for signals injected into pins 4 and 5 .

## FREQUENCY SYNTHESIS

Frequency multiplication can be achieved with the NE564 with the insertion of a counter (digital frequency divider) in the loop.

A block diagram is shown in Figure 9-36 and the associated performance characteristic curve in Figure 9-35. Here the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input frequency so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property is the use of the NE564 in wide range frequency synthesizers.


Figure 9-29


Figure 9-31




In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency component is dc and is the error voltage which drives the VCO to keep the NE564 in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency


Figure 9-36
component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to
remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.

## DETAILED DESCRIPTION OF 565

The 565 is a general purpose PLL designed to operate at frequencies below 1 MHz . Functionally, the circuit is similar to the 562 in that the loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565 , it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.

The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagram of the VCO is shown in Figure 9-37. $I_{1}$ is the charging current created by the application of the control voltage $\mathrm{V}_{\mathrm{c}}$. In the initial state, Q3 is off and the current $\mathrm{I}_{1}$ charges capacitor C1 through the diode D2. When the voltage on C1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q3. This provides a current sink and
essentially grounds the emitters of Q1 and Q2 to become reverse biased. The charging current $\mathrm{I}_{1}$ now flows through D1, Q1 and Q3 to ground. Since the base-emitter voltage of Q2 is the same as that of Q1, an equal current flows through Q2. This discharges the capacitor C1 until the lower triggering threshold is reached at which point the cycle repeats itself. Because the capacitor C1 is charged and discharged with the constant current $\mathrm{I}_{1}$, the VCO produces a triangle wave form as well as the square wave output of the Schmitt trigger.
The actual circuit is shown in Figure 9-38. Transistors Q1-Q7 and diodes D1-D3 form the precision current source. The base of Q1 is the control voltage input to the VCO. This voltage is transferred to pin 8 where it is applied across the external resistor R1. This develops a current through R1 which enters pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q1 base current, all the current that enters pin 8, appears at the anodes of diodes D2 and D3. When Q8 (controlled by the Schmitt trigger) is on, D3 is reverse biased and all the current flows through D2 to the duplicating current source Q5-Q7, R2-R3 and appears as the capacitor discharge current at the collector of Q5. When Q8 is off, the duplicating current source Q5-Q7,

## SIMPLIFIED DIAGRAM OF 565 VCO



Figure 9-37
R2-R3 floats and the charging current passes through D3 to charge C1.

The Schmitt trigger (Q11, Q12) is driven from the capacitor triangle wave form by the emitter follower Q9. Diodes D6-D9 prevent saturation of Q11 and Q12, enhancing the switching speed. The Schmitt trigger output

SCHEMATIC DIAGRAM OF 565


Figure 9-38
is buffered by emitter follower Q13 and is brought out to pin 4, and is also connected back to the current source by the differential amplifier (Q14-Q16).

When operated from dual symmetrical supplies, the square wave on pin 4 will swing between a low level of slightly ( 0.2 V ) below ground to a high level of one diode voltage drop ( 0.7 V ) below positive supply. The triangle wave form on pin 9 is approximately centered between positive and negative supply and has an amplitude of 2 V with supply voltages of $\pm 5 \mathrm{~V}$. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase detector is again of the doublybalanced modulator type. Transistors Q20 and Q24 form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q20 and Q24 through external resistors to ground. The switching stage Q18, Q19, Q22 and Q23 is driven from the Schmitt trigger via pin 5 and D11. Diodes D12 and D13 limit the phase detector output, and differential amplifier Q26 and Q27 provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to pin 7) and the collector resistance R24 (typically $3.6 \mathrm{k} \Omega$ ). The voltage on pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is normally equal to the output voltage on pin 7. This allows differential stages to be both biased and driven by connecting them to pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R1 and C1 and is given approximately by
(Equation 9-28)

$$
f_{0} \simeq \frac{1.2}{4 R 1 C 1}
$$

When the phase comparator is in the limiting mode (Vin $\geq 200 \mathrm{mVp}$-p), the lock range can be calculated from the expression:
(Equation 9-29)

$$
2 \omega \mathrm{~L}=2 \mathrm{~K}_{0} \mathrm{~K}_{\mathrm{d}} \mathrm{~A} \theta_{\mathrm{d}}
$$

where $K_{0}$ is the VCO conversion gain, $K_{d}$ is the phase detector gain factor, $A$ is the amplifier gain and $\theta_{\mathrm{d}}$ is the maximum phase error over which the loop can remain in lock
(Equation 9-30)

$$
\mathrm{K}_{\mathrm{o}}=\frac{50 \mathrm{f}_{\mathrm{o}}}{\mathrm{~V}_{\mathrm{cc}}} \text { radians } / \mathrm{sec} / \mathrm{volt}
$$

(where $f_{0}$ is the free-running frequency of the VCO and $V_{c c}$ is the total supply voltage applied to the circuit.)
(Equation 9-31)

$$
\begin{aligned}
& \mathrm{K}_{\mathrm{d}}=\frac{1.4}{\pi} \text { volts } / \text { radian } \\
& \mathrm{A}=1.4 \\
& \theta_{\mathrm{d}}=\frac{\pi}{2} \text { radians }
\end{aligned}
$$

The lock range for the 565 then becomes:
(Equation 9-32)

$$
\mathrm{fL}_{\mathrm{L}} \cong \frac{\omega \mathrm{~L}}{2 \pi} \cong \frac{8 \mathrm{f}_{\mathrm{o}}}{\mathrm{~V}_{\mathrm{CC}}} \mathrm{~Hz}
$$

to each side of the center frequency, or a total range of:
(Equation 9-33)

$$
2 f_{L} \cong \frac{16 f_{\mathrm{o}}}{V_{c c}} \mathrm{~Hz}
$$

The capture range, over which the loop can acquire lock with the input signal is given approximately by:
(Equation 9-34)

$$
2 \omega_{C} \cong 2 \sqrt{\frac{\omega L}{\tau}}
$$

where $\omega \mathrm{L}$ is the one-sided lock range

$$
\omega L=2 \pi f_{L}
$$

and $\tau$ is the time constant of the loop filter

$$
\tau=\mathrm{RC}_{2}
$$

with $R=3.6 \mathrm{~K} \Omega$.
This can be written as:
(Equation 9-35)

$$
\mathrm{f}_{\mathrm{C}} \cong \pm \frac{1}{2 \pi} \sqrt{\frac{2 \pi f_{\mathrm{L}}}{\tau}}= \pm \frac{1}{2 \pi} \sqrt{\frac{32 \pi \mathrm{f}_{\mathrm{o}}}{\mathrm{~V}_{\mathrm{cc} \tau}}}
$$

to each side of the center frequency of a total capture range of:

$$
\mathrm{fc}_{\mathrm{C}} \cong \frac{1}{\pi} \sqrt{\frac{32 \pi \mathrm{fo}^{\prime}}{\tau \mathrm{V} \mathrm{Cc}}}
$$

(Equation 9-36)

This approximation works well for narrow capture ranges ( $f_{C}=1 / 3 f_{L}$ ) but becomes too large as the limiting case is approached ( $\mathrm{f}_{\mathrm{C}}=$ fL).

## DETAILED DESCRIPTION OF 566

The 566 is the voltage controlled oscillator portion of the 565. The basic die is the same as that of the 565 ; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 9-39. Transistor Q18 has been a buffered triangle waveform output. (The triangle waveform is available at capacitor C1 also, but any current drawn from pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q19 by pin 4. The circuit will operate at frequencies up to 1 MHz and may be programmed by the voltage applied on the control terminal (pin 5), current injected into pin 6 or the value of the external resistor and capacitor (R1 and C1).

## DETAILED DESCRIPTION OF 567

The 567 is a PLL designed specifically for frequency sensing or tone decoding. Like the 561, the 567 has a controlled oscillator, a phase detector and a second auxiliary or quadrature phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature phase detector output. During lock, the quadrature phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder center frequency and bandwidth are specified by the center frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range.

The current controlled oscillator is shown in simplified form in Figure 9-40. It provides both a square wave output and a quadrature output. The control current $I_{c}$ sweeps the oscillator $\pm 7 \%$ of the center frequency, which is set by external components R1 and C1. It operates as follows:

Transistors Q1 through Q6 form a flip-flop which can switch pin 5 between $V_{\text {be }}$ and $V+-$ $V_{b e}$. Thus, the R1C1 network is driven from a square wave of $V+-2 V_{\text {be }}$ peak-to-peak volts. On the positive portion of the square wave, $C 1$ is charged through $R 1$ until $V_{1}$ is reached. A comparator circuit driven from C1 at pin 6 then supplies a pulse which resets the flip-flop so that pin 5 switches to $\mathrm{V}_{\text {be }}$ and C 1 is discharged until $\mathrm{V}_{2}$ is reached. A second comparator then supplies a pulse which sets the flip-flop and C1 resumes charging.

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is
(Equation 9-37)
$\mathrm{V}_{1}-\mathrm{V}_{2}=\left(\mathrm{V}+-2 \mathrm{~V}_{\mathrm{be}}\right) \frac{\mathrm{R} 22+\mathrm{R} 23}{\mathrm{R} 21+\mathrm{R} 22+\mathrm{R} 23+\mathrm{R} 23+\mathrm{R} 24}$
$=K\left(V+-2 V_{b e}\right)$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 9-41 shows the pin 5 and pin 6 voltages during operation. It is obvious from the proportion that $t_{1}+t_{2}$ is independent of the magnitude of $\mathrm{V}^{+}$and dependent only on the time constant R1C1 of the external components. Moreover, if $\left(\mathrm{V}_{1}\right.$ $\left.+\mathrm{V}_{2}\right) / 2=\mathrm{V}+/ 2$, then $\mathrm{t}_{1}=\mathrm{t}_{2}$ and the duty cycle is $50 \%$. Note that the triangular waveform is phase shifted from the square wave. A differential stage (Q22 and Q23) amplifies


Figure 9-39
the triangular wave with respect to $\left(\mathrm{V}_{1}\right.$ and $\mathrm{V}_{2}$ )/2 to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase shifted about $80^{\circ}$, but no operating compromises result from this slight deviation from true quadrature.)

One source of error in this oscillator scheme is current drawn by the comparators from the R1C1 mode. An emitter follower, therefore, is inserted at $X$ to minimize this drain and Q21 placed in series with Q20 to drop the comparator sensing voltage one $\mathrm{V}_{\text {be }}$ to compensate for the $V_{b e}$ drop in the emitter follower.

## LOOP GAIN CONSTANTS (Ko, $K_{d}$ )

Table 9-4 gives the gain constants ( $\mathrm{K}_{\mathrm{o}}, \mathrm{K}_{\mathrm{d}}$ ) for the Signetics' loops. The values given are for the standard connection with no gain reduction or tracking adjustment components connected. The dc amplifier gain $A$ has been included in either the $\mathrm{K}_{0}$ or $\mathrm{K}_{\mathrm{d}}$ value, depending on which side of the low pass filter terminals the gain is present. This


causes no hardship in calculations since the loop gain $\mathrm{K}_{\mathrm{v}}$ becomes simply $\mathrm{K}_{0} \mathrm{~K}_{\mathrm{d}}$.
In order to insure that the square wave drops quickly and accurately to $V_{b e}$, an active clamp scheme is applied to the collector of Q2. The base of Q9 is held at $2 V_{b e}$ so that as Q2 is turned on by its base current, its collector is held at $\mathrm{V}_{\mathrm{be}}$. Because Q2 and Q3 have the same geometry and their base-emitter voltages are the same, the maximum Q2 current when clamped is essentially the same as the collector current of Q3 (as limited by R5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.
Current control of the frequency is achieved by making R21 somewhat less than R24 and restoring the proper voltage for $50 \%$ duty cycle by drawing $\mathrm{I}_{\mathrm{c}}$ of $100 \mu \mathrm{~A}$ for the R21, Q20 junction. When $I_{c}$ is then varied be-
tween 0 and $200 \mu \mathrm{~A}$, the frequency changes by $\pm 7 \%$. Because of the slight shift in the voltage levels $\mathrm{V}_{1}$ and $\mathrm{V}_{2}$ with $\mathrm{I}_{\mathrm{c}}$, the square wave duty cycle changes from about $47 \%$ to about $53 \%$ over the control range. To avoid drift of center frequency with temperature and supply voltage changes when
$I_{c} \neq O, I_{C}$ is also made a function of $V+-2 V_{b e}$.
The CCO circuit is shown in the tone decoder schematic diagram, Figure 9-42.

A doubly-balanced multiplier formed by Q32 through Q37 (Figure 9-42) functions as the phase detector. The input signal is applied to the base of Q32. Transistors Q34Q37 are driven by a square wave taken from the CCO at the collector of Q2. Phase detector input bias is provided by three diodes, Q38 through Q40, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R26 and R27, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop dc amplifier is formed by Q51 and Q52. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full $\pm 7 \%$. Therefore, full detection bandwidth can be obtained for any inband input signal greater than about 70 mVrms . However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi / 2$ as possible
for all but the smallest input levels since this greatly facilitates operation of the quadrature lock detector. Emitter resistors R36 and R37 help to stabilize the gain over the required temperature range. Another function of the dc amplifier is to allow a higher impedance level at the low pass filter terminal (pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter resistors help stabilize the loop gain over the temperature range.

The quadrature phase detector (QPD), formed by a second doubly-balanced multiplier Q42-Q47, is driven from the quadrature output ( $E, F$, in Figure 9-47) of the CCO. The signal input comes from the emitters of the input transistors Q32 and Q33.
The output stage, Q53 through Q62, compares the average QPD current in the low pass output filter R3C3 with a temperature compensated current in R39 (forming the threshold voltage $V_{t}$ ).
Since R3 is slightly lower in value than R39, the output stage is normally off. When the lock and the QPD current $\mathrm{I}_{\mathrm{q}}$ occurs, pin 1 voltage drops below the threshold voltage $V_{t}$ and the output stage is energized.

The uncommitted collector (pin 8) of the power npn output transistor can drive both 100-200mA loads and logic elements, including TTL.

Table 9-4

| PLL GAIN CONSTANTS* $\mathbf{K}_{\mathbf{o}} \mathbf{K}_{\mathbf{d}}\left(\mathbf{K}_{\mathbf{v}}=\mathbf{K}_{\mathbf{o}} \mathbf{K}_{\mathbf{d}}\right)$ |  |  |  |
| :---: | :---: | :---: | :---: |
|  | 5608, 5618, 5828 | 565 |  |
| ${ }_{6}$ |  <br> $0.64 \omega \mathrm{o} \frac{\mathrm{rad}}{\text { sec-volt }} \begin{gathered}\text { Differential Input } \\ \text { to VCO }\end{gathered}$ | $\frac{8.0 \omega_{0}}{\text { Total Supply Votage }}$ $=0.67 \omega_{0} \frac{\mathrm{rad.}}{\text { sec.vot }}$ at $\pm 6$ volts | $0.44 \omega_{0} \sigma_{\text {sec.volt }}^{\text {rad }}$ |
| $\mathrm{k}_{\mathrm{d}}$ |  <br> m:x |  |  |

*The dc amplifier gain $A$ has been included in $K_{o}$ or $K_{d}$, depending on which side of the LPF terminals the amplifier is located.

SCHEMATIC DIAGRAM OF 567


Figure 9-42

## EXPANDING LOOP CAPABILITY

## Low Pass Filter Circuits (560N, 561N and 562N)

The low pass filters used with the 560 N , 561 N and 562 N are externally adjusted to provide the desired operational characteristics. To select the most appropriate type of filter and component values, a basic understanding of filter operation is required.
A FM signal to be demodulated is matched in the phase comparator with the voltage controlled oscillator signal, which is tuned to the FM center frequency. Any resulting phase difference between these two signals is the demodulated FM signal. This demodulated signal is normally at frequencies between dc and upper audio frequencies.
The choice of low pass filter response gives a degree of design freedom in determining
the capture range or selectivity of the loop. The attenuation of the high frequency error components at the output of the phase detector enhances the interference rejection characteristics of the loop. The filter also provides a short-term memory for the PLL that ensures rapid recapture of the signal if the system is thrown out of lock due to noise transient.

To ensure absolute closed loop stability at all signal levels within the dynamic range of the loop, the open loop PLL is required to have no more than 12 dB per octave high frequency roll-off.
The capacitor in each filter circuit shown in Figure 9-43 will provide 6 dB per octave rolloff at the first break point-the desired bandwidth frequency. The resistor $R_{x}$ shown in filters (c) and (d) is used to break the response up at high frequencies to
ensure 6 dB per octave roll-off at the loop unity gain frequency. $R_{x}$ is typically between 50 and $200 \Omega$.

Calculations of values for low pass filters shown can be made using the complex second-degree transfer function equations given, or approximated using the equation:
(Equation 9-38)
$\mathrm{C} 1=\frac{26.60}{\mathrm{f}}$ mfd for filters $(\mathrm{a})$ and $(\mathrm{c})$, and the equation:
$C 1=\frac{13.30}{f}$ mfd for filters (b) and (d) where $f$ is the desired first break frequency in Hz .
At frequencies greater than 5 MHz where the loop may be prone to instability, filters (C) and (D) should be used. For operation at low frequencies, a simple type (b) lag filter with no added resistance is usually sufficient.


Figure 9-43


## Operating Frequency Extension to $60 \mathrm{MHz}(560 \mathrm{~N}, 561 \mathrm{~N}, 562 \mathrm{~N})$

The frequency range of the $560 \mathrm{~N}, 561 \mathrm{~N}$ and 562 N phase locked loops may be extended to 60 MHz by the addition of two $10 \mathrm{k} \Omega$ resistors from the timing capacitor terminals to the negative power supply as shown in Figure 9-44. The inclusion of a $5 \mathrm{k} \Omega$ potentiometer between these $10 \mathrm{k} \Omega$ resistors and the negative supply provides a simple method of fine tuning.

## Increased Loop Output Voltage <br> For Small Frequency Deviations (565)

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into pin 8 and increase the value of R1. One scheme for this is shown in Figure $9-45$. The basis for this scheme is the fact that the output voltage controls only the current through R1 while the current through Q1 remains constant. Thus, if most of the charging current is due to Q1, the total current can be varied only a small amount due to the small change in current through R1. Consequently, the VCO can track the input signal over a small frequency range yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

Diode D1 is a Zener diode, used to allow a larger voltage drop across $\mathrm{R}_{\mathrm{A}}$ than would otherwise be available. D4 is a diode which should be matched to the emitter-base junction of Q1 for temperature stability. In addition, D1 and D2 should have the same breakdown voltages and D3 and D4 should be similar so that the voltage seen across $\mathrm{R}_{\mathrm{B}}$ and $R_{C}$ is the same as that seen across pins 10 and 1 of the phased locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The center frequency can be found by:
(Equation 9-39)

$$
f_{0} \simeq \frac{2 R_{B}}{\left(R_{B}+R_{C}\right) R_{A} C 1}+\frac{1}{4 R 1 C 1} \mathrm{~Hz}
$$

and the total lock range is given by:
(Equation 9-40)
$2 \Delta f_{L} \simeq \frac{22.4 V_{D}\left(R_{B}+R_{C}\right) R_{A} f_{0}}{\left(\left|V_{1}\right|+\left|V_{2}\right|-V_{Z}-V_{D}\right)\left(8 R_{B} R_{1}+R_{A}\left[R_{B}+R_{C}\right]\right)} H z$ where:
$V_{D}=$ forward biased diode voltage $\approx 0.7 \mathrm{~V}$
$\mathrm{V}_{\mathrm{z}}=$ Zener diode breakdown voltage
$\mathrm{V}_{1}=$ positive supply voltage
$\mathrm{V}_{2}=$ negative supply voltage
$\mathrm{f}_{0}=$ free-running VCO center frequency
When the output excursion at pin 7 need be only a volt or so, diodes D1, D2 and D3 may be replaced by short circuits.

The value of R1 can be selected to give a prescribed output voltage for a given frequency deviation.
(Equation 9-41)

$$
R 1=\frac{R_{A}\left(R_{B}+R_{C}\right) f_{0}}{R_{B}\left(\left|V_{1}\right|+\left|V_{2}\right|-0.7\right) \Delta f}
$$

where $f_{o}$ is the center frequency and $\Delta f$ is the desired frequency deviation per volt of output.

In most instances, $\mathrm{R}_{\mathrm{B}}$ and $\mathrm{R}_{\mathrm{A}}$ are chosen to be equal so that the voltage drop across them is about 200 mV . For the best temperature stability, diode D1 should be a basecollector shorted transistor of the same type as Q1.

## Expanded Lock Range (565)

When the 565 is connected normally, feedback to the VCO from the phase detector is internal. That is, an amplifier makes the pin 8 voltage track the pin 7 (phase detector output) voltage. Since the capacitor C1 charge current is determined by the current through resistance R1, the frequency is a function of the voltage at pin 8 . It is possible, however, to bypass and swamp the internal loop amplifier so that the current into pin 8 is no longer a function of the pin 8 voltage but only of the pin 7 voltage. This makes a greater charge-discharge current variation possible, allowing a greater lock range. Figure 9-46 shows such a circuit in which the $\mu$ A741 operational amplifier is set for a differential gain of 5 , feeding current to pin 8 through the 33 k resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the user should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to $1500 \mu \mathrm{~A}$ which also specifies the pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

EXPANDED LOCK RANGE CONFIGURATION FOR 565


Figure 9-46

## INCREASED LOOP GAIN AND

 LOCK RANGE FOR 565

Figure 9-47

## Breaking the Internal Feedback Loop (565)

Many times it would be advantageous to be able to break the feedback connection between the output (pin 7) and the voltage control terminal (Q1) of the VCO. This can be easily done once it is seen that it is the current into pin 8 which controls the VCO frequency. If the external resistor R1 is replaced with a current source, such as in Figure 9-47, we have effectively broken the internal voltage feedback connection. The current flowing into pin 8 is now independent of the voltage on pin 8. The output voltage (on pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 947. This scheme allows the addition of enough gain for the loop to stay in lock over a 100:1 frequency range, or conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between $0^{\circ}$ and $180^{\circ}$. In addition, it is now possible to do special filtering to improve the performance in certain applications. For instance, in frequency multiplication applications it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

## Breaking the Internal Feedback Loop (560, 561, 562)

The internal control voltage feedback loop can also be easily broken on the 560, 561 and 562. The key in this case is to bias the range control terminal (pin 7 ) to +2 V which turns off the controlled current source. Now the phase comparator output voltage will
have no effect on the charging current which sets the VCO frequency: Now an external feedback loop can be built with the desired transfer function. Figure $9-48$ shows a practical application of this principle. The control voltage is taken from across the low pass filter terminals, amplified, and used to add or subtract current into the timing capacitor nodes.


## Minimizing Tone Decoder Response Time

The 567 Tone Decoder is a specialized loop which can be set up to respond to a given tone (constant frequency) within its bandwidth. The center frequency is set by a resistor R1 and capacitor C1 which determine the free-running frequency. The bandwidth is controlled by the low-pass filter capacitor C2. A third capacitor C3 integrates the output of the quadrature phase detector (QPD) so that the dc lockindicating component can switch the power output stage on when lock is present. The 567 is optimized for stability and predictability of center frequency and bandwidth.

Two events must occur before an output is given. First, the loop portion of the 567 must achieve lock. Second, the output capacitor C3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low pass filter. Thus, C2 must be as small as possible. However, C2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 9-49, reprinted from the 567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C2 and the input amplitude is 200 mV rms or greater. The response time is given in cycles of center frequency. For example, a $2 \%$ bandwidth at a center frequency of 1000 cycles can require as long as 280 cycles ( 280 ms ) to lock when the initial phase relationship is at its worst. Figure 950 gives a typical distribution of response time versus input phase. Note that, assuming random initial input phase, only 30/180 $=1 / 6$ of the time will the lock-up time be longer than half the worst case lock-up time. Figure 9-51 shows some actual measurements of lock-up time for a set-up having a worst case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.
The lower curve on the graph shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C2 required for this minimum response time is
(Equation 9-42)

$$
C^{\prime} 2=\frac{130}{f_{0}}\left[\frac{10 k-R_{A}}{R_{A}}\right] \mu F
$$



Figure 9-49


Figure 9-50

It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value (C2) of C2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect on the lock-up time-usually negligible in comparison to the variation caused by input phase.

Lock-up transients can be displayed on a two-channel scope with ease. Figure 9-52 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at pin 2 , the low
pass filter voltage. The input frequency is offset slightly from the center frequency so that the locked and unlocked voltage are different. It is apparent that, while the C2 decay during unlock is always the same, the lock transient is different each time. This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing so a favorable initial phase is created that is not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C2 or input
amplitude is seen. However, the repetition rate must be readjusted for worst-case lockup after each change.

Once lock is achieved, the quadrature phase detector output at pin 1 is integrated by C3 to extract the dc component. As C3 charges from its quiescent value $\mathrm{V}_{\mathrm{q}}$ (see Figure 9-53) to its final value $\left(V_{q}-\Delta V\right)$, it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted $\mathrm{V}_{\mathrm{q}}$ is very close (within 50 mV ) to $\mathrm{V}_{\mathrm{t}}$, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant ( $\tau=4700 \mathrm{C} 3$ ) expires before $V_{t}$ is crossed so that C3 does not greatly influence the response time. However, as shown in Figure 9-53a, the turn-off

## LOCK-UP TIME VARIATION DUE TO RANDOM INITIAL PHASE



Figure 9-51

TONE DECODER LOCK-UP TRANSIENT


Figure 9-52
delay time can be quite long when C3 is large. Figure $9-53 b$ shows how desensitizing the output stage by connecting a highvalue resistor between pin 1 and pin 4 (plus supply) can equalize the turn-on and turnoff time. If turn-off delay is important in the overall response time, then desensitizing can reduce the total delay.

But why not make C3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large twice-center-frequency component that must be filtered out. Also, noise, outband signals and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C 3 . What must be done, then, is to make C3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in smal steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:
a. After the center frequency has been set, adjust C 2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 9-51) suggests that worst-case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction. (See data sheet.)
b. Check lock-up time by observing the waveform at pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.
c. Starting with a large value of C3 (say 10 C2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.
d. Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.
e. Apply the chatter prevention technique to clean up the output.
If this procedure results in a worst-case

## EFFECT OF THRESHOLD VOLTAGE (Vt) ADJUSTMENT ON THE TONE DECODER TURN-ON AND TURN-OFF DELAY



Figure 9-53a


Figure 9-53b
response time that is too slow, the following suggestions may be considered:
a. Relax the bandwidth requirement.
b. Operate the entire system at higher frequency when this option is available.
c. Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurrence of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal $10 \%$ of the time with one unit, it will drop to $1 \%$ with two units.
d. Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.
$e$. If the system design permits, send the tone to be detected continuously at a low level (say 25 mVrms ) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing the signal ampli-
tude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as $1 / 3$ to $1 / 2$ the center frequency when C3 is small. This is equivalent to ASK (amplitude shift keying).

## FM IF Amplifier/Demodulator With Muting (561N)

In this application, the loop portion of the 561 N operates in the usual manner for FM demodulation. To introduce muting (squelch) the synchronous AM detector portion of the PLL is used to detect the presence of an input signal and to open a muting gate. Figure $9-54$ shows a typical circuit incorporating the muting feature.

The input section of the circuit is a broadband, amplifier-limiter. The tuned LC network at the AM input, pin 4, is adjusted to provide a $90^{\circ}$ phase shift at the IF frequency. This network is adjusted for maximum output at pin 1, demodulated AM output, with a carrier applied, at the IF frequency.
Three transistors at the right of the diagram (Q1, Q2 and Q3) and the 1N457 diode form

## TYPICAL FM IF AMPLIFIER/ DEMODULATOR WITH MUTING



* T1:20 Turns Biflar No. 36 Wire on 1/2-Watt Resistor Body (For 10.7 MHz )
** Part of NE510N

Figure 9-54
the muting gate. Gating is accomplished by applying the demodulated FM output through the 1N457 diode and by biasing the diode on and off as follows: During periods with no input applied, Q1 is shut off and Q2 conducts. Therefore, the diode is effectively back biased since its anode potential developed by the 10k resistors across the power supply is approximately +13.5 V . When an input is applied to the circuit, Q1 is turned on and Q2 shuts off, reducing its collector potential below 9 V . Thus, the diode is forward biased and the demodulated IF output is gated through to the circuit output.

Muting threshold adjustment is accomplished using the 2.5 k potentiometer. Transistor Q3 is used as a bias generator for the differential pair, Q1 and Q2. In turn, the bias of Q3 is obtained from internal PLL bias points at pins 12 and 13. Thus, the muting gate will track the PLL over wide temperature variations.

## FM Demodulator (560N)

When used as a FM demodulator, the 560 N phase locked loop requires selection of external components and/or circuits to create the desired response. The areas to be considered are:
a. Input signal conditioning
b. Tuning-VCO frequency
c. Low pass filter selection/gain adjustment
d. Output swing
e. Tracking range adjustment
f. De-emphasis network selection

Figure 9-55 illustrates schematically a typical FM demodulator with IF amplifier and limiter using the 560N PLL. The amplitude of the input signal has a pronounced effect on the operation. For the tracking range to be constant, the input signal level should be greater than 2 mVrms . In addition, AM rejection diminishes at higher signal levels and drops to less than 20 dB for signals greater than 30 mV . If either the tracking range or AM rejection is critical, the input signal should be conditioned to be in the 2 to 10 mV range, using either a limiter or a combination limiter-amplifier. This circuit should limit at the smallest input voltage that is expected.

The PLL is tuned by adjusting the VCO to the center frequency of the FM signal. This is accomplished by connecting a capacitor across pins 2 and 3 . The capacitor value is determined using the equation $\mathrm{C}_{0} \simeq 300 / f_{0}$, pF where $\mathrm{f}_{\mathrm{o}}$, the free-running VCO frequency , is in MHz . The exact value is not important as the internal resistors are only within $\pm 10 \%$ of nominal value and fine tuning is normally required. Fine tuning may be accomplished by using a trimmer capacitor in parallel with $\mathrm{C}_{0}$ or by using a potentiometer connected across the power supply with the
rotor connected to pin 6 through a $200 \Omega$ current limiting resistor.
The dc gain of the loop, which sets the lock range and threshold sensitivity, can be controlled by the placement of a resistance between pins 14 and 15, the low pass filter terminals. A low pass filter connected to these terminals controls the capture range or selectivity of the loop. In basic terms, it may be said that the low pass filter sets the bandwidth of the demodulated information which will be obtained. For most applications, a single capacitor connected between pins 14 and 15 will provide the required filtering. The capacitance value required can be approximated as follows:
(Equation 9-43)

$$
C \approx \frac{13.30}{f} \mathrm{mfd}
$$

where $f$ is the desired bandwidth in Hz . For example, if the desired information bandwidth is 15 kHz , the required low pass filter capacitance will be:
(Equation 9-44)

$$
C \approx \frac{13.30}{15000}=885 \mathrm{pF}
$$

TYPICAL FM DEMODULATOR WITH IF AMPLIFIER AND LIMITER USING THE 560N

**Part of NE501N

Figure 9-55

The output swing is a function of the frequency deviation of the incoming signal, and is approximately $0.3 \mathrm{Vp}-\mathrm{p}$ for $\pm 1 \%$ deviation. For example, a standard 10.7 MHz IF frequency has a deviation of $\pm 75 \mathrm{kHz}$; therefore, the percentage deviation equals

$$
\frac{ \pm 0.75 \times 100}{10.7}= \pm 0.7 \%
$$

and the output voltage will be

$$
0.3 \vee \mathrm{p}-\mathrm{p} \times \frac{.7 \%}{1 \%}=.21 \mathrm{~V} \text { p-p, }
$$

## or 74 mVrms for $100 \%$ modulation.

The de-emphasis network requires an external capacitor from pin 10 to ground. This capacitor $C_{d}$ and the $8000 \Omega$ internal resistance should produce a time constant of approximately $75 \mu$ s for standard FM broadcast demodulation. The value of the deemphasis capacitor for this application is determined by the following formula:

$$
C_{d}=\frac{75 \times 10^{-6}}{8000}=0.0094 \mathrm{mfd}
$$

For most applications, a 0.01 mfd value would be satisfactory since the manufacturing tolerance of the resistor is on the order of $20 \%$.

## Phase Locked AM Receiver (561N)

The Signetics 561 N can be used as an AM detector/receiver. AM detection is accomplished as illustrated in the block diagram of Figure 9-56a. The phase locked loop is locked to the signal carrier frequency and its VCO output is used to provide the local oscillator signal for the product detector or synchronous demodulator. The PLL locks to its input signal with a constant $90^{\circ}$ phase error. The amplitude of the signal at the output of the product detector is a function of the phase relationship of the carrier of the incoming signal and the local oscillator; it will be a maximum when the carrier and local oscillator are in phase or $180^{\circ}$ out of phase and a minimum when they are in quadrature. It is, therefore, necessary to add a $90^{\circ}$ phase shift network in the system to compensate for the normal PLL phase shift. The 561 is designed for this to be incorporated between the signal input and the input to the phase comparator input, pin 12 or pin 13.

Connection as an AM detector/receiver is given in Figure 9-56b. The bypass and coupling capacitors should be selected for low impedance at the operating frequency. $\mathrm{C}_{0}$ is selected to make the VCO oscillate at the frequency to be received and $C_{x}$ is selected, in conjunction with the output resistance ( $8000 \Omega$ ) and the load resistance, to roll off the audio output for the desired bandwidth.


The phase shift network may be determined from the following equations:
(Equation 9-45)

$$
C_{y}=\frac{1.3 \times 10^{-4}}{f_{c}} \mathrm{pF}
$$

where $f_{c}$ is the carrier frequency of the signal to be received and $R_{y}=3000 \Omega$. A receiver for standard AM reception is easily constructed using the circuit of Figure 956 b . Its operating range will be from 550 kHz to 1.6 MHz . All bypass and coupling capacitors are 0.1 mfd . $\mathrm{C}_{\mathrm{y}}$ is selected using a frequency which is the geometric mean of the limits of the frequencies which are to be received.

## PHASE LOCKED AM RECEIVER


$C_{B}=$ Bypass Capacitor
$\mathrm{C}_{\mathrm{C}}=$ Coupling Capacitor

Figure 9-56b

$$
\begin{aligned}
& \text { (Equ } \\
& f_{c}=\sqrt{f_{\text {niflo }}}=1.6 \times 0.55=.94 \mathrm{MHz} \\
& \text { then: } \\
& C_{y}=\frac{1.3 \times 10^{-4}}{.94 \times 10-6}=135 \mathrm{pF}
\end{aligned}
$$

The low pass filter for the loop, $C_{L}$, is not critical for no information is being derived directly from the loop error signal and one need only be assured of stable loop operation. A . 01 mfd capacitor was found to be adequate.
Tuning may be accomplished in several ways. The simplest method uses a variable capacitor as $C_{o}$. It should be trimmed so that when set for minimum capacitance, the VCO frequency is approximately 1.6 MHz . The capacitance used may be obtained from the following formula:

$$
C_{0} \approx \frac{300 p F}{f_{0}} \quad \text { where } f_{0} \text { is in } \mathrm{MHz}
$$

Application of this formula shows that the minimum capacitance should be about 180 pF and the maximum capacitance should be 550 pF . A second tuning method utilizes the fine tuning input, pin 6. When current is inserted or removed from this pin, the VCO frequency will change, thereby tuning the receiver. Select $C_{0}$, when the current at pin 6 is zero, to make the VCO operate at the mean frequency used in the phase shift network calculation $(940 \mathrm{kHz})$. The complete standard AM broadcast band may now be tuned with one potentiometer. The resistor in series with the arm of the potentiometer is selected to give the desired tuning range and will be about $1200 \Omega$ when an 18 V power supply is used.

For operation, this receiver requires an antenna and a good grounding system. Operation may be improved by including a broadband untuned RF amplifier, but care should be used to ensure that the phase locked loop is not overdriven, e.g. input signals should be kept less than 0.5 Vrms .

## IF STAGE WITH AGC AND AM/FM DETECTION (561N)

The circuit shown in Figure 9-57 is basically an IF strip at 10.7 MHz employing a buffer amplifier, two stages of gain, two ganged stages of AGC and an AGC summing amplifier. A single 561 N PLL serves as both the AM and FM detector. Input sensitivity to insure lockup for either AM or FM demodulation is approximately $10 \mu \mathrm{~V}$. The input level to the 561 N is held level at $305 \mathrm{mVp}-\mathrm{p}$ during input amplitude excursion from $10 \mu \mathrm{~V}$ to $120 \mathrm{mVp}-\mathrm{p}$. Potentiometer $\mathrm{R}_{\mathrm{AGC}}$ is adjusted at no input for a quiescent dc voltage (pin 6 of amplifier $\mu \mathrm{A} 741$ ) of -90 mV . This presets the MC1496 multipliers at a maximum gain condition. The gain is slowly reduced as the RF input level rises and full AGC action begins.
The bandwidth of linear demodulation of AM is 1 Hz to 4.5 Hz and of $F M$ is 1 Hz to 36 kHz .

IF gain adjustment can be provided with the installation of a potentiometer between pins 4 and 9 of either (or both) of the $\mu \mathrm{A} 733$, a zero ohm setting insuring maximum gain.
The addition of a conventional converter front-end and audio driver stages completes the circuitry for a receiver.

## Translation Loop for Precise FM (561N, 562N)

A translation loop mixes the output of two oscillators and produces a signal whose frequency is equal to the sum or difference of the two. In the most useful application of this circuit, one oscillator is a precise crystal-controlled oscillator and the second is a low frequency voltage-controlled oscillator so that the loop output is a FM signal whose center frequency is slightly offset from the crystal oscillator frequency. Since the offset oscillator supplies only a small percentage of the final output frequency, it need not be as precise as the crystal oscillator.
Such a loop is shown in Figure 9-58a. The VCO is driven until the filtered low frequency component of the PD2 output is equal to the offset frequency $f_{m}$. When this occurs, lockup is achieved and the VCO output is either $f_{R}+f_{m}$ or $f_{R}-f_{m}$. By adjusting the VCO free-running slightly above $f_{m}$, the latter case can be eliminated. If $f_{m}$ is frequency modulated, then the output will also be frequency modulated since it has the same absolute deviation.

Figure 9-58b shows a translation loop made from a 561 N and 562 N . It is designed to produce a 4.5 MHz signal with a deviation of $\pm 25 \mathrm{kHz}$. The 561 N serves as the VCO and PD1; the 562 N serves as the crystal oscillator and PD2. A 4.400 MHz crystal controls the reference frequency $f_{R}$. The offset frequency $f_{m}$ is 100 kHz frequency modulated $\pm 25 \mathrm{kHz}$ at a modulation frequency of 400 Hz . The accuracy of the output frequency is that of the reference oscillator plus that of the offset oscillator; since $f_{m}$ is a small percentage ( $2 \%$ ) of $f_{R}$, its stability can be considerably less than that of the crystal oscillator. In this case, $f_{m}$ can be provided by a 566 VCO modulated, if desired, by a second 566. (The triangle wave 566 output results in a constant df/dt.)
Special layout precautions are required to be sure that no high frequency coupling occurs via grounds or power supply lines. The circuit is adjusted by trimming the 562 VCO trimmer capacitor until the beat note present at test point 1 has the same frequency as $f_{m}$ throughout the deviation range ( $f_{m}$ can be deviated by hand or very slowly, say, at a 1 Hz rate, to observe that the beat note does not break up during sweep. If the beat note is lost at either extreme, adjust the VCO trimmer. If the full deviation cannot be obtained, decrease the 562 low pass filter capacitor slightly. Connect a counter to the output to be sure the loop is locked to $f_{R}+f_{m}$ and not $f_{R}-f_{m}$ (unless the latter is desired).

## IF GAIN STAGE WITH AGC AND AM/FM DETECTION



Figure 9-57

Naturally, the component values given may be altered for other applications. Note that as $f_{m}$ is made a smaller and smaller percentage of the total output frequency, it becomes difficult to prevent locking in the $f_{R}-f_{m}$ mode since the 562 lock range will likely include both $f_{R}-f_{m}$ and $f_{R}+f_{m}$. However, if $f_{m}$ is made too large a portion of the output frequency, then overall stability suffers unless $f_{m}$ is also quite precise.

## Phase Locked FSK

## Demodulators (560N, 565)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the " 0 " and " 1 " states (commonly called space and mark) of the binary data signal.


Figure 9-58a

The 560 N phase locked loop can be used as a receiving converter to demodulate FSK audio tones and to provide a shifting dc voltage to initiate mark or space code elements. The PLL can replace the bulky audio filters and undependable relay circuits previously used for this application. Connec-
tion of the 560N PLL as a FSK demodulator is illustrated in Figure 9-59.

The system functions by locking-on and tracking the output frequency of the receiver. The demodulator frequency shift appears at pin 9 as a direct-current voltage of


Figure 9-58b

## FSK DEMODULATOR USING 560N



Figure 9-59
about 60 mV amplitude and must be amplified and signal-conditioned to interface with the printer. The input voltage at pin 12 should be from 30 mV to 2 V peak-to-peak, square or sine wave. Pin 10, the deemphasis terminal, is used for bandshaping. The capacitor connected between this terminal and ground bypasses unwanted high frequency noise to ground. Pin 9 is the output (approximately 60 mVdc ) which is amplified, conditioned and fed to a voltage comparator amplifier ( $\mu \mathrm{A} 710$ ) to provide the proper voltages for interfacing with the printer. This specific circuit was designed to match the Bell 103C and 103D Data Phones. When modifying this circuit to accommodate other systems, maintain the resistance to ground from pin 9 at approximately $15 \mathrm{~K} \Omega$. Pins 3 and 2 are the connections for the external capacitor that determine the free-running frequency of the VCO. The $0.33 \mu \mathrm{~F}$ value indicated provides a VCO frequency, $f_{0}$, of approximately 1060 Hz . The value of the timing capacitor can be calculated by use of the following equation:
(Equation 9-48)
$C_{o}=\frac{300 \mathrm{pF}}{f_{0}}$ where $f_{o}$ is in hertz.
The output has a swing of 2 V peak-to-peak, over a 0 to 600 baud input FSK rate, with less than $10 \%$ jitter at the comparator output. The circuit is operative over a temperature range of $0^{\circ}$ to $75^{\circ} \mathrm{C}$ with a total drift of approximately 100 mV over the temperature range.

A simple scheme using the 565 to receive FSK signals of 1070 Hz and 1270 Hz is shown in Figure 9-60. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.
The loop filter capacitor C 2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency component. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate ( 300 baud or bits per second, or 150 Hz ) and twice the input frequency (about 2200 Hz ). The free-running frequency should be adjusted (with R1) so that the dc voltage level at the output is the same as that at pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6.

The input connection is typical for cases where a dc voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a $600 \Omega$ input impedance).
A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 9-61. Here, a constant current is injected into pin 8 by means of transistor Q1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift. The basis for this scheme is the fact that the output voltage (control voltage for VCO ) controls only the current through R1, while the current through Q1 remains constant. Thus, if most of the capacitor charging current is due to Q1, the current variation due to R1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25 mfd loop filter capacitor gives approximately $30 \%$ overshoot on the output pulse, as seen in the accompanying photographs.



The output is then filtered with a two-stage RC ladder filter with a band edge chosen to be approximately 800 Hz (approximately half-way between the maximum keying rate of 150 Hz and twice the carrier frequency). The' number of stages on the filter can be more or less depending on the degree of uncertainty allowable in the comparator output pulse. Two small capacitors (typically 0.001 mfd ) are connected between pins 8 and 7 of the 565 and across the input of the comparator to avoid possible oscillation problems.
For best operation, the free-running VCO frequency should be adjusted so that the output voltage (corresponding to the input frequencies of 1070 Hz and 1270 Hz swings equally to both sides of the reference voltage at pin 6 . This can be easily done by adjusting the center frequency of the VCO so that the output signal of the $\mu \mathrm{A} 710$ comparator has a $50 \%$ duty cycle. It is usually necessary to decouple pin 6 with a large capacitor connected to the positive supply in order to obtain a stable reference voltage for the $\mu \mathrm{A} 710$ comparator.

Figure 9-62 shows the output of the $\mu \mathrm{A} 710$ comparator and the output of the 565 phase
locked loop after the filter at rates of 100 , 200 and 300 baud, respectively.

## Analog Light-Coupled Isolators $(565,567)$

The analog isolator shown in Figure 9-63a is basically a FM transmission system with light as the transmission medium. Because of the high degree of electrical isolation achieved, low-level signals may be transmitted without interference by great potential difference between the sending and receiving circuits. The transmitter is a 565 used as a VCO with the input applied to the VCO terminal 7 . Since the light emitting diode is driven from the 565 VCO output, the LED flashes at a rate proportional to the input voltage. The receiver is a photo transistor which drives an amplifier having sufficient gain to apply a 200 mV peak-to-peak signal to the input of the receiving 565 , which then acts as a FM detector with the output appearing at pin 7 . Since the output has a twice carrier frequency ripple, it is best to keep the carrier frequency as high as possible (say, 100 times the highest modulation frequency ). Because of the excellent temperature stability of the 565 , drift is minimal even when dc levels are being transmitted. If
operation to dc is not required, the output of the receiver can be capacitively coupled to the next stage. Also, a 566 can be used as the transmitter.
Figure 9-63b shows that the 567 may be used in the same manner when operation from 5 V supplies is required. Here, the output stage of the 567 is used to drive the LED directly. When the free-running frequency of the receiving 567 is the same as that of the transmitting 567, the non-linearity of the two controlled oscillator transfer functions cancel so that highly linear information transfer results.
Figure $9-64$ is an oscillogram of the input and output of the Figure 9-63a circuit. The output can easily be filtered to remove the sum frequency component.

## PHASE MODULATORS

If a phase locked loop is locked onto a signal at the center frequency, the phase of the VCO will be $90^{\circ}$ with respect to the input signal. If a current is injected into the VCO terminal (the low pass filter output), the phase will shift sufficiently to develop an opposing average current out of the phase detector so that the VCO voltage is constant

## LIGHT-COUPLED ANALOG ISOLATORS



Figure 9-63a

and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase detector output rather than the VCO swing, the phase can be modulated over the full range of 0 to $180^{\circ}$. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 9-65a. The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 9-65b shows an implementation of this circuit using the 567 .

WAVEFORMS OF LIGHT-COUPLED ANALOG ISOLATOR (CIRCUIT A)


Figure 9-64

PHASE MODULATION USING THE PLL


Figure 9-65a

PHASE MODULATION USING THE PLL


Figure 9-65b

## Dual Tone Decoders (567)

Two integrated tone decoders can be connected (as shown in Figure 9-66a) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R1C1 and R1C1 are chosen, respectively, for tones 1 and 2 . If sequential tones ( 1 followed by 2 ) are to be decoded, then C3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure $9-66$ b shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the
unit 2 output stage is biased off by R2 and CR1 until activated by tone 1. A further variation is given in Figure 9-66c. Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn-on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

## High Speed, Narrow Band Tone Decoder

The circuit of Figure 9-66a may be used to

obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70 mV rms at all times to prevent detection band shrinkage and C2 should be between $130 / f_{0}$ and $1300 / f_{0}$ mfd where $f_{0}$ is the nominal detection frequency. The small value of C2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

## Touch-Tone ${ }^{\circledR}$ Decoder (567)

Touch-Tone ${ }^{\circledR}$ decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 967. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R1 and C1, to one of the seven tones. The R2 resistor reduces the bandwidth to about $8 \%$ at 100 mV and $5 \%$ at 50 mVrms . Capacitor C4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltage ( 50 to 100 mVrms ), the bandwidth can be controlled in the normal manner by selecting C 2 , thereby eliminating the seven R2 resistors and C4.

The only unusual feature of this circuit is the means of bandwidth reduction using the R2 resistors. In the Alternate Method of Bandwidth Reduction, Figure 9-68, an external resistor RA can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R2 serves the same function as $R_{A}$ except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R2 resistors of the two 567s which are being activitated. Capacitor C4 decouples the ac currents at the common point.

Figure 9-67 shows several additions to the "normal" method of tone decoding. The reduced capture time (shown dotted around the 697 Hz decoders) and reduced unlock time (shown with the 1477 Hz decoder) can be added to allow greater response time to the decoder at the expense of additional components. The addition of resistor R2 can be of greater advantage when selected such that the bandwidth of each decoder can be individually adjusted.


Figure 9-67
NOTE

$$
\frac{130}{1_{0}}\left(\frac{10 K+R}{R}\right)<C_{2}<\frac{1300}{1_{0}}\left(\frac{10 K+R}{R}\right)
$$

Adjust control for symmetry 0 , detection band edges about fo.

Figure 9-68


Figure 9-69

The curve in Figure 9-69 indicates that in order to obtain more control of the decoder the resistor R2 should be less than 10K.
The reduced capture time technique is described below.

Typical capture time for a phase lock loop can be as long as 10 cycles of incoming signal. For a frequency of 697 Hz (low tone of a touch tone system) this ends up in a delay time of up to 15 milliseconds. Lower frequencies result in much longer delays. In order to relieve these extended delays and to use external components (loop filter and low pass filter) which more closely match the design criteria, a system such as shown in Figure 9-67 is used.

The output of one of the tone decoders is phase shifted by 90 degrees at the given tone and fed into the second tone decoder. This forces the second tone decoder VCO to be phase shifted 90 degrees from the reference signal. The incoming signal is then fed to both devices. The maximum phase shift of the signal will be 45 degrees resulting in a 6 dB reduction in capture time.
The approach can be further expanded if a
third device is used, with each loop phase shifted 30 degrees from each other.

Improved noise immunity can be achieved by adding resistors across pins 1 and 4. A $50 \mathrm{k} \Omega$ resistor will improve the noise threshold by approximately $2-3 \mathrm{~dB}$. In effect the sensitivity of the system is reduced.

Latch up circuity is included in this set up. The outputs of each device are wire "OR" together.

## Reduced Release Time

Due to the nature of the output filter capacitor and the internal resistor, the decode unlatch time can be as long as 40 ms . This time can be reduced to less than $1 / 4$ of a cycle of the incoming tone by incorporating the circuitry shown in Figure 9-67. The output of the 567 is "added" together along with the output of a comparator. The comparator is triggered by the output of the 567 filter section. This output responds (within 1 cycle) of the incoming signal. The net result is the increased unlatch time of the decoder.

## Low Cost Frequency Indicator (567)

Figure 9-70 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set $6 \%$ above the desired sensing frequency and unit 2 is set $6 \%$ below the desired frequency. Now, if the incoming frequency is within $13 \%$ of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within $1 \%$ of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

## CRYSTAL-STABILIZED PHASE LOCKED LOOP

Figure 9-71a shows the 560 N connected as a tracking filter for signals near 10 MHz . The crystal keeps the free-running frequency at the desired value. Figure 9-71b gives the lock and capture range as a function of input amplitude. An emitter follower has been added to the normal VCO output to prevent pulling the loop off frequency.


Figure 9-71a

## LOCK RANGE vs INPUT AMPLITUDE

input
AMPLITUD
(mV(p-p))


Figure 9-71b

## Ramp Generators (566)

Figure 9-72 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the pin 3 output rapidly discharges C1 at the end of the charging period so that charging can resume instantaneously. The pnp transistor likewise rapidly charges the timing capacitor C 1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period $\tau$ is $1 / 2 f_{0}$ where $f_{0}$ is the 566 free-running frequency in normal operation. Therefore,
(Equation 9-49)

$$
\tau=\frac{1}{2 \mathrm{f}_{\mathrm{o}}}=\frac{\mathrm{RT} \mathrm{C}_{1} \mathrm{~V}+}{5\left(\mathrm{~V}+-\mathrm{V}_{\mathrm{C}}\right)}
$$

where $V_{c}$ is the bias voltage at pin 5 and $R_{T}$ is the total resistance between pin 6 and $\mathrm{V}+$. Note that a short pulse is available at pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)

## Sawtooth and Pulse Generator (566)

Figure 9-73 shows how pin 3 output can be used to provide different charge and discharge currents for C1 so that a sawtooth output is available at pin 4 and a pulse at pin 3. The pnp transistor should be well saturated to preserve good temperature stability. The charge and discharge times may be estimated by using the formula

$$
\tau=\frac{\mathrm{R}_{\mathrm{T}} \mathrm{C} 1 \mathrm{~V}+}{5\left(\mathrm{~V}+-\mathrm{V}_{\mathrm{c}}\right)}
$$

(Equation 9-50)
where $R_{T}$ is the combined resistance between pin 6 and $V+$ for the interval considered.

## Triangle-To-Sine Converters

Conversion of triangular wave shapes to sinusoids is usually accomplished by dioderesistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than $2 \%$ distortion
The first scheme (Figure 9-74a) uses the nonlinear IDS-VDS transfer characteristic of a p-channel junction FET to shape the triangle waveform. The second scheme (Figure 9-74b) uses the non-linear emitter

NEGATIVE RAMP GENERATOR


Figure 9-72a

POSITIVE RAMP GENERATOR


Figure 9-72b


Figure 9-73a


Figure 9-73b


Figure 9-74a
base junction characteristic of the 511 N for shaping.
In both cases, the amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the dioderesistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

## Single Tone Burst <br> Generator (566)

Figure 9-75 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is as a communications network alert signal. Cessation of the tone is accomplished by the SCR, which shunts the timing capacitor C1 charge current when activated. The SCR is gated on when C2 charges up to the gate voltage, which occurs in 0.5 seconds. Since only $70 \mu \mathrm{~A}$ are available for triggering, the

SCR must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R2 (and increasing C2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for $\mathrm{R} 2, \mathrm{R} 2=82 \mathrm{~K}$.

If the SCR is replaced by a npn transistor, the tone can be switched on and off at will at the transistor base terminal.

## Low Frequency FM

## Generators (566)

Figures 9-76 and 9-77 show FM generators for low frequency (less than 0.5 mHz center frequency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.
Capacitor C1 selects the modulation frequency adjustment range and C 1 selects
the center frequency. Capacitor C 2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.
If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

## Radio Frequency FM

## Generators (566, 560N)

Figure 9-78 shows how a 560 N may be used as a FM generator with modulation supplied by a 566 function generator. Capacitor C 1 is chosen to give the desired modulation range, C 2 is large enough for undistorted coupling and C3 with its trimmer specifies the center frequency. The VCO output may be taken differentially or single ended.
A 561 N or 562 N with appropriate pin numbering changes may also be used in this application. If a sweep generator is desired, the 566 may be connected as a ramp generator (described elsewhere in this chapter).


Figure 9-74b


## FREQUENCY MODULATED GENERATOR FOR SMALL DEVIATIONS (TO $\pm 20 \%$ )



Figure 9-76

## Precision Power Inverter $(566,540)$

Figure 9-79 shows a precision 12 Vdc to 115 Vac 100 W inverter. Its triangular output is derived from the 566 function generator, providing a high degree of frequency stability ( $\pm .02 \%{ }^{\circ} \mathrm{C}$ ). The 540 power driver is used to drive the power output stage. Because of third harmonic attenuation in the transformer, the output is very close to a pure 60 Hz sine wave.

## DESIGN IDEAS FOR USING PHASE LOCKED LOOPS

The following design ideas were drawn mainly from the Signetics-EDN Phase Locked Loop Contest. These circuits should be viewed as design suggestions only since Signetics has not verified their operating characteristics. In all cases, however, the principle of operation appears to be sound.

Quotation marks indicate quotes taken directly from the contest entry.

## Aircraft VHF <br> Omnidirectional Range (VOR) Receiver

Herbert F. Kraemer of Minneapolis, Minnesota, submitted the winning contest entry which uses one phase locked loop (562) as an AM detector, a second loop (565) as an


Figure 9-79

FM detector and a third loop (565) as a selfbiased phase detector.
"The circuit is a new type of VOR (VHF omnidirectional range) receiver used in air navigation to determine an airplane's angular bearing with respect to a VOR transmitter located on the ground. The principles of the circuit allow any desired increase in accuracy, as compared to current units, with potential cost savings.
"A VOR station transmits in the VHF band ( $108-117.9 \mathrm{MHz}$ ). Two signals are transmitted on the same carrier, i.e.,

1. A 30 Hz reference signal which frequency modulates an audio frequency subcarrier of 9960 Hz . This subcarrier then amplitude modulates the VHF carrier.
2. A 30 Hz directional signal which amplitude modulates the VHF carrier.
"The latter signal varies in phase with respeat to the reference, depending on the bearing of the VOR station and the receiver. Both signals are in phase when the receiver is north of the transmitter and 180 degrees out of phase when the receiver is south.
"Current VOR receivers are specified to be accurate within a 1-2 degree bearing, but many pilots accept 4 degree errors. The major design problem is to produce a receiver which will measure phase differences to an accuracy of about 1 degree, throughout the entire 360 degree range."

Although analog quarter-square multipliers can be built to an accuracy of $0.01 \%$, the
simpler analog phase detectors are only accurate to $3-4^{\circ}$. This circuit uses the NE562 PLL to frequency multiply the two 30 Hz signals, producing 60 and 120 Hz signals. A digital method combines these signals, thereby dividing the entire range of bearings into eight $45^{\circ}$ sectors. One of eight lights on the display will light, showing the pilot his approximate bearing. An analog method is then used to further determine the phase difference and the bearing within the given $45^{\circ}$ sector. Extending the principle further, sectors of $221 / 2^{\circ}$ could be used for improved accuracy.
This VOR receiver does not have the conventional to-from switch since it indicates directly throughout the entire $360^{\circ}$ range. Confusion of $180^{\circ}$ in bearing (going the wrong way) is impossible with this receiver.

System Description (References to Block Number-Figure 9-80)
Block 1. This is a standard VHF tuner.
Block 2. The NE561 is used for IF and AM detection.
Block 3. A low pass filter removes the 9960 Hz subcarrier. It appears that a zero crossing detector is not needed to shape the input signal to the NE562.
Block 4. Frequency multiplier.
Block 5. High pass filter.
Block 6. FM detection of 30 Hz signal.
Block 7. A calibration adjustment to compensate for any phase shifts throughout the circuit. A gain may be needed since the FM detector output is low.
Block 8. Another frequency multiplier.

Block 9. Standard ripple flip-flops for divide-by-two.

Block 10. A null principle is normally used in a VOR receiver so that the pilot can fly along a predetermined course, nulling the needle by turning his plane. To insure that the needle always reacts in the same direction for a given direction of error, even sectors are treated differently than odd sectors. The phase comparison is made with respect to C for odd sectors, and with respect to $\overline{\mathrm{C}}$ for even sectors.

Block 11. "At the desired null, the two signals must be 90 degrees out of phase to obtain a zero output from the phase detector. Some gain may be needed to compensate for the losses in Block 10.

Block 12. The phase detector portion of the NE565 only is used. The VCO part is unused but may be valuable in certain types of special displays.
An alternate form of analog phase detector might be an AND gate followed by a standard duty cycle integrator, such as used on dwell meters.

Block 13. The digital signals from the flipflops are decoded with AND gates to indicate the sector corresponding to the phase lag between the two 30 Hz signals."

## Speech Privacy Circuit (Speech Scrambler)

The second place entry was that of David M. Alexander of Austin, Texas. His application for the loop was a voice scramblerunscrambler for private communications.
"This circuit utilizes the principles of frequency inversion and masking to render speech unintelligible to listeners not possessing a similar unit. A synchronization signal is generated as part of the scrambled signal which phase locks the decoding carrier oscillator to the coding oscillator and thus guarantees minimum distortion in the unscrambled speech. This synch signal also increases the security close to the inversion point where they are displaced only slightly from their original values.
"In operation, a single circuit serves as both scrambler and unscrambler at one end of a two-way communications link. It is switched from the receive mode to the transmit mode by a multipole relay controlled by the push-to-talk switch on the system microphone or handset.
"As can be seen by the diagram (Figure 981), the major components of the system

## VHF OMNIDIRECTIONAL RANGE (VOR) RECEIVER



Figure 9-80

## SIMPLIFIED DIAGRAM OF VOICE SCRAMBLER



Figure 9-81
are the synch oscillator PLL-1 (NE560N), the carrier oscillator-modulator PLL-2 (NE561N) and the mixer-gain stage OA-1 ( $\mu$ A709).
"In the transmit mode, PLL-1 is adjusted to free-run at the inversion frequency $(1.5 \mathrm{kHz})$, or $1 / 2$ the desired carrier frequency. PLL-2 is phase locked to this oscillator and operates on its second harmonic frequency ( 3 kHz ). The audio to be scrambled is applied to the input of the multiplier of PLL-2. This produces the sum and difference products of the input audio and the encoding carrier. The sum product is filtered out by the low pass filter (Lx-Cx), leaving only the difference product. This product consists of the original audio signal with the frequency components inverted about $1 / 2$ the carrier frequency, or 1.5 kHz . The square wave output of the oscillator of PLL-1 is low pass filtered by network Ly-Cy to produce a sine wave sync signal which is mixed with the inverted speech by OA-1 to produce the final scrambled signal.
"In the receive mode, PLL-1 is phase locked to the 1.5 kHz synch and masking signal and acts as a signal conditioner for this signal. PLL-2 doubles this frequency to produce the decoding carrier. The scrambled signal is notch-filtered by network $\mathrm{Lz}-\mathrm{Cz}$ to remove the 1.5 kHz sync and masking signal and the resultant inverted audio applied to the multiplier of PLL-2. Here it is re-inverted in a manner similar to that of the transmit mode. The resultant unscrambled audio is amplified in OA-1 for output to further system audio stages."
[Note: It is suggested that the 1.5 kHz "sync and masking" signal be changed to 1.0 kHz , since PLL-2 (free-running at 3 kHz ) will lock
to the third harmonic of the 1 kHz square wave from the PLL-1 more readily than to the small second harmonic of the 1.5 kHz signal. It may then be desirable to disconnect the notch filter during transmission. Of course, the filters may be implemented using active filter techniques.]

## Precision Programmable Time Delay Generator

Sam Butt of Gaithersburg, Maryland, submitted the third place entry. This circuit provides both a pulse and a high frequency output at some time $t_{d}$ after an input pulse is received. The interval $t_{d}$ is programmable in 10 steps by means of a digital output switch.
Figure 9-82 shows the circuit in simplified form. It works as follows:

The 562 VCO is set so that its center frequency is at a point slightly above (say 10.5 MHz ) the window of the 10 MHz band pass filter (BPF). Thus, no rf appears at the output. When a pulse is received at the input, the flip-flop is set so as to actuate one input $A$ of the N8880A NAND gate.

The other side of the NAND gate $B$ receives a signal which occurs at the rate of $\mathrm{f}_{\mathrm{r}} / \mathrm{M}$ where $M$ is set by the binary-output switch. The output of the NAND gate begins to drive the N8291A binary ripple counter which is connected to the divide-by-N circuit in the loop feedback path. When 10 counts have been registered, the divide-by-N counter is putting out $f_{0} / 10$ or (in the assumed case) 1.05 MHz . Since the phase comparator now sees two frequencies very close together, the loop locks up and $f_{o}=10 f_{r}$. Since $f_{r}$ is 1 MHz , the VCO operates at 10 MHz rf which the band pass filter passes to the output. This rf is detected and used to reset the input flip-flop and the counter in preparation for the next input pulse. The duration of the rf output is determined mainly by the
detector time constant. The duration of the output pulse, which begins when the rf detector actuates the one-shot, is determined by the one-shot time constant.
(Equation 9-51)
The delay time is $t_{d}=\frac{N M}{f_{r}}$
where $M$ is settable between 1 and 10 using the digital switch.

## Metal Detector Using PLL as a Frequency Meter (565)

The metal detector shown in Figure 9-83 was submitted to the Signetics-EDN Phase Locked Loop Contest by Jim Blecksmith of Irvine, California. It incorporates a 565 as a frequency meter which indicates the frequency change in a Colpitts oscillator whose tank coil approaches a metal object. The loop output voltage at pin 7 is compared with the reference voltage at pin 6 and the difference amplified by meter amplifier Q4, Q5.

To increase the loop output (pin 7) to about 0.5 V per percent of frequency deviation, a current source (Q2, Q3) is used to supply most of the capacitor ( 2.5 mA ) charge and discharge current at pin 8 . The 20 k resistor connected to pin 8 changes the charge and discharge current by $0.5 \mathrm{~V} / 20 \mathrm{k} \Omega=0.25 \mathrm{~mA}$ or about $1 \%$ per 0.5 V . Since the voltage at pins 8 and 7 track, the loop output voltage is also 0.5 V per percent deviation. (This technique of increasing loop output swing for small frequency deviations is discussed in the Expanding Loop capability section of this chapter.)

Increasing oscillator frequency, as indicated by a rising meter indication, results when the search coil is brought near a nonferrous metal object. Reduced oscillator

frequency, as indicated by a dropping meter reading, results from the search coil being brought near a ferrous object.

## Programmed Phase or Frequency Shift

Howard E. Clupper of Chadds Ford, Pennsylvania, submitted the following circuit in which "a digital phase shifter is inserted in the loop between the VCO and the phase comparator. The phase shift is programmed by sequentially selecting the ring counter by means of the multiplexer and up-down counter.
"As shown in Figure 9-84, the eight ring counter outputs are separated by $45^{\circ}$, which is within the lock-in range of the loop. Output 1 is constrained to follow
the phase shift introduced and may be used, for example, to drive a synchronous motor above or below its normal speed, while still maintaining reference with the input. This is accomplished by monitoring the contents of the up-down counter (which may be any length). As long as the counter does not overflow, the motor may be advanced or retarded in any manner and then returned to the original relationship with respect to the 60 Hz reference input by running the U/D counter to the initial value.
"For higher frequency outputs, a divide-by- N counter may be added in the normal manner and the output taken directly from the VCO at output 2.
"Operation in this mode would provide
means to generate a precisely controlled FM signal of any arbitrary center frequency depending upon the frequency of the reference input and the value of N ."

The 565 may be used in this circuit in place of the 562 for lower frequency applications (less than 500 kHz ).

## FSK Data Converter For Cassette Recorder

A circuit scheme which allows an ordinary reel or cassette tape recorder to be used as a digital data recorder was submitted by Daniel Chin of Burlington, Massachusetts.
"The circuit design allows any singletrack audio tape recorder with frequency response to 7 kHz to be used as a digital

PHASE LOCK LOOP METAL DETECTOR


Figure 9-83

PROGRAMMED PHASE OR FREQUENCY SHIFTER


Figure 9-84
recorder for many non-critical applications. This application provides a complete data recording system using two recorded frequencies on a single track. The two frequencies are obtained from two synchronized NE565s. Detection of the recorded frequencies requires a third NE565. A fourth circuit is used to generate and synchronize the system clock. The advantages obtained by using these techniques are elimination of the need for:

1. A timing channel to strobe off the data, or
2. A third frequency for null, while using the other two frequencies for 1 and 0.
"This implementation, therefore, is one of the simplest ways to get a digital recording system on an audio recorder. It is shown in block diagram form in Figure 985.
"The parameters chosen for the circuit design allow a digital recording bit rate of 800 Hz or 1008 -bit characters per second. Though 100 characters per second is less than the 300-character-persecond speed of a high-speed paper tape reader, the low cost of this circuitry combined with the audio tape recorder should make this system very attractive from a cost performance viewpoint. This is especially true when compared with the normal Teletype speed of 10 characters per second.
"The circuits will also work with the readily available low cost cassette recorders now available, which make compact as well as low cost information storage. A FSK system of recording is used, which allows the voice recording and reproduction electronics of the recorder to be unmodified for use in recording digital information. The retained electronics may also be used to record voice message identification of the various sections of the tape.
"The intended use of this circuit is to convert an audio recorder for minicomputer written for engineering design applications. Such an application requires good information storage and retrieval over a wide range of storage time. Redundancy may be incorporated by using a two-channel recorder (stereo) and a FSK detector per channel. The outputs of the two detectors could then be ORed digitally to recover recorded is and, thus, give a safeguard against dropouts.

## Circuit Description

"Four NE565s are used in three circuits to achieve the design. These are:


Figure 9-86a
"The FSK detector (Figure 9-86a) is used to detect 6.4 kHz for a 1 and 4.8 kHz for a 0 . The data output is taken from a $\mu \mathrm{A} 711$ connected to pins 7 and 6 of the NE565. The recording method used is RZ FSK, which means that a zero is recorded as 4.8 kHz for the entire bit period and one is recorded as 6.4 kHz for about 60 percent of the period and 4.8 kHz for the remaining 40 percent of the period. This 60 percent bit duty cycle insures that the clock will synchronize with a negative transition during the time that a 1 should be detected.
"The clock generator (Figure 9-86b) is used to derive the 800 Hz with no input. When the data pulses are extracted from the recorded data, the clock is synchro-
nized to the data. The design allows up to 7 zeros in succession without causing the clock to go out of synchronization. This condition is easily met if odd parity is used to record the 8 -bit characters. (One of the 8 bits is a parity bit and, thus, one bit out of 8 is always a one.)
"The FSK generator (Figure 9-86c) provides the FSK signal for recording on tape. It consists of 2 oscillators locked to the basic 800 Hz system clock but oscillating at 6.4 kHz and 4.8 kHz . The incoming data to be recorded selects either oscillator as the frequency to be recorded. Harmonic suppression of the square wave output is taken care of automatically by the high frequency roll off characteristic of the tape recorder."


## Tape Recorder Flutter Meter

Using the 561 as a flutter meter for tape recorders was suggested by Ronald Blair of Houston, Texas. His circuit is given in Figure 9-87.
"The Signetics PLL 561 N is used to detect the frequency variations of the playback 3 kHz tone. The VCO frequency is set to a nominal 3 kHz by $\mathrm{C}_{0}$ and fine tuning trimmer. The demodulated output is ac coupled to a high input impedance amplifier. An oscilloscope can be used to measure peak deviations and a true RMS voltmeter is used to make RMS flutter readings. Note: Waveform is complex and averaging or peak reading meters will not give true readings.
"The output may be calibrated by feeding in a 3 kHz tone from an oscillator and offsetting the frequency by $1 \%$ and measuring the output level shift. Good recorders have RMS flutter of less than $0.1 \%$. The output can be filtered to study selected frequency bands.
"Speed variations in the movement of tape across the heads in a 4 tape recorder cause the playback frequency to vary from the original signal being recorded. These speed variations are caused by mechanical problems associated with the

tape drive and tape guidance mechanisms. The variation in frequency of the playback signal is called flutter and is generally measured over a frequency range of $0.5 \mathrm{~Hz}+0.200 \mathrm{~Hz}$.
"Test tapes with low recorded flutter variations are available to test playback mechanisms. These tapes are standardized at 3 kHz . With the systems equipped with record heads, a 3 kHz can be recorded for analysis."
[Note: A 565 may be used in place of the 561 N since the frequency is quite low.]

## SECTION 27 appenpices

| INCHES |  |  | DECIMALEQUIVALENT | MILLIMETER <br> EQUIVALENT <br> 0.397 <br> 0.794 |
| :---: | :---: | :---: | :---: | :---: |
| 1/64 | 1/32 |  |  |  |
| 3/64 |  | 1/16 | $\begin{aligned} & .0469 \\ & .0625 \end{aligned}$ | $\begin{aligned} & \hline 1.191 \\ & 1.588 \end{aligned}$ |
| 5/64 | 3/32 |  | $\begin{aligned} & .0781 \\ & .0938 \end{aligned}$ | $\begin{aligned} & 1.985 \\ & 2.381 \end{aligned}$ |
| 7/64 |  | 1/8 | $\begin{aligned} & \hline .1094 \\ & .1250 \end{aligned}$ | $\begin{aligned} & 2.778 \\ & 3.175 \end{aligned}$ |
| 9/64 | 5/32 |  | $\begin{aligned} & .1406 \\ & .1563 \end{aligned}$ | $\begin{aligned} & 3.572 \\ & 3.969 \end{aligned}$ |
| 11/64 |  | 3/16 | $\begin{aligned} & .1719 \\ & .1875 \end{aligned}$ | $\begin{aligned} & 4.366 \\ & 4.762 \end{aligned}$ |
| 13/64 | 7/32 |  | $\begin{aligned} & .2031 \\ & .2188 \end{aligned}$ | $\begin{aligned} & 5.159 \\ & 5.556 \end{aligned}$ |
| 15/64 |  | 1/4 | $\begin{aligned} & .2344 \\ & .2500 \end{aligned}$ | $\begin{aligned} & 5.953 \\ & 6.350 \end{aligned}$ |
| 17/64 | 9/32 |  | $\begin{aligned} & .2656 \\ & .2813 \end{aligned}$ | $\begin{aligned} & 6.747 \\ & 7.144 \end{aligned}$ |
| 19/64 |  | 5/16 | $\begin{aligned} & .2969 \\ & .3125 \end{aligned}$ | $\begin{aligned} & 7.541 \\ & 7.937 \end{aligned}$ |
| 21/64 | 11/32 |  | $\begin{aligned} & .3281 \\ & .3438 \end{aligned}$ | $\begin{aligned} & 8.334 \\ & 8.731 \end{aligned}$ |
| 23/64 |  | 3/8 | $\begin{aligned} & \hline .3594 \\ & .3750 \end{aligned}$ | $\begin{aligned} & 9.128 \\ & 9.525 \end{aligned}$ |
| 25/64 | 13/32 |  | $\begin{aligned} & .3906 \\ & .4063 \end{aligned}$ | $\begin{array}{r} 9.922 \\ 10.319 \end{array}$ |
| 27/64 |  | 7/16 | $\begin{aligned} & .4219 \\ & .4375 \end{aligned}$ | $\begin{aligned} & \hline 10.716 \\ & 11.112 \end{aligned}$ |
| 29/64 | 15/32 |  | $\begin{aligned} & .4531 \\ & .4688 \end{aligned}$ | $\begin{aligned} & 11.509 \\ & 11.906 \end{aligned}$ |
| 31/64 |  | 1/2 | $\begin{array}{r} .4844 \\ .5000 \\ \hline \end{array}$ | $\begin{aligned} & 12.303 \\ & 12.700 \\ & \hline \end{aligned}$ |
| 33/64 | 17/32 |  | $\begin{aligned} & .5156 \\ & .5313 \end{aligned}$ | $\begin{aligned} & 13.097 \\ & 13.494 \end{aligned}$ |
| 35/64 |  | 9/16 | $\begin{aligned} & .5469 \\ & .5625 \end{aligned}$ | $\begin{aligned} & 13.891 \\ & 14.287 \end{aligned}$ |
| 37/64 | 19/32 |  | $\begin{aligned} & .5781 \\ & .5938 \end{aligned}$ | $\begin{aligned} & 14.684 \\ & 15.081 \end{aligned}$ |
| 39/64 |  | 5/8 | $\begin{aligned} & \hline .6094 \\ & .6250 \end{aligned}$ | $\begin{aligned} & 15.478 \\ & 15.875 \end{aligned}$ |
| 41/64 | 21/32 |  | $\begin{aligned} & \hline .6406 \\ & .6563 \end{aligned}$ | $\begin{aligned} & \hline 16.272 \\ & 16.669 \end{aligned}$ |
| 43/64 |  | 11/16 | $\begin{aligned} & .6719 \\ & .6875 \end{aligned}$ | $\begin{aligned} & 17.067 \\ & 17.463 \end{aligned}$ |
| 45/64 | 23/32 |  | $\begin{aligned} & .7031 \\ & .7188 \end{aligned}$ | $\begin{aligned} & 17.860 \\ & 18.238 \end{aligned}$ |
| 47/64 |  | 3/4 | $\begin{aligned} & \hline .7344 \\ & .7500 \end{aligned}$ | $\begin{aligned} & 18.635 \\ & 19.049 \end{aligned}$ |
| 49/64 | 25/32 |  | $\begin{aligned} & .7656 \\ & .7813 \end{aligned}$ | $\begin{aligned} & 19.446 \\ & 19.842 \end{aligned}$ |
| 51/64 |  | 13/16 | $\begin{aligned} & .7969 \\ & .8125 \end{aligned}$ | $\begin{aligned} & 20.239 \\ & 20.636 \end{aligned}$ |
| 53/64 | 27/32 |  | $\begin{aligned} & .8281 \\ & .8438 \end{aligned}$ | $\begin{aligned} & 21.033 \\ & 21.430 \end{aligned}$ |
| 55/64 |  | 7/8 | $\begin{aligned} & .8594 \\ & .8750 \end{aligned}$ | $\begin{aligned} & \hline 21.827 \\ & 22.224 \end{aligned}$ |
| 57/64 | 29/32 |  | $\begin{aligned} & .8906 \\ & .9063 \end{aligned}$ | $\begin{aligned} & 22.621 \\ & 23.018 \end{aligned}$ |
| 59/64 |  | 15/16 | $\begin{aligned} & .9219 \\ & .9375 \end{aligned}$ | $\begin{aligned} & 23.415 \\ & 23.812 \end{aligned}$ |
| 61/64 | 31/32 |  | $\begin{aligned} & .9531 \\ & .9688 \end{aligned}$ | $\begin{aligned} & 24.209 \\ & 24.606 \end{aligned}$ |
| 63/64 |  | 1.0 | $\begin{array}{r} .9844 \\ 1.0000 \end{array}$ | $\begin{array}{r} 25.004 \\ 25.400 \\ \hline \end{array}$ |

## MATHEMATICAL CONSTANTS

| $\pi$ | $=3.14$ | $\sqrt{\pi}$ | $=1.77$ |
| ---: | :--- | ---: | :--- |
| $2 \pi$ | $=6.28$ | $\sqrt{\frac{\pi}{2}}=1.25$ |  |
| $(2 \pi)^{2}$ | $=39.5$ | $\sqrt{2}$ | $=1.41$ |
| $4 \pi$ | $=12.6$ | $\sqrt{3}$ | $=1.73$ |
| $\pi^{2}$ | $=9.87$ | $\frac{1}{\sqrt{2}}$ | $=0.707$ |
| $\frac{\pi}{2}$ | $=1.57$ | $\frac{1}{\sqrt{3}}$ | $=0.577$ |
| $\frac{1}{\pi}$ | $=0.318$ | $\log \pi$ | $=0.497$ |
| $\frac{1}{2 \pi}$ | $=0.159$ | $\log \frac{\pi}{2}$ | $=0.196$ |
| $\frac{1}{\pi^{2}}$ | $=0.101$ | $\log \pi^{2}$ | $=0.994$ |
| $\frac{1}{\sqrt{\pi}}$ | $=0.564$ | $\log \sqrt{\pi}$ | $=0.248$ |

## TEMPERATURE CONVERSION TABLE

|  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 100 | - 148 | + 60 | +140 | +220 | +428 | +380 | $+716$ |
| 95 | -139 | + 65 | +149 | +225 | +437 | +385 | +725 |
| 90 | - 130 | + 70 | $+158$ | $+230$ | $+446$ | $+390$ | +734 |
| 85 | - 121 | + 75 | +167 | $+235$ | $+455$ | +395 | +743 |
| 80 | - 112 | + 80 | +176 | +240 | +464 | +400 | +752 |
| 75 | - 103 | + 85 | +185 | $+245$ | $+473$ | +405 | +761 |
| 70 | - 94 | + 90 | +194 | +250 | $+482$ | $+410$ | $+770$ |
| 65 | - 85 | + 95 | +203 | +255 | +491 | +415 | +779 |
| 60 | - 76 | +100 | +212 | +260 | +500 | +420 | +788 |
| 55 | - 67 | +105 | +221 | +265 | $+509$ | +425 | +797 |
| 50 | - 58 | +110 | $+230$ | $+270$ | $+518$ | $+430$ | +806 |
| 45 | - 49 | +115 | +239 | $+275$ | +527 | $+435$ | $+815$ |
| 40 | - 40 | +120 | $+248$ | $+280$ | +536 | $+440$ | +824 |
| 35 | - 31 | +125 | +257 | $+285$ | +545 | +445 | +833 |
| 30 | - 22 | +130 | +266 | $+290$ | +554 | $+450$ | $+842$ |
| 25 | - 13 | +135 | $+275$ | $+295$ | +563 | +455 | +851 |
| - 20 | - 4 | +140 | $+284$ | $+300$ | +572 | $+460$ | $+860$ |
| - 15 | + 5 | +145 | +293 | +305 | +581 | +465 | +869 |
| - 10 | + 14 | +150 | +302 | $+310$ | $+590$ | $+470$ | $+878$ |
| 5 | + 23 | +155 | +311 | +315 | +599 | $+475$ | $+887$ |
| 0 | + 32 | $+160$ | $+320$ | $+320$ | +608 | $+480$ | $+896$ |
| + 5 | $+41$ | $+165$ | +329 | +325 | +617 | $+485$ | +905 |
| + 10 | $+50$ | $+170$ | +338 | $+330$ | $+626$ | $+490$ | +914 |
| + 15 | + 59 | +175 | $+347$ | $+335$ | +635 | $+495$ | +923 |
| + 20 | + 68 | +180 | +356 | $+340$ | +644 | $+500$ | +932 |
| $+25$ | + 77 | +185 | $+365$ | +345 | $+653$ | +505 | +941 |
| + 30 | $+86$ | +190 | $+374$ | +350 | +662 | $+510$ | +950 |
| + 35 | + 95 | +195 | +383 | +355 | $+671$ | $+515$ | +959 |
| + 40 | +104 | +200 | +392 | $+360$ | $+680$ | +520 | +968 |
| $+45$ | +113 | +205 | +401 | +365 | $+689$ | $+525$ | $+977$ |
| + 50 | +122 | +210 | $+410$ | +370 | +698 | $+530$ | +986 |
| - 55 | +131 | +215 | +41 | +3 | +7 | $+535$ | 95 |

## REACTANCE CHART



TABLE OF DECIBELS


## FREQUENCY CONVERSION FACTORS



## military

The Signetics Mil 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows The program is designed to provide our customers:

- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows
- Better delivery lead times by minimizing spec negotiation time, plus allows customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs

The following explains the different processing options available to you. Specia device marking clearly distinguishes the type of screening performed. Refer to Tables 1 and 2

## JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

## JAN PROCESSING (JBX)

This option is extremely useful when the reliability and screening of a JAN device is required, however, Signetics is not listed on the QPL for the product needed. Processing is performed to Mil-Std-883 Method 5004 , and product is $100 \%$ electrically tested to the appropriate JAN slash sheet.

Group B, C and D data for JAN processed and the other military processing levels

|  | JB | JBX | RBX | RB | S |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | JAN <br> Qualified | JAN <br> Processed | JAN <br> Rel | $/ 883$ | Mil <br> Temp |
| 54/54H | X | X | X | X | X |
| 54 LS | X | X | X | X | X |
| 54 S | X | X | X | X | X |
| $82 / 8 \mathrm{~T}$ | X | X | X | X | X |
| 93 XX | X | X | X | X | X |
| 96 XX | - | - | X | X | X |
| Linear | X | X | X | X |  |
| Bipolar Memory | Planned | X |  |  |  |
| Microprocessor | - | - | X | X | X |
|  |  |  | X | X |  |

Table 1 MILITARY SUMMARY

| JAN CASE OUTLINE AND LEAD FINISH | SIGNETICS MILITARY PACKAGE TYPES |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Dual-In-Line |  |  |
|  | 8-Pin | 10-Pin | 14-Pin | 16-Pin | 24-Pin |
| CB | - | - | F | - | - |
| EB | - | - | - | F | - |
| JB | - | - | - | - | I/F* |
| DB | - | - | W | - | - |
| FB | - | - | - | W | - |
| ZC | - | - | - | - | Q |
| GC | T | - | - | - | - |
| IC | - | K | - | - | - |

The gold plated versions of these packages will be available for a limited time.
All products listed in the Military section are also available in Die form.

## Table 2 MILITARY PACKAGE AVAILABILITY

which follow, consist of Group B, C and D testing performed per Mil-Std-883 Method 5005, in accordance with the Signetics Military Data Program

## JAN REL (RBX)

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std883 Method 5004, and is $100 \%$ electrically tested to industry data sheets.

## /883B (RB)

This is a lower priced version of the JAN Rel option described above. Processing is identical with the only exceptions being the dc electrical testing over the temperature range and ac electrical testing at room temperature are performed as a part of Group A instead of $100 \%$.

## MIL TEMP/883C (S/RC)

If you need a Military temp. range device,
but do not require all the high reliability screening performed in the other processing options, our Mil-Temp. product is ideal. Mil-Temp. parts are the standard full MilTemperature range product guaranteed to a 1\% AQL to the Signetics data sheet parameters.

## MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 3.

A Military Generic family is defined as consisting of die function and package type families.

## Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs
and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

| QUALIFIED SUB-GROUPS | QUALIFIES | OPTION 1 | OPTION 2 |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{A} \\ & \mathrm{~B} \end{aligned}$ | Electrical Test <br> Package-Same package construction and lead finish. | See NOTE 1 <br> Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal. | See NOTE 1 <br> Data selected from devices manufactured within 24 weeks of manufacturing period. |
| C | Die/Process-Devices representing the same process families. | Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period. | Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period. |
| D | Package-Same package construction and lead finish. | Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. <br> If specific data not available, Option 2 will be supplied. | Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period. |

NOTE

1. Group $A$ is performed on each lot or sublot of Signetics devices.

Table 3 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

| DESCRIPTION OF REQUIREMENTS AND SCREENS | MIL-M-38510 AND MIL-STD883 REQUIREMENTS, METHODS AND TEST CONDITIONS | REQUIREMENT | PROCESSING LEVELS |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \text { CLASS } \\ \text { A } \end{gathered}$ | JAN Qualified (JB) | JAN Processed (JBX) | JAN Rel (RBX) | $\begin{gathered} / 883 B \\ \text { (RB) } \end{gathered}$ | $\begin{gathered} / 883 C \\ \text { (RC) } \end{gathered}$ |
| General Mil-M-38510 <br> 1. Pre-Certification <br> A. Product Assurance Program Plan <br> B. Manufacturer's Certification | The manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1 | - | X | X | N/A | N/A | N/A | N/A |
| 2. Certification | Received after manufacturer has completed a successful survey, Para. 3.4.1.2 | - | X | X | N/A | N/A | N/A | N/A |
| 3. Device Qualification | Device qualification shall consist of subjecting the desired device to groups $A, B, C \& D$ of method 5005 to tightened LTPD, Para. 3.4.1.2 | - | X | X | N/A | N/A | N/A | N/A |
| 4. Traceability | Traceability maintained back to a production lot Para. 3.4.6 | - | $x$ | $x$ | X | $x$ | X | $x$ |
| 5. Country of Origin | Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1 | - | X | X | N/A | N/A | N/A | N/A |
| Screening Per Method 5004 of Mil-Std-883 |  |  |  |  |  |  |  |  |
| 6. Internal Visual (Precap) | 2010, Cond. A or B | 100\% | XA | XB | XB | XB | XB | XB |
| 7. Stabilization Bake | 1008, Cond. C Min; (24 Hrs @ $150^{\circ} \mathrm{C}$ ) | 100\% | X | X | X | X | X | X |
| 8. Temperature Cycling* <br> *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, $0^{\circ}$ to $+100^{\circ} \mathrm{C}$ ) | 1010, Cond. C; <br> ( 10 cycles, $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ ) | 100\% | X | X | X | X | $x$ | X |
| 9. Constant Acceleration | 2001, Cond. E; <br> ( 30 kg in YI Plane) | 100\% | X | X | X | X | X | X |
| 10. Visual Inspection | There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off." | 100\% | X | X | $x$ | X | X | X |
| 11. Seal (Hermeticity) |  |  |  |  |  |  |  |  |
| A. Fine | Cond. A or B ( $5.0 \times 10-8 \mathrm{CC} / \mathrm{Sec}$ ) | 100\% | x | $X$ | $x$ | $X$ | $x$ | $x$ |
| B. Gross | Cond. C2 Min. | 100\% | X | X | X | X | X | X |
| 12. Interim Electricals (Pre Burn-In) | Per applicable device specification | $\begin{aligned} & \text { 100\% } \\ & \text { Optional } \end{aligned}$ | $\begin{aligned} & 100 \% \\ & \text { Read \& } \end{aligned}$ | Slash Sheet | Slash <br> Sheet | Data Sheet | Data Sheet | N/A |
| 13. Burn-In | 1015, Cond. as specified (160 hrs. Min. at $125^{\circ} \mathrm{C}$ ) | 100\% | Record $100 \%$ | X | X | X | X | N/A |
| 14. Final Electricals | Per applicable Device Specification | 100\% | $\begin{gathered} 240 \mathrm{hrs} . \\ 100 \% \end{gathered}$ | Slash | Slash |  | Data | Data |
| A. Static Tests |  | 100\% | Read \& Record | Sheet | Sheet | Sheet | Sheet | Sheet |
| @ $25^{\circ} \mathrm{C}$ <br> B. Static Tests | Sub Group 1 |  | x | X | X | X | X | X |
| $@+125^{\circ} \mathrm{C}$ <br> C. Static Tests | Sub Group 2 |  | X | X | X | X | N/A | N/A |
|  | Sub Group 3 |  | X | X | X | X | N/A | N/A |

Table 4 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS

| DESCRIPTION OF REQUIREMENTS AND SCREENS | MIL-M-38510 AND MIL-STD883 REQUIREMENTS, METHODS AND TEST CONDITIONS | REQUIREMENT | PRocessing levels |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\underset{A}{\text { CLASS }}$ | JAN Qualified (JB) | JAN <br> Processed (JBX) | JAN Rel (RBX) | /883B <br> (RB) | /883C <br> (RC) |
| D. Dynamic Test <br> @ $25^{\circ} \mathrm{C}$ <br> E. Functional Test @ $25^{\circ} \mathrm{C}$ <br> F. Switching Test @ $25^{\circ} \mathrm{C}$ | Sub Group 4 for (Linear Product Mainly) <br> Sub Group 7 <br> Sub Group 9 |  | X | x <br> X x | X <br> X <br> X | x | X <br> X <br> N/A | X <br> X <br> N/A |
| 15. Percent Defective allowable (PDA) | A PDA of $10 \%$ is a normal requirement applied against the static tests @ $25^{\circ} \mathrm{C}(\mathrm{A}-1)$. This is controlled by the slash sheets for JB \& JBX products. For RBX \& RB $10 \%$ is standard. | 10\% | 5\% | X | ¢ | X | $x$ | N/A |
| 16. Marking | Fungus Inhibiting Paint | 100\% | As Req'd | $\begin{array}{\|c\|} \hline \text { JM38510/ } \\ \text { XXXX } \\ \text { Slash } \\ \text { Sheet \# } \end{array}$ | M38510/ <br> XXXX <br> Slash <br> Sheet \# | M38510/ <br> SXXXX Sig. Basic \# | $\begin{gathered} \text { SXXXX/ } \\ 883 \mathrm{~B} \\ \text { Sig. } \\ \text { Basic \# } \end{gathered}$ | $\begin{gathered} \text { SXXXX/ } \\ 883 C \\ \text { Sig. } \\ \text { Basic \# } \end{gathered}$ |
| 17. X-Ray | 2012 |  | 100\% | N/A | N/A | N/A | N/A | N/A |
| 18. External Visual | 2009 | 100\% | X | X | X | X | X | X |
| Quality Conformance Inspection per Method 5005 of Mil-Std-883 |  |  |  |  |  |  |  |  |
| 19. Group A | Electrical Tests-Final Electricals (\#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.) | Each Lot | X | X | x | $x$ | x | X |
| 20. Group B | Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual \& mechanical, bond strength \& solderability. | Every 6 week per microcircuit group | x | $x$ | Gener | c Data Avai |  |  |
| 21. Group C | Die related tests I.E. $1,000 \mathrm{hr}$. operating life, temperature cycling, \& constant acceleration. | Every 3 months per package type | X | X | Gener | c Data Av |  |  |
| 22. Group D | Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, \& salt atmosphere. | Every 6 months per package type | X | X |  | ic Data Ava |  |  |

Table 4 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS (Cont'd)

|  |  |  | $\begin{aligned} & \text { JAN } \\ & \text { QUAL* } \end{aligned}$ | JAN PROC- <br> ESSED | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | $\begin{gathered} \text { JM38510 } \\ \text { SLASH } \\ \text { SHEET } \end{gathered}$ |  |  | ¢ |
| 5400 | Quad 2-Input NAND Gate | /00104 | 11 | F W | F W |
| 5401 | Quad 2-Input NAND Gate with o/c | /00107 | 11 | F W | F W |
| 5402 | Quad 2-Input NOR Gate | /00401 | 11 | F W | F W |
| 5403 | Quad 2-Input NAND Gate with o/c | /00109 | 11 | F | F |
| 5404 | Hex Inverter | /00105 | 11 | F W | F W |
| 5405 | Hex Inverter with o/c | 100108 | 11 | F W | F W |
| 5406 | Hex Inverter w/Buffer/Driver with o/c | /00801 | - - | F W | F W |
| 5407 | Hex Buffer/Driver with o/c | /00803 | - - | F W | F W |
| 5408 | Quad 2-Input AND Gate | /01601 | 11 | F W | F W |
| 5409 | Quad 2-Input AND Gate with o/c | /01602 | 11 | F W | F W |
| 5410 | Triple 3-Input NAND Gate | /00103 | 11 | F W | F W |
| 5411 | Triple 3-Input NAND Gate | - | - - | - - | F W |
| 5412 | Triple 3-Input NAND Gate wih o/c | /00106 | - - | - | F W |
| 5413 | Dual NAND Schmitt Trigger | /15101 | * * | F W | F W |
| 5414 | Hex Schmitt Trigger | /15102 | * * | F W | F W |
| 5416 | Hex Inverter Buffer/Driver with o/c | /00802 | - - | F W | F W |
| 5417 | Hex Buffer/Driver with o/c | /00804 | - | F W | F W |
| 5420 | Dual 4-Input NAND Gate | /00102 | 11 | F W | F W |
| 5421 | Dual 4-Input AND Gate | - | - - | - - | F W |
| 5426 | Quad 2-Input NAND Gate with o/c | /00805 | 1 - | F - | F |
| 5427 | Triple 3-Input NOR Gate | /00404 | * * | F W | F W |
| 5428 | Quad 2-Input NOR Buffer | /16201 | - | - - | F W |
| 5430 | 8-Input NAND Gate | /00101 | 11 | F W | F W |
| 5432 | Quad 2-Input OR Gate | /16101 | * * | - - | F W |
| 5433 | Quad 2-Input NOR Buffer with o/c | - | - - |  | F W |
| 5437 | Quad 2-Input NAND Buffer | /00302 | 11 | F W | F W |
| 5438 | Quad 2-Input NAND Buffer with o/c | /00303 | 11 | F W | F W |
| 5439 | Quad 2-Input NAND Buffer | - | - - | - - | F W |
| 5440 | Dual 4-Input NAND Buffer | /00301 | 11 | F W | F W |
| 5442 | BCD-to-Decimal Decoder | /01001 | 11 | F W | F W |
| 5443 | Excess 3-to-Decimal Decoder | 101002 | 11 | F W | F W |
| 5444 | Excess 3-Gray-to-Decimal Decoder | 101003 | 11 | F W | F W |
| 5445 | BCD-to-Decimal Decoder/Driver with o/c | /01004 | - - | F W | F W |
| 5446A | BCD-to-7 Segment Decoder/ Driver | /01006 | - - | F W | F W |
| 5447A | BCD-to-7 Segment Decoder/ Driver | /01007 | - - | F W | F W |
| 5448 | BCD-to-7 Segment Decoder/ Driver | 101008 | - - | F W | F W |
| 5450 | Expandable Dual 2-Wide 2Input A01 | 100501 | 11 | F W | F W |
| 5451 | Dual 2-Wide 2-Input A01 Gate | 100502 | 11 | F W | F W |
| 5453 | 4-Wide 2-Input A01 Gate (Expandable) | /00503 | 11 | F W | F W |
| 5454 | 4-Wide 2-Input A01 Gate | 100504 | 11 | F W | F W |
| 5455 | 2-Wide 4-Input A01 Gate | 104005 | - | - - | - - |

NOTE
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* $=$ In process

LOGIC-5400 SERIES (Cont'd)

|  |  |  | $\begin{aligned} & \text { JAN } \\ & \text { QUAL* } \end{aligned}$ | $\begin{array}{\|c\|} \hline \text { JAN } \\ \text { PROC- } \\ \text { ESSED } \\ \hline \end{array}$ | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | $\begin{aligned} & \text { JM38510 } \\ & \text { SLASH } \\ & \text { SHEET } \end{aligned}$ |  |  |  |
| 5460 | Dual 4-Input Expander | - | - | - - | F W |
| 5470 | J-K Flip-Flop | /00206 | 11 | F W | $F \quad W$ |
| 5472 | J-K Master-Slave Flip-Flop | /00201 | 11 | $F \quad W$ | $F \quad W$ |
| 5473 | Dual J-K Master-Slave Flip-Flop | /00202 | 11 | F W | $F \quad W$ |
| 5474 | Dual D-Type Edge-Triggered Flip-Flop | /00205 | 11 | F W | F W |
| 5475 | Quad Bistable Latch | /01501 | 11 | F W | F W |
| 5476 | Dual J-K Master-Slave Flip-Flop | /00204 | 11 | F W | F W |
| 5477 | Quad Bistable Latch | /01502 | - 1 | W | W |
| 5480 | Gated Full Adder | - | - - | - - | F W |
| 5483 | 4-Bit Binary Full Adder | /00602 | 11 | F W | F W |
| 5485 | 4-Bit Magnitude Comparator | /15001 | 11 | F W | F W |
| 5486 | Quad 2-Input Exclusive-OR Gate | /00701 | 11 | F W | F W |
| 5490 | Decade Counter | /01307 | * * | F W | F W |
| 5491 | 8-Bit Shift Register | - | - - | - - | F W |
| 5492 | Divide-by-Twelve Counter | /01301 | 11 | F W | F W |
| 5493 | 4-Bit Binary Counter | /01302 | 11 | F W | F W |
| 5494 | 4-Bit Shift Register (PISO) | - | - - | - - | F W |
| 5495 | 4-Bit Left-Right Shift Register | /00901 | 1 | F | F W |
| 5496 | 5-Bit Shift Register | /00902 | 11 | F W | F W |
| 54100 | 4-Bit Bistable Latch (Dual) | - | - - | - - | F W |
| 54107 | Dual J-K Master-Slave Flip-Flop | /00203 | $1-$ | F | F |
| 54109 | Dual J-K Positive EdgeTriggered Flip-Flop | - | - - | - | F W |
| 54116 | Dual 4-Bit Latch with Clear | /01503 | 2 - | 1 - | 1 - |
| 54121 | Monostable Multivibrator | /01201 | 11 | F W | F W |
| 54122 | Retriggerable Monostable Multivibrator | /01202 | - - | - - | - - |
| 54123 | Retriggerable Monostable Multivibrator | /01203 | 11 | F W | F W |
| 54125 | Quad Bus Buffer Gate w/Tri-State Outputs | /15301 | 22 | F W | F W |
| 54126 | Quad Bus Buffer Gate w/Tri-State Outputs | /15302 | 22 | F W | F W |
| 54128 | Quad 2-Input NOR Buffer | - | - - | - - | F W |
| 54132 | Quad Schmitt Trigger | /15103 | * * | F. W | F W |
| 54145 | BCD-to-Decimal Decoder/Driver with o/c | /01005 | - | F W | F W |
| 54147 | 10-Line to 4-Line Priority Encoder | /15601 | * * | F W | F W |
| 54148 | 8-Line to 3-Line Priority Encoder | /15602 | * * | F W | F W |
| 54150 | 16-Line to 1-Line Mux | /01401 | 2 - | $1-$ | 1 |
| 54151 | 8-Line to 1-Line Mux | /01406 | 22 | F W | F W |
| 54152 | 8-Line to 1-Line Mux | - | - | - | F W |
| 54153 | Dual 4-Line to 1-Line Mux | /01403 | 22 | F W | F W |
| 54154 | 4-Line to 16-Line Decoder/ Demux | /15201 | * - | 1 | I Q |
| 54155 | Dual 2-Line to 4-Line Decoder/Demux | /15202 | 22 | F W | F W |
| 54156 | Dual 2-Line to 4-Line Decoder/Demux | /15203 | 22 | F W | F W |
| 54157 | Quad 2-Input Data Selector (non-inv.) | /01405 | 11 | F W | F W |
| 54158 | Quad 2-Input Data Selector (inv.) | - | - - | - - | F W |
| 54160 | Synchronous 4-Bit Decade Counter | /01303 | 11 | F W | F W |

## NOTE

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LOGIC-5400 SERIES (Cont'd)

|  |  |  | JAN QUAL | JAN PROC- <br> ESSED | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | $\begin{aligned} & \text { JM38510 } \\ & \text { SLASH } \\ & \text { SHEET } \end{aligned}$ |  |  |  |
| 54161 | Synchronous 4-Bit Binary Counter | /01306 | 11 | F W | F W |
| 54162 | Synchronous 4-Bit Decade Counter | /01305 | 11 | F W | F W |
| 54163 | Synchronous 4-Bit Binary Counter | /01304 | 11 | F W | F W |
| 54164 | 8-Bit Parallel-Out Serial Shift Register | /00903 | 1 - | F - | F |
| 54165 | Parallel-Load 8-Bit Shift Register | /00904 |  | F W | $\begin{array}{ll} F & W \\ F & W \end{array}$ |
| 54166 | 8-Bit Shift Register | - | - - | - - | F |
| 54170 | 4X4 Register File | /01801 |  |  |  |
| 54174 | Hex D-Type Flip-Flop with Clear | /01701 | 11 | F W | F W |
| 54175 | Quad D-Type Edge-Triggered Flip-Flop | /01702 | 11 | F W | F W |
| 54180 | 8-Bit Odd/Even Parity Checker | 101901 | - 2 | F W | F W |
| 54181 | 4-Bit Arithmetic Logic Unit | /01101 | 1 | 1 | 1 |
| 54182 | Look-Ahead Carry Generator | /01102 | 11 | F W | F W |
| 54190 | Synchronous Up/Down Counter (BCD) | - | - - | - - | * * |
| 54191 | Synchronous Up/Down Counter (Binary) | - | - - | - - | * * |
| 54192 | Synchronous Decade Up/Down Counter | /01308 | * * | F W | F W |
| 54193 | Synchronous 4-Bit Binary Up/Down Counter | /01309 | * * | F W | F W |
| 54194 | 4-Bit Bidirectional Universal Shift Register | /00905 | * * | F W | F W |
| 54195 | 4-Bit Parallel-Access Shift Register | /00906 | * * | F W | F W |
| 54198 | 8-Bit Shift Register | - | - - | - - | 1 Q |
| 54199 | 8-Bit Shift Register | - | - - | - - | - - |
| 54221 | Dual Monostable Multivibrator | - | - - | - - | F W |
| 54279 | Quad S-R Latch | - | - - | - - | F W |
| 54298 | Quad 2-Input Mux with Storage | - | - - | - - | F W |
| 54365 | Hex Buffer w/Common Enable (3-State) | /16301 | * * | * * | * |
| 54366 | Hex Buffer w/Common Enable (3-State) | /16302 | * * | * * | F W |
| 54367 | Hex Buffer, 4-Bit and 2-Bit (3-State) | /16303 | * * | * * | F W |
| 54368 | Hex Buffer, 4-Bit and 2-Bit (3-State) | /16304 | * | * * | F W |

NOTE
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* $=$ In process

| DEVICE | DESCRIPTION | JM38510 <br> SLASH <br> SHEET | JAN QUAL | $\begin{aligned} & \hline \text { JAN } \\ & \text { PROC- } \\ & \text { ESSED } \\ & \hline \end{aligned}$ | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| 54H00 | Quad 2-Input NAND Gate | /02304 | 11 | F W | W |
| 54 H 01 | Quad 2-Input NAND Gate with o/c | 102306 | 1 | F W | F W |
| 54H04 | Hex Inverter | 102305 | 11 | F W | W |
| 54H05 | Hex Inverter with o/c | - |  |  | w |
| 54H08 | Quad 2-Input AND Gate | /15501 | 2 - | $F-$ | F W |
| 54H10 | Triple 3-Input NAND Gate | 102303 | 1 | F W | F W |
| 54 H 11 | Triple 3-Input NAND Gate | /15502 | 2 - | F | F W |
| 54 H 2 O | Dual 4-Input NAND Gate | 102302 | 1 | F W | F W |
| 54 H 21 | Dual 4-Input AND Gate | /15503 | 2 | F | F W |
| 54 H 22 | Dual 4-Input NAND Gate with o/c | /02307 |  | F W | F W |
| 54H30 | 8-Input NAND Gate | 102301 | 11 | F W | w |
| 54H40 | Dual 4-Input NAND Buffer | 102401 |  | F W | F W |
| 54H50 | Expandable Dual 2-Wide 2-Input A01 | /04001 |  | F W | F W |
| 54H51 | Dual 2-Wide 2-Input A01 Gate | 104002 | 11 | F W | F W |
| 54H52 | $\begin{aligned} & \text { Expandable 4-Wide 2-2-2-3 } \\ & \text { Input AND-OR Gate } \end{aligned}$ | - | - - | - - | F W |
| 54H53 | 4-Wide 2-Input A01 Gate (Expandable) | 104003 | 11 | F W | F W |
| 54H54 | 4-Wide 2-Input A01 Gate | /04004 | 11 | F W | w |
| 54H55 | 2-Wide 2-Input A01 Gate | /04005 | 11 | F W | F W |
| 54H60 | Dual 4-Input Expander | - | - - | - - | F W |
| 54H61 | Triple 3-Input Expander | - | - - | - - | F W |
| 54H62 | 3-2-2-3 Input AND-OR Expander | - | - - | - - | F W |
| 54H71 | J-K Master-Slave Flip-Flop with AND-OR Inputs | - | - - | - - | F W |
| 54H72 | J-K Master-Slave Flip-Flop | 102201 | 1 | F W | F W |
| 54H73 | Dual J-K Master-Slave Flip-Flop | 102202 | 11 | F W | F W |
| 54H74 | Dual D-Type Edge-Triggered Flip-Flop | 102203 | 1 | F W | F W |
| 54H76 | Dual J-K Master-Slave Flip-Flop | 102204 | 1 . 1 | F W | F W |
| 54H101 | J-K Negative Edge-Triggered Flip-Flop | /02205 | 11 | F W | F W |
| 54H102 | J-K Negative Edge-Triggered Flip-FIop | - | - - | - | F W |
| 54H103 | Dual J-K Negative EdgeTriggered Flip-Flop | /02206 | 11 | F W | F W |
| 54H106 | Dual J-K Negative EdgeTriggered Flip-Flop | - | - | - - | F W |
| 54H108 | Dual J-K Negative EdgeTriggered Flip-Flop | - | - - | - - | F - |

NOTE
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1 = Level 1 Qualification
$2=$ Level 2 Qualification

LOGIC-54LS SERIES

|  |  |  | JAN QUAL | $\begin{aligned} & \text { JAN } \\ & \text { PROC- } \\ & \text { ESSED } \end{aligned}$ | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | $\begin{aligned} & \text { JM38510 } \\ & \text { SLASH } \\ & \text { SHEET } \end{aligned}$ |  |  |  |
| 54LS00 | Quad 2-Input NAND Gate | /30001 | 22 | F W | F W |
| 54LS01 | Quad 2-Input NAND Gate with o/c | - | - - | F W | F W |
| 54LS02 | Quad 2-Input NOR Gate | /30301 | 22 | F W | F W |
| 54LS03 | Quad 2-Input NAND Gate with o/c | /30002 | 11 | F W | F W |
| 54LS04 | Hex Inverter | /30003 | 11 | F W | F W |
| 54LS05 | Hex Inverter with o/c | /30004 | 11 | F W | F W |
| 54LS08 | Quad 2-Input AND Gate | /31004 | 22 | F W | F W |
| 54LS09 | Quad .2-Input AND Gate with o/c | - | - - | - - | F W |
| 54LS10 | Triple 3-Input NAND Gate | /30005 | 11 | F W | F W |
| 54LS11 | Triple 3-Input NAND Gate | /31001 | 22 | F W | $F \quad W$ |
| 54LS12 | Triple 3-Input NAND Gate with o/c | /30006 | 11 | F W | F W |
| 54LS13 | Dual NAND Schmitt Trigger | /31301 | * * | F W | F W |
| 54LS14 | Hex Schmitt Trigger | /31302 | * * | F W | $F \quad W$ |
| 54LS15 | Triple 3-Input AND Gate with o/c | /31002 | 2 | F W | F W |
| 54LS20 | Dual 4-Input NAND Gate | /30007 | 11 | F W | F W |
| 54LS21 | Dual 4-Input AND Gate | /31003 | 22 | F W | $F \quad W$ |
| 54LS22 | Dual 4-Input NAND Gate with o/c | /30008 | 11 | F W | F W |
| 54LS26 | Quad 2-Input NAND Gate with o/c | /32101 | * * | F W | F W |
| 54LS27 | Triple 3-Input NOR Gate | /30302 | 22 | F W | F W |
| 54LS28 | Quad 2-Input NOR Buffer | /30204 | * * | F W | F W |
| 54LS30 | 8-Input NAND Gate | /30009 | 22 | F W | F W |
| 54LS32 | Quad 2-Input OR Gate | /30501 | 22 | F W | F W |
| 54LS33 | Quad 2-Input NOR Buffer with o/c | - | - - | - - | F W |
| 54LS37 | Quad 2-Input NAND Buffer | /30202 | 22 | F W | F W |
| 54LS38 | Quad 2-Input NAND Buffer with o/c | /30203 | * * | F W | F W |
| 54LS40 | Dual 4-Input NAND Buffer | /30201 | 22 | F W | F W |
| 54LS42 | BCD-to-Decimal Decoder | /30703 | * * | * * | F W |
| 54LS51 | Dual 2-Wide 2-Input A01 Gate | 103401 | 22 | F W | $F \quad W$ |
| 54LS54 | 4-Wide 2-Input A01 Gate | /30402 | 22 | F W | F W |
| 54LS55 | 2-Wide 4-Input A01 Gate | - | - - | - - | F W |
| 54LS73 | Dual J-K Master-Slave Flip-Flop | /30101 | - | - - | F W |
| 54LS74 | Dual D-Type Edge-Triggered Flip-Flop | /30102 | * * | F W | F W |
| 54LS75 | Quad Bistable Latch | - | - - | F W | F W |
| 54LS76 | Dual J-K Master-Slave Flip-Flop | /30110 | * * | F W | F W |
| 54LS78 | Quad Bistable Latch | - | - - | - | F W |
| 54LS83A | 4-Bit Binary Full Adder | /31201 | * * | $F$ W. | F W |
| 54LS85 | 4-Bit Magnitude Comparator | /31101 | * * | F W | F W |
| 54LS86 | Quad 2-Input Exclusive-OR Gate | /30502 | * * | F W | F W |
| 54LS90 | Decade Counter | /31501 | * * | F W | F W |
| 54LS92 | Divide-by-Twelve Counter | /31510 | * * | F W | F W |
| 54LS93 | 4-Bit Binary Counter | /31502 | * * | F W | F W |
| 54LS95 | 4-Bit Left-Right Shift Register | /30603 | * * | F W | F W |
| 54LS96 | 5-Bit Shift Register | /30604 | * * | F W | F W |

## NOTE

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LOGIC-54LS SERIES (Cont'd)

|  |  |  | JAN QUAL | $\begin{array}{\|c\|} \hline \text { JAN } \\ \text { PROC- } \\ \text { ESSED } \\ \hline \end{array}$ | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | $\begin{gathered} \text { JM38510 } \\ \text { SLASH } \\ \text { SHEET } \end{gathered}$ |  |  |  |
| 54LS107 | Dual J-K Master-Slave Flip-Flop | /30108 | * * | F W | F W |
| 54LS109 | Dual J-K Positive EdgeTriggered Flip-Flop | /30109 | * * | F W | F W |
| 54 LS 112 | Dual J-K Negative EdgeTriggered Flip-Flop | /30103 | * * | F W | F W |
| 54LS113 | Dual J-K Negative EdgeTriggered Flip-Flop | /30104 | * * | F W | F W |
| 54LS114 | Dual J-K Negative EdgeTriggered Flip-Flop | /30105 | * * | F W | F W |
| 54LS122 | Retriggerable Monostable Multivibrator | /31403 | - - | - - | - - |
| 54LS125 | Quad Bus Buffer Gate w/Tri-State Outputs | /32301 | * * | * * | F W |
| 54LS126 | Quad Bus Buffer Gate w/Tri-State Outputs | /32302 | * * | * * | F W |
| 54LS132 | Quad Schmitt Trigger | /31303 | * * | F W | F W |
| 54LS136 | Quad Exclusive-OR with o/c | - | - - |  | F W |
| 54LS138 | 3-to-8 Line Decoder/Demux | /30701 | * * | * * | F W |
| 54LS139 | Dual 2-to-4 Line Decoder/ Demux | /30702 | * * | * * | F W |
| 54LS145 | BCD to Decimal Decoder/Dye | - |  | - | F W |
| 54LS151 | 8-Line to 1-Line Mux | /30901 |  | * * |  |
| 54LS153 | Dual 4-Line to 1-Line Mux | /30902 | * * | F W | F W |
| 54LS154 | 4-Line to 16-Line Decoder/ Demux | - | - | - - | 1 Q |
| 54LS155 | Dual 2-Line to 4-Line Decoder/Demux | - | - - | - | F W |
| 54LS157 | Quad 2-Input Data Selector (non-inv.) | /30903 | * * | F W | F W |
| 54LS158 | Quad 2-Input Data Selector (inv.) | /30904 | * * | F W | F W |
| 54LS160 | Synchronous 4-Bit Decade Counter | /31503 | * * | * * | F W |
| 54LS161 | Synchronous 4-Bit Binary Counter | /31504 | * * | F W | F W |
| 54LS162 | Synchronous 4-Bit Decade Counter | /31511 | * * | * * | F W |
| 54LS163 | Synchronous 4-Bit Binary Counter | /31512 | * * | * * | F W |
| 54LS164 | 8-Bit Parallel-Out Serial Shift Register | /30605 | * * | F W | F W |
| 54LS170 | 4X4 Register File | - | - - | - - | F W |
| 54LS173 | Quad D-Type Flip-Flop (Tri-State) (8T10) | - | - - | - | F W |
| 54LS174 | Hex D-Type Flip-Flop with Clear | /30106 | * * | F W | F W |
| 54LS175 | Quad D-Type Edge-Triggered Flip-Flop | /30107 | * * | F W | $F$ W |
| 54LS181 | 4-Bit Arithmetic Logic Unit | /03801 | 2 - | 1 - | 1 Q |
| 54LS190 | Synchronous Up/Down Counter (BCD) | /31513 | * * | F W | F W |
| 54LS191 | Synchronous Up/Down Counter (Binary) | /31509 | * * | F W | F W |

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LOGIC-54LS SERIES (Cont'd)

|  |  |  | JAN QUAL | $\begin{array}{\|c\|} \hline \text { JAN } \\ \text { PROC- } \\ \text { ESSED } \\ \hline \end{array}$ | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | $\begin{gathered} \text { JM38510 } \\ \text { SLASH } \\ \text { SHEET } \end{gathered}$ |  |  | ¢ |
| 54LS192 | Synchronous Decade Up/Down Counter | /31507 | * * | F W | F W |
| 54LS193 | Synchronous 4-Bit Binary Up/Down Counter | /31508 | * * | F W | F W |
| 54LS194 | 4-Bit Bidirectional Universal Shift Register | /30601 | * * | * * | * * |
| 54LS195 | 4-Bit Parallel-Access Shift Register | /30602 | * * | * * | * * |
| 54LS196 | Presettable Decade Counter/ Latch (8290) | /31601 | * * | * * | * * |
| 54LS197 | Presettable Binary Counter/ Latch (8291) | /31602 | * * | * * | * * |
| 54LS221 | Dual Monostable Multivibrator | /31402 |  | * * | * * |
| 54L.S251 | Data Selector/Mux with 3-State Outputs | /30905 | * * | * * | * * |
| 54LS253 | Dual 4-Line to 1-Line Data Selector/Mux | /30908 | * * | F W | F W |
| 54LS257 | Quad 2-Line to 1-Line Data Selector/Mux | /30906 | * * | F W | F W |
| 54LS258 | Quad 2-Line to 1-Line Data Selector/Mux | /30907 | * * | * * | F W |
| 54LS260 | Dual 5-Input NOR Gate | - | - - | - - | F W |
| 54LS261 | 2X4 Parallel Binary Multiplier | - | - - | - - | F W |
| 54LS266 | Quad Exclusive-NOR Gate | /30303 | 22 | F W | F W |
| 54LS279 | Quad S-R Latch | - | - - | - - | F W |
| 54LS280 | 9-Bit Odd/Even Parity Generator/Checker | - | - - | - - | * |
| 54LS283 | 4-Bit Adder | /31202 | * * | * * | F W |
| 54LS290 | Decade Counter | /32003 | * * | F W | F W |
| 54LS293 | 4-Bit Binary Counter | /32004 | * * | F W | F W |
| 54LS295A | 4-Bit Right-Shift Left-Shift Register | /30606 | * * | * * | F W |
| 54LS298 | Quad 2-Input Mux with Storage | - | - - | - - | F W |
| 54LS365 | Hex Buffer w/Common Enable (3-State) | /32201 | * * | * * | F W |
| 54LS366 | Hex Buffer w/Common Enable (3-State) | /32202 | * * | * * | F W |
| 54LS367 | Hex Buffer, 4-Bit and 2-Bit (3-State) | /32203 | * * | * * | F W |
| 54LS368 | Hex Buffer, 4-Bit and 2-Bit (3-State) | /32204 | * * | * * | F W |
| 54LS375 | Quad Latch | - | - - | - - | $F \quad W$ |
| 54LS386 | Exclusive-OR Gate | - | - - | - - | $F \quad W$ |
| 54LS395 | 4-Bit Cascadeable Shift Register (3-State) | /30607 | * | * * | F W |
| 54LS445 | BCD to Decimal Decoder/Dye | - | - - | - - | F W |
| 54LS670 | 4X4 Register File (Tri-State) | - | - - | - - | F W |

NOTE
Per QPL 38510-28 dated 1 April 1977.
$1=$ Level 1 Qualification
$2=$ Level 2 Qualification

|  |  |  | JAN QUAL | $\begin{aligned} & \text { JAN } \\ & \text { PROC- } \\ & \text { FSSEED } \end{aligned}$ | $\begin{array}{\|c\|} \hline \text { MIL } \\ \text { REL/883 } \\ \hline \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | JM38510 <br> SLASH <br> SHEET |  |  |  |
| 54S00 | Quad 2-Input NAND Gate | /07001 | 11 | F W | F W |
| 54S02 | Quad 2-Input NOR Gate | /07301 | 22 | F W | F W |
| $54 \mathrm{SO3}$ | Quad 2-Input NAND Gate with o/c | 107002 | 22 | F W | F W |
| 54S04 | Hex Inverter | /07003 | 11 | F W | F W |
| 54 S 05 | Hex Inverter with o/c | /07004 | 11 | F W | F W |
| $54 \mathrm{S08}$ | Quad 2-Input AND Gate | /08003 | * * | F W | F W |
| 54S09 | Quad 2-Input AND Gate with o/c | /08004 | - - | - - | F W |
| 54 S 10 | Triple 3-Input NAND Gate | 107005 | 22 | F W | F W |
| 54 S 11 | Triple 3-Input NAND Gate | /08001 | 22 | F W | F W |
| 54 S 15 | Triple 3-Input AND Gate with o/c | /08002 | 22 | F W | F W |
| 54S20 | Dual 4-Input NAND Gate | /07006 | 22 | F W | F W |
| 54S22 | Dual 4-Input NAND Gate with o/c | /07007 | 11 | F W | F W |
| 54S30 | 8-Input NAND Gate | 107008 | - - | - - | - - |
| 54S32 | Quad 2-Input OR Gate | - | - - | - - | F W |
| 54 S 40 | Dual 4-Input NAND Buffer | /07201 | 22 | F W | F W |
| 54 S 51 | Dual 2-Wide 2-Input A01 Gate | /07401 | 22 | F W | F W |
| $54 \mathrm{S64}$ | 4-2-3-2 Input A01 Gate | /07402 | 22 | F W | F W |
| 54 S 65 | 4-2-3-2 Input A01 Gate | /07403 | 22 | F W | F W |
| $54 \mathrm{S74}$ | Dual D-Type Edge-Triggered Flip-Flop | /07101 | 22 | F W | F W |
| $54 \mathrm{S85}$ | 4-Bit Magnitude Comparator | /08201 | * - | F - | F |
| 54 S 86 | Quad 2-Input Exclusive-OR Gate | /07501 | 22 | F W | F W |
| 54 S 112 | Dual J-K Negative EdgeTriggered Flip-Flop | /07102 | - - | - - | F W |
| 545113 | Dual J-K Negative EdgeTriggered Flip-Flop | /07103 | - - | - - | F W |
| $54 S 114$ | Dual J-K Negative EdgeTriggered Flip-Flop | /07104 | - - | - - | F W |
| 54S133 | 13-Input NAND Gate | /07009 | 22 | F W | F W |
| 545134 | 12-Input NAND Gate w/TriState Outputs | /07010 | 22 | F W | F W |
| 545135 | Quad Exclusive-OR/NOR Gate | /07502 | - - | - - | - - |
| 545138 | 3-to-8 Line Decoder/Demux | /07701 | - - | - - | - - |
| 545139 | Dual 2-to-4 Line Decoder/ Demux | /07702 | - - | - - | F W |
| 54 S 140 | Dual 4-Input NAND Line Driver | /08101 | 22 | F W | F W |
| $54 \mathrm{S151}$ | 8-Line to 1-Line Mux | /07901 | 22 | F W | F W |
| 545153 | Dual 4-Line to 1-Line Mux | /07902 | 22 | F W | F W |
| $54 \mathrm{S157}$ | Quad 2-Input Data Selector (non.inv.) | /07903 | 22 | F W | F W |
| 54 S 158 | Quad 2-Input Data Selector (inv.) | /07904 | * | F W | F W |
| 54 S 174 | Hex D-Type Flip-Flop with Clear | /07106 | - - | - | * * |
| $54 S 175$ | Quad D-Type Edge-Triggered Flip-Flop | /07105 | - - | - - | * * |
| $54 \mathrm{S181}$ | 4-Bit Arithmetic Logic Unit | /07801 | * - | 1 - | 1 |
| 54 S 182 | Look-Ahead Carry Generator | /07802 | - - | - - | * * |
| $54 \mathrm{S194}$ | 4-Bit Bidirectional Universal Shift Register | /07601 |  | - | - - |
| 54S195 | 4-Bit Parallel-Access Shift Register | /07602 | - - | - - | - - |

NOTE
Per QPL 38510-28 dated 1 April 1977
$1=$ Level 1 Qualification
$2=$ Level 2 Qualification

## LOGIC-54S SERIES (Cont'd)

|  |  |  | JAN QUAL | $\begin{aligned} & \text { JAN } \\ & \text { PROC- } \\ & \text { ESSED } \end{aligned}$ | $\begin{gathered} \text { MIL } \\ \text { REL/883 } \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEVICE | DESCRIPTION | JM38510 SLASH SHEET |  |  |  |
| 54S251 | Data Selector/Mux with 3-State Outputs | 108905 |  | - | - - |
| 54 S 253 | Dual 4-Line to 1-Line Data Selector/Mux | - | - - | - - | F W |
| 54 S 257 | Quad 2-Line to 1-Line Data Selector/Mux | 107906 | - - | - - | - - |
| 54 S 258 | Quad 2-Lint to 1-Line Data Selector/Mux | /07907 | - - | - - | - |
| 54 S 260 | Dual 5-Input NOR Gate | - | - - | - - | F W |
| 54 S 280 | 9-Bit Odd/Even Parity Generator/Checker | /07703 | - - | - | - - |
| 54 S 350 | 4/6 Bit Shifter-Tri-State | - |  | - - | F |

NOTE
Per QPL 38510-28 dated 1 Apr. 1977
$1=$ Level 1 Qualification
$2=$ Level 2 Qualification

| DEVICE | DESCRIPTION | JM38510 SLASH SHEET | JAN QUALIFIED* |  | JAN <br> PROCESSED |  | MILREL/883MIL TEMP |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Dip | Flat Pack | Dip | Flat Pack | Dip | Flat Pack |
| 8200 | Dual 5-Bit Buffer Register | - | - | - | - | - | I | Q |
| 8201 | Dual 5-Bit Buffer Register with D Inputs | - |  | - | - | - | 1 | Q |
| 8202 | 10-Bit Buffer Register | - | - | - | - | - | 1 | Q |
| 8203 | 10-Bit Buffer Register with D Inputs | - | - | - | - | - | 1 | Q |
| 8230 | 8-Input Digital Multiplexer | 101402 | * | * | F | W | F | w |
| 8231 | 8-Input Digital Multiplexer | - | - | - | - | - | F | w |
| 8232 | 8 -Input Digital Multiplexer | - | - | - | - | - | F | w |
| 8233 | 2-Input 4-Bit Digital Multiplexer | - | - | - | - | - | F | w |
| 8234 | 2-Input 4-Bit Digital Multiplexer |  | - | - | - | - | F | W |
| 8235 | 2-Input 4-Bit Digital Multiplexer | - | - | - | - | - | F | w |
| 8241 | Quad Exclusive-OR Gate | - | - | - | - | - | F | w |
| 8242 | Quad Exclusive-NOR Gate | - | - | - | - | - | F | w |
| 8243 | 8 -Bit Position Scaler | - | - | - | - | - | 1 | Q |
| 8250 | Binary-to-Octal Decoder | /15204 | 2 | 2 | F | w | F | w |
| 8251 | BCD-to-Decimal Decoder | /15205 | 2 | 2 | F | W | F | w |
| 8252 | BCD-to-Decimal Decoder | /15206 | 2 | 2 | F | W | F | W |
| 8260 | Arithmetic Logic Unit | - | - | - | - | - | 1 | Q |
| 8261 | Fast Carry Extender | - | - | - | - | - | F | w |
| 8262 | 9-Bit Parity Generator and Checker | - | - | - | - | - | F | w |
| 8263 | 3-Input 4-Bit Digital Multiplexer | - | - | - | - | - | 1 | Q |
| 8264 | 3-Input 4-Bit Digital Multiplexer |  | - | - | - | - | 1 | Q |
| 8266 | 2-Input 4-Bit Digital Multiplexer | - | - | - | - | - | F | w |
| 8267 | 2-Input 4-Bit Digital Multiplexer | - | - | - | - | - | F | w |
| 8268 | Gated Full Adder | - | - | - | - | - | F | Q |
| 8269 | 4-Bit Comparator | - | - | - | - | - | F | w |
| 8270 | 4-Bit Shift Register | - | - | - | - | - | F | w |
| 8271 | 4-Bit Shift Register | - | - | - | - | - | F | w |
| 8273 | 10-Bit Serial-In, Parallel-Out Shift Register | - | - | - | - | - | F | w |
| 8274 | 10-Bit Parallel-In, Serial-Out Shift Register | - | - | - | - | - | F | w |
| 8275 | Quad Bistable Latch | - | - | - | - | - | F | w |
| 8276 | 8 -Bit Serial Shift Register | - | - | - | - | - | F | - |
| 8277 | Dual 8-Bit Shift Register | - | - | - | - | - | F | - |
| 8280 | Presettable Decade Counter | - | - | - | - | - | F | W |
| 8281 | Presettable Binary Counter | - | - | - | - | - | F | w |
| 8284 | Binary Up/Down Counter | - | - | - | - | - | F | w |
| 8285 | Decade Up/Down Counter | - | - | - | - | - | F | w |
| 8288 | Divide-by-Twelve Counter | - | - | - | - | - | F | w |
| 8290 | Presettable High Speed Decade Counter | - | - | - | - | - | F | w |
| 8291 | Presettable High Speed Binary Counter | - | - | - | - | - | F | w |
| 8292 | Presettable Low Power Decade Counter | - | - | - | - | - | F | W |
| 8293 | Presettable Low Power Binary Counter | - | - | - | - | - | F | W |
| 9300 | 4-Bit Shift Register | /15901 | * | * | F | W | F | w |
| 9301 | BCD to Decimal Decoder | /15206 | 2 | 2 | F | W | F | w |
| 9308 | Dual 4-Bit Latch w/Clear | - | - | - | - | - | 1 | Q |
| 9309 | Dual 4-Input Multiplexer | /01404 | 1 | 1 | F | W | F | w |
| 9310 | 4-Bit Decade Counter | - | - | - | - | - | F | w |
| 9312 | 8 -Input Digital Multiplexer | 101402 | * | * | F | w | F | w |
| 9316 | 4-Bit Binary Counter | - | - | - | - | - | F | w |
| 9322 | Data Selector-Multiplexer | - | - | - | - | - | F | w |
| 9324 | 5-Bit Comparator | /15002 | * | * | F | WF | W | - |
| 9334 | 8-Bit Addressable Latch | /16001 | - | - | - | - | F | w |
| 9602 | Dual Monostable Multivibrator |  | * | * | F | w | F | W |

NOTE

[^9]LOGIC-8T INTERFACE SERIES

| DEVICE | DESCRIPTION | JAN M38510 SHEET | MIL REL/883 MIL TEMP |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | Dip | Flat <br> Pack |
| 8 T04 | 7-Segment Decoder Display Driver (Active-Low Outputs) | - | F | W |
| 8 T05 | 7-Segment Decoder Display Driver (Active-Hi Outputs) | - | F | W |
| 8T06 | 7-Segment Decoder Display Driver (Active-Low Outputs) | - | F | W |
| 8T09 | Quad Bus Driver with Tri-State Outputs | - | F | W |
| 8T10 | Quad D-Type Bus Latch (Tri-State) | - | F | W |
| 8T13 | Dual Line Driver | - | F | W |
| 8T14 | Triple Line Receiver/Schmitt Trigger | - | F | W |
| 8 T 18 | Dual 2-Input NAND (High Voltage to TTL Interface) | - | F | W |
| 8T20 | Bidirectional Monostable Multivibrator (Diff. Input) | - | * | * |
| 8 T22 | Retriggerable Monostable Multivibrator (54122/9601) | - | F | W |
| 8T26A | Quad Bus Driver/Receiver (Tri-State Outputs) | - | F | W |
| 8T28 | Quad Non-Inverting Bus Driver/Receiver (Tri-State Outputs) | - | F | W |
| 8T31 | 8-Bit Bidirectional I/O Port | - | * | * |
| 8T32 | Programmable 8-Bit, I/O Port (3-State) | - | 1 | * |
| 8 T33 | Programmable 8-Bit, I/O Port (Open Collector) | - | 1 | * |
| 8 T35 | Asynchronous Programmable 8-Bit I/O Port (Open Collector) | - | 1 |  |
| 8 ¢T37 | Hex Bus Receiver with Hysteresis-Schmitt Trigger (DM8837) |  | F | W |
| 8T38 | Quad Bus Transceiver (Open Collector) (DM8838) | - | F | W |
| 8 T 80 | Quad 2-Input NAND Gate (High Voltage) | - | F | W |
| 8T90 | Hex Inverter (High Voltage) | - | F | W |
| 8T95 | High Speed Hex Buffers/Inverters (74365/DM8095) | - | F | W |
| 8 T96 | High Speed Hex Buffers/Inverters (74366/DM8096) | - | F | W |
| $8 \mathrm{T97}$ | High Speed Hex Buffers/Inverters (74367/DM8097) |  | F | W |
| 8T98 | High Speed Hex Buffers/Inverters (74368/DM8098) |  | F | W |

[^10]BIPOLAR MEMORIES CROSS REFERENCE

| DEVICE | ORGANIZATION | PACKAGE* | FAIRCHILD | HARRIS | MMI | INTERSIL | AMD | TI |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PROMs |  |  |  |  |  |  |  |  |
| 82 S 23 | $32 \times 8$ | F R | - | 7602-2 | 5330 | 5600 | 27508 | $54 S 188$ |
| 82S115 | $512 \times 8$ | 1 R | - | 7644-2 | - | - | - |  |
| 82S123 | 32X8 | F R | - | 7603-2 | 5331 | 5610 | 27 S09 | 54 S 288 |
| $82 \mathrm{S126}$ | 256X4 | F R | 93416 | 7610-2 | 5300 | 5603 | 27 S10 | 54 S 387 |
| 825129 | 256X4 | F R | 93426 | 7611-2 | 5301 | 5623 | 27 S 11 | 54 S 287 |
| 825130 | $512 \times 4$ | F R | 93436 | 7620-2 | 5305 | 5604 | - | - |
| $82 \mathrm{S131}$ | 512 X 4 | F R | 93446 | 7621-2 | 5306 | 5624 | - | - |
| 82 S 136 | 1024X4 | F, I R | 93443 | 7642-2 | 5352 | 5606 | - | - |
| $82 S 137$ | 1024X4 | F, I R | 93453 | 7643-2 | 5353 | 5626 | - | - |
| $82 S 140$ | 512X8 | 1 R | 93438 | 7640-2 | 5340 | 5606 | - | - |
| 825141 | $512 \times 8$ | 1 R | 93448 | 7641-2 | 5341 | 5625 | - | - |
| $82 S 180$ | 1024X8 | 1 R | - | - | 5380 |  | - | - |
| $82 \mathrm{S181}$ | 1024X8 | $1 \quad \mathrm{R}$ | - | - | 5381 | - | - | - |
| $82 \mathrm{S184}$ | 2048×4 | 1 R | - | - | - | - | - | - |
| $82 \mathrm{S185}$ | 2048X4 | 1 R | - | - | - | - | - | - |
| $\begin{aligned} & \text { FPLAs } \\ & 82 S 100 \end{aligned}$ | 16X48X8 | 1 R | 93459 | - | 82S100 | - | 27 S 100 |  |
| 82S101 | $16 \times 48 \times 8$ | 1 R | 93458 | - | 82 S 101 | - | 27 S 101 | - |
| $\begin{aligned} & \text { PLAs } \\ & \text { 82S200 } \end{aligned}$ | 16X48X8 | R | - | - | - | - | - | - |
| 82S201 | 16X48×8 | $!\quad \mathrm{R}$ | - | - | - | - | - | - |
| RAMs |  |  |  |  |  |  |  |  |
| 54S89 | 16X4 | F $\quad$ R | - | - | - | - | - |  |
| $54 \mathrm{S189}$ | 16X4 | F $\quad$ R | - | - | - | - | - | 54189 |
| 54 S 200 | 256X1 | F $\quad$ R | - | - | - | - | - | 54 S 200 |
| 54 S 201 | 256X1 | F $\quad$ R | - | - | - | - | - | 54S201 |
| 545301 | 256X1 | F R | - | - | - | - | - | 54S301 |
| $82 \mathrm{SO9}$ | 64X9 | l R | 93419 | - | - | - | - | - |
| ${ }_{8} 2 \mathrm{~S} 10$ | 1024X1 | $\begin{array}{ll}\text { F, } & \mathrm{R} \\ \mathrm{F}\end{array}$ | 93415 | - | - | 55S08 | 2952 | - |
| $82 \mathrm{S11}$ | 1024X1 | F, I R | 93425 | - | - | 55S18 | 2953 | - |
| 82 S 16 | 256x1 | F $\quad$ R | 93421 | - | 5531 | 5523 | 2700 | - |
| $82 \mathrm{S17}$ | 256X1 | F $\quad$ R | 93411 | - | 5530 | 5533 | 2701 | - |
| 82 S 25 | 16X4 | $F \quad \mathrm{~F}$ | 93403 | 0064 | 5560 | 5501 | 3101 | - |
| ROMs |  |  |  |  |  |  |  |  |
| $82 \mathrm{S15}$ | $512 \times 8$ |  |  |  |  |  |  |  |
| 82S223 | $32 \times 8$ |  |  |  |  |  |  |  |
| 82 S 224 | 32X8 |  |  |  |  |  |  |  |
| 825226 | 256X4 |  |  |  |  |  |  |  |
| 82S229 | 256X4 |  |  |  |  |  |  |  |
| 82S230 | 512X4 |  |  |  |  |  |  |  |
| 825231 | 512X4 |  |  |  |  |  |  |  |
| 82S280 | 1024X8 |  |  |  |  |  |  |  |
| 82S281 | 1024X8 |  |  |  |  |  |  |  |

*NOTE
R=BeO Flat Pack
$\mathrm{F}=$ Cerdip
I= Ceramic DIP

LINEAR MIL REL/883 MIL TEMP.

| DEVICE | DESCRIPTION | PACKAGE |
| :---: | :---: | :---: |
|  | COMPARATORS |  |
| SE521 | Dual Comparator | F |
| SE526 | Analog Voltage Comparator | F K |
| SE527 | Analog Voltage Comparator | F K |
| SE529 | Analog Voltage Comparator | F K |
| LH2111 | Dual Comparator | F |
| LM111 | Comparator | F T |
| LM119 | Dual Comparator | F K |
| LM139 | Quad Comparator | F |
| LM193/193A | Dual Comparator | T |
| $\mu \mathrm{A} 710$ | Differential Voltage Comparator | F T |
| $\mu \mathrm{A} 711$ | Comparator | $F \quad K$ |
| SE510 | DIFFERENTIAL AMPLIFIERS <br> Dual Differential Amplifier | F |
| SE511 | Dual Differential Amplifier | F |
| SE515 | Differential Amplifier | $F \quad K$ |
| $\mu \mathrm{A} 733$ | Video Amplifier | $F \quad K$ |
| LF155/156 | OPERATIONAL AMPLIFIERS FET Op Amp | T |
| LH2101A | Dual Op Amp | F |
| LH2108A | Dual Op Amp | F |
| LM101 | High Perf. Op Amp | F T |
| LM101A | High Perf. Op Amp | F T |
| LM107 | General Purpose Op Amp | $F \quad F$ |
| LM108 | Precision Op Amp | $F \quad \mathrm{~T}$ |
| LM108A | Precision Op Amp | F T |
| LM124 | Quad Op Amp | F |
| LM158 | Dual Op Amp | T |
| MC1556 | Op Amp | $F \quad T$ |
| MC1558 | Dual Op Amp | F T |
| SE532 | Dual Op Amp | T |
| SE535 | Hi Slew Rate Op Amp | T |
| SE538 | Hi Slew Rate Op Amp | T |
| $\mu \mathrm{A} 709$ | Op Amp | F T |
| $\mu$ A709A | Op Amp | F T |
| $\mu \mathrm{A} 741$ | General Purpose Op Amp | $F \quad$ T |
| $\mu \mathrm{A} 747$ | Dual Op Amp | F K |
| $\mu$ A748 | General Purpose Op Amp | F T |


| DEVICE | DESCRIPTION | PACKAGE |
| :---: | :---: | :---: |
| SE567 | PHASE LOCKED LOOPS Tone Decoder P11 | F T |
|  | LINE RECEIVERS Dual Differential Line Receiver | F |
| DM7830 | Dual Differential Line Receiver | F |
|  | TIMERS |  |
| SE555 | Timer | F T |
| SE556 | Dual Timer | F |
| SE558/9 | Quad Timer | F |
|  | VOLTAGE REGULATORS <br> 5 Volt Regulator | DA |
| SE5554 | Dual Track Reg | F |
| 78XX (7) | Positive Reg | DA |
| 79XX (7) | Negative Reg | DA |
| 79MXX (7) | Med Power Reg | DB |
| $\mu \mathrm{A} 723$ | Precision Voltage Regulator | $F \quad L$ |
| DS1611-1614 | DRIVERS |  |
|  | Peripheral Drivers | T |
|  | D/A |  |
| MC1508-8 | 8-Bit D/A | F |
| SE5008 | 8-Bit D/A | F |
| SE5009 | 8-Bit D/A | F |

BIPOLAR MICROPROCESSORS

|  |  | AVAILABILITY |  |
| :---: | :---: | :---: | :---: |
| PRODUCT | DESCRIPTION | Dip | Flat Pack |
| 3001 | Microprogram Control Unit | I | R |
| 3002 | Central Processing Element (2-bit slice) | I | R |
| $8 \times 300$ | Interpreter/Microcontroller | I | $*$ |
| $2901-1$ | Central Processing Element (4-bit slice) | $*$ | $*$ |

*Under development

## MICROPROCESSOR SUPPORT CIRCUITS

| PRODUCT | DESCRIPTION | AVAILABILITY |  |
| :---: | :---: | :---: | :---: |
|  |  | Dip | Flatpack |
| LOGIC |  |  |  |
| 54123 | Retriggerable Monostable Multivibrator | F | W |
| 54180 | 8-Bit Odd/Even Parity Checker | F | W |
| 54298 | Quad 2-Input Mux with Storage | F | W |
| 54 S 182 | Look-Ahead Carry Generator | * | * |
| 545194 | 4-Bit Bidirectional Shift Register | * | * |
| 54S195 | 4-Bit Parallel Access Shift Register | * | * |
| 54LS365 | High Speed Hex Tri-State Buffer | F | * |
| 54LS366 | High Speed Hex Tri-State Buffer | F | * |
| 54LS367 | High Speed Hex Tri-State Buffer | F | * |
| 54LS368 | High Speed Hex Tri-State Buffer | F | * |
| 8262 | 9-Bit Parity Generator Checker | F | W |
| 8281 | Presettable Binary Counter | F | W |
| 8291 | Presettable High Speed Binary Counter | F | W |
| 9602 | Dual Monostable Multivibrator | F | W |
| INTERFACE |  |  |  |
| 8T09 | Quad Bus Driver with Tri-State Output | F | W |
| 8T10 | Quad D-Type Bus Latch (Tri-State Outputs) | F | W |
| 8T13 | Dual Line Driver | F | W |
| 8T14 | Triple Line Receiver/Schmitt Trigger | F | W |
| 8T26A | Quad Bus Driver/Receiver (Tri-State) | F | W |
| 8T28 | Quad Bus Non-Inverting Driver/Receiver (Tri-State) | F | W |
| 8T32 | Programmable 8-Bit I/O Port (3-State) | 1 | * |
| 8 T33 | Programmable 8-Bit I/O Port (Open Collector) | 1 | * |
| 8T35 | Asynchronous Programmable 8-Bit I/O Port (Open Collector) | 1 | * |
| 8 T 95 | High Speed Hex Buffer (Tri-State) | F | * |
| 8T96 | High Speed Hex Inverter (Tri-State) | F | * |
| 8T97 | High Speed Hex Buffer (Tri-State) | F | * |
| 8T98 | High Speed Hex Inverter (Tri-State) | F | * |

## PACHAGES

## Pl|thers

## INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

## General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across VCC and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

## Plastic Only

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

## Hermetic Only

9. Lead material
a. Alloy 52-gold plated, or solder dipped.
b.ASTM alloy F-15 (KOVAR) or equivalentgold plated, tin plated, or solder dipped.
c. ASTM alloy F-30 (Alloy 42) or equivalenttin plated.
d.ASTM alloy F-15 (KOVAR) or equivalentgold plated.
e.ASTM alloy F-15 (KOVAR) or equivalenttin plated.
10. Body Material
a. 1010 Steel-nickel plated or tin plate over nickel.
b. Eyelet, ASTM alloy F-15 or equivalent-gold or tin plated.
c. Eyelet, ASTM alloy F-15 or equivalent-gold or tin plated, glass body.
d. Ceramic with glass seal at leads.
e. BeO ceramic with glass seal at leads.
f. Ceramic with ASTM alloy F-15 or equivalent.
11. Lid Material
a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
b. Nickel or tin plated nickel, weld seal.
c. Ceramic, glass seal.
d. ASTM alloy $\mathrm{F}-15$ or equivalent, gold plated.
e. BeO Ceramic with glass seal.
f. Translucent $\mathrm{A1}_{2} \mathrm{O}_{3}$, glass seal.

PLASTIC PACKAGES

| NO. OF LEADS | PACKAGE CODE | $\theta_{\mathrm{ja}} / \theta_{\mathrm{jc}}\left({ }^{0} \mathrm{C} / \mathrm{W}\right)$ | DESCRIPTION1 | PAGE |
| :---: | :---: | :---: | :---: | :---: |
| Standard Dual-in-Line |  |  |  |  |
| 8 | NE | 162/65 |  | 3 |
| 14 | NH | 150/65 | TO-116/MO-001 | 3 |
| 16 | NJ | 137/53 | MO-001 | 3 |
| 18 | NK | 135/53 |  | 3 |
| 20 | NL | 135/53 |  | 3 |
| 22 | NM | 120/53 |  | 3 |
| 24 | NN | 116/53 | MO-015 | 4 |
| 28 | NQ | 116/53 | MO-015 | 4 |
| 40 | NW ${ }^{3}$ | 110/50 | MO-015 | 4 |
| Power Dual-in-Line |  |  |  |  |
| 14 | NHA ${ }^{2}$ | 95/33 | Butterfly | 3 |
| 16 | NJA ${ }^{2}$ | 95/33 | Butterfly | 3 |
| 18 | NKA ${ }^{2,3}$ | 90/26 | Butterfly | 3 |
| 20 | NLA ${ }^{2,3}$ | 90/26 | Butterfly | 3 |
| 24 | NNA ${ }^{2}$ | 60/23 | Butterfly | 4 |
| 28 | NQA ${ }^{2}$ | 56/21 | Butterfly | 4 |
| Power |  |  |  |  |
| 3 | S | 200/70 | TO-92 | 5 |
| 3 | U | 75/3 | TO-220 | 5 |
| $3+$ GND | GB ${ }^{3}$ | 95/15 | Single-in-Line (SIL) | 5 |
| 4 + GND | $\mathrm{GC}^{3}$ | 95/15 | Single-in-Line (SIL) | 5 |
| $12+$ GND | $\mathrm{PH} / \mathrm{PHA}^{3}$ | 3 95/15 | Batwing | 5 |

12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb .010 inches.
15. Maximum glass climb or lid skew is .010 inches.
16. Typical four places.
17. Dimension also applies to seating plane.

Pheners

HERMETIC PACKAGES

| NO. OF LEADS | $\begin{aligned} & \text { PACKAGE } \\ & \text { CODF } \end{aligned}$ | $\theta_{\mathbf{j a}} / \theta_{\mathbf{j c}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | DESCRIPTION ${ }^{1}$ | PAGE |
| :---: | :---: | :---: | :---: | :---: |
| Metal Headers |  |  |  |  |
| 2 | DA | TBD | TO-3 Solid Header | 6 |
| 3 | DB | TBD | TO-39 Solid Header, Short Can | 6 |
| 4 | DC | TBD | TO-72 Solid Header | 6 |
| 4 | DE | TBD | TO-72 Glass Filled Header | 6 |
| 8 | T | 150/25 | TO-99 Header ( 200 Dia.) | 7 |
| 10 | K | 150/25 | TO-100 Header, Short Can | 7 |
| 10 | L | 150/25 | TO-100 Header, Tall Can | 7 |
| Flat Packs |  |  |  |  |
| 10 | WF | 240/50 | Flat Ceramic | 8 |
| 14 | WH | 205/50 | Flat Ceramic | 8 |
| 16 | WJ | 200/50 | Flat Ceramic | 8 |
| 24 | WN | 155/40 | Flat Ceramic | 8 |
| 16 | RJ/RJA | 133/30 | Flat Ceramic, BeO | 8 |
| 18 | RKA ${ }^{3}$ | TBD | Flat Ceramic, BeO | - |
| 24 | RNA | TBD | Flat Ceramic, BeO | 8 |
| 28 | RQA | TBD | Flat Ceramic, BeO | 9 |
| 40 | RWA | TBD | Flat Ceramic, BeO | 9 |
| 10 | QF | 230/55 | Flat Ceramic | 9 |
| 14 | QH | 185/45 | Flat Ceramic | 9 |
| 16 | QJ | 170/45 | Flat Ceramic | 9 |
| 24 | QN | 155/44 | Flat Ceramic | 9 |
| 10 | QFA | 230/55 | Flat Ceramic Laminate | 10 |
| 14 | QHA | 185/45 | Flat Ceramic Laminate | 10 |
| 16 | QJA | 170/45 | Flat Ceramic Laminate | 10 |
| 24 | QNA | 155/44 | Flat Ceramic Laminate | 10 |
| Cerdip Family |  |  |  |  |
| 14 | FH | 110/30 | Dual in-Line Ceramic | 11 |
| 16 | FJ | 100/30 | Dual-in-Line Ceramic | 11 |
| 18 | FK | 93/27 | Dual-in-Line Ceramic | 11 |
| 22 | FM | 75/27 | Dual-in-Line Ceramic | 11 |
| 24 | FN | 60/26 | Dual-in-Line Ceramic | 11 |
| Laminated Ceramic, Side Brazed Lead |  |  |  |  |
| 8 | IEA | 100/30 | Dip Laminate | 12 |
| 14 | IHA | 95/25 | Dip Laminate | 12 |
| 16 | IJA | 90/25 | Dip Laminate | 12 |
| 18 | IKA | 88/25 | Dip Laminate | 12 |
| 22 | IMA | 80/25 | Dip Laminate | 12 |
| 24 | INC/IND | - 65/25 | Dip Laminate | 12 |
| 28 | IQA | 60/25 | Dip Laminate | 13 |
| 40 | IWA | 55/25 | Dip Laminate | 13 |
| 50 | IZA | TBD | Dip Laminate | 13 |

## NOTES

1. Dual-in-Line packages unless otherwise described
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads
3. Package not yet available, scheduled for 1977 release

## PACKAGES

PLASTIC: Standard and Power Dual-In-Line

## NE Package



## NJ Package and NJA Package



## NL Package and NLA Package



## NH Package and NHA Package



NK Package and NKA Package


NM Package


## PACKAGES

## PLASTIC: Standard and Power Dual-In-Line (cont'd.)

NN Package and NNA Package


NQ Package and NQA Package


NW Package

## Package not yet available

 Scheduled for 1977 release
## PACKAGES

PLASTIC: Power (Not Dual-In-Line)

## S Package



## U Package



GB Package

Package not yet available Scheduled for 1977 release

Package not yet available Scheduled for 1977 release

## PH/PHA Package




댐ㅁㅁtirs

## PACKAGES

## HERMETIC: Metal Headers

## DA Package



## DC Package



CONSTRUCTION NOTES: 9b, 10b, 11b

## DB Package



CONSTRUCTION NOTES: 9b, 10b, 11b

## DE Package



CONSTRUCTION NOTES: 9b, 10c, 11b

## PACKAGES

## HERMETIC: Metal Headers (cont'd.)

## T Package



CONSTRUCTION NOTES: 9b, 10c, 11b

## K Package



CONSTRUCTION NOTES: 9b, 10c, 11b

## L Package



CONSTRUCTION NOTES: 9b, 10c, 11b

## HERMETIC: Flat Packs

## WF Package



CONSTRUCTION NOTES: 9c, 10d, 11c

## WH Package



## WN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

## RNA Package



## PACKAGES

HERMETIC: Flat Packs (cont'd.)


CONSTRUCTION NOTES: 9c, 10e, 110

## OF Package



CONSTRUCTION NOTES: 9d, 10d, 11c

## QJ Package



CONSTRUCTION NOTES: 9d, 10d, 11c

## RWA Package



OH Package


CONSTRUCTION NOTES: 9d, 10d, 1ich
QN Package


## PACKAGES

HERMETIC: Flat Packs (cont'd.)

## OFA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

OJA Package


CONSTRUCTION NOTES: 9d, 10f, 11c

OHA Package

CONSTRUCTION NOTES: 9d, 10f, 11c

QNA Package

CONSTRUCTION NOTES: 9d, 10f, 11c


RKA Package

Package not yet available
Scheduled for 1977 release

## PACRAGES

## HERMETIC: Cerdip

FH Package


CONSTRUCTION NOTES: 9c, 10d, 11c

FK Package


CONSTRUCTION NOTES: 9c. 10d, 11c

## FJ Package

CONSTRUCTION NOTES: 9c, 10d, 11c

## FM Package



FN Package


CONSTRUCTION NOTES: 9c, 10d, 11c

## PACRAES

## HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package

construction notes: 9e, 10f, 11c

## IJA Package



CONSTRUCTION NOTES: 9e, 10f, 119

## IMA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

IHA Package


CONSTRUCTION NOTES: 9e, 10f, 11c

## IKA Package



CONSTRUCTION NOTES: 9e, 10f, 110

INC Package and IND Package


CONSTRUCTION NOTES: 9e, 10f, 11c, 11f (IND

## PACKAGES

HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

## IQA Package



IWA Package


## IZA Package



CONSTRUCTION NOTES: 90, 10f, 11c

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[^0]:    is $\mathrm{V}+-1.5 \mathrm{~V}$, but either or both inputs can go to +32 V without damage

[^1]:    1. $7900 \mathrm{C}-0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$
[^2]:    4. $-40^{\circ} \mathrm{C} \leq \mathrm{TJ} \leq+125^{\circ} \mathrm{C}$ for SA78MHVOOC
[^3]:    4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
    5. Specified with trigger input high.
    6. Time measured from a positive going input pulse from 0 to 0.8 VCc into the threshold to the drop from high to low of the output. Trigger is tied to threshold
[^4]:    $\dagger$ Exact value depends on line length
    $\ddagger \mathrm{V}_{\mathrm{Cc}}$ is 4.5 V to 5.5 V for both the DS7820 and DS7830
    *Optional to control response time

[^5]:    Design data for the two previous circuits (for other circuits the same sequence of component value selection must be used):
    BT138 triac with: $\quad V_{G T}=1.6 \mathrm{~V}$ at $0^{\circ} \mathrm{C} \quad$ Mains voltage: $\mathrm{V}_{\mathrm{S}}=220 \mathrm{~V}$ $\mathrm{I}_{\mathrm{GT}}=72 \mathrm{~mA}$ at $0^{\circ} \mathrm{C}$ Triac load: 1200 W $\mathrm{IL}<60 \mathrm{~mA}$

[^6]:    NOTE
    All resistance values are typical and in ohms.
    All capacitance values are in picofarads.

[^7]:    NOTES

    1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
    2. Pin number references pertain to K package pinout only.
[^8]:    1. Chroma input signal voltage $=0$ and normal reference input signal voltage $=1.0 \mathrm{Vp}-\mathrm{p}$
    2. Reference Figure 2
[^9]:    Per QPL 38510-28 dated 1 Apr. 1977
    $1=$ Level 1 Qualification
    $2=$ Level 2 Qualification

[^10]:    * = Qualification planned

