Exhibit 6

# BRIEF DESCRIPTION OF CIRCUIT FUNCTIONS

# CM24 GSIII 107B brief circuit description

## 1. Video pre-amplifier:

The TDA4886A (7301) is a monolithic integrated RGB pre-amplifier for colour monitor system with I2C bus control and OSD mixer, in addition to bus control beam current limiting, the signal are amplified in order to drive output driver LM2435 (7701), individual black level control is provided by using 3 DAC outputs (pin 17/20/23) for external cut-off control.

The RGB input signals with nominal signal amplitude of 0.7Vb-w are capacitively coupled (2308/2310/2311) into TDA4886A from a 75 Ω (3301/3302/3303) source and actively clamped to an internal DC voltage during signal black level by CLBL (pin 5) signal from deflection controller. A fast signal blanking is driven by CLBL signal and control bit DISV=1.

The input signal is related to the internal reference black level can be simultaneously adjusted by contrast control via I2C bus with 6 bits DAC. For white point adjustment the individual three channels gain control are driven by I2C bus with 6 bit DAC too.

In the output stage the nominal input signal will be amplified to 2.8Vb-w output color signal at nominal contrast and maximum gain. Individual output clamping is to set the reference black level of the signal output to a value which corresponds to the intend cut-off voltage of the CRT cathodes, all feedback reference are driven by I2C bus.

The output signal from pre-amplifier R (pin19), G (pin16) and B (pin22) are sent to LM2435 to have around 40Vp-p amplitude, which are AC coupled to the CRT and need to be clamped to cut-off level. These are achieved by the black level clamp circuits 7721, 7722, 6721, 6722, 2724, 3723, 3724, 3725, 3726, 3727 for Red channel, the rest channel are identical to it and all of three channels are controlled by TDA4886A.

The OSD signal are inserted during fast blanking active period, the OSD and fast blanking signal are generated by OSD IC MTV018.

## 2.0. Micro-controller & USB device:

The micro-controller P83C830(7801) is monitor micro-controller which can interface to the PC host via DDC (SCL, SDA) and provide the automatic alignment funtion in production. The internal built in hardware can detect sync. presence for the VESA DPMS standard of various display mode with separated (pin 13: H 16; V) or composite sync. (pin15) signal. The digital/analog voltage output can be used to control the video and deflection function of the monitor.

Besides to control two bus driven IC TDA4841 and TDA4886A via I2C bus , micro-controller output still handle the rest function as V-DC shift, rotation, brightness, stand-by, off mode, degaussing, LED color, H-unlock detector, ABL, s-cap switch, H-Dc shift, and H-linearity, after alignment the data are stored at EEPROM 7804.

The CM2400 can iterface with host system via USB (Universal serial bus), this interfacing is achieved by using a bus transformation IC PDIUSBD11 (7891) which transforms the USB to IIC bus then link with micro-controller P83C380 to accept the command from host and provide the monitor control function like H-size, V-sise, -------etc., this makes the CM2400 into an USB device.

**3. Deflection controller:**

The TDA4841 is a high performance and efficient solution for autosync monitors. All functions are controllable by I2C bus. TDA4841 provides synchronization processing, horizontal and vertical with full autosync capability, it provides extended function e.g. as a flexible B+ control. and extensive set of geometry control facilities.

The HSYNC (pin15) is the input for horizontal synchronization signal which can be separated or composite TTL sync with positive or negative polarity. The horizontal oscillator capacitor at HCAP (pin 29) for optimum jitter performance the value of 10nF must not be changed. The given value is widely synchronized from 30KHz to 92KHz.

PLL1 phase detector compares the middle of horizontal sync with a fixed point on the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL1 (pin 26). Via register HPOS the I2C bus allows a linear adjustment of the relative phase between horizontal sync and oscillator sawtooth (in PLL1 loop). Via registers HPARAL and HPINBAL correction of pin unbalance and parallelogram is done by modulating the phase between oscillator sawtooth and horizontal flyback (in PLL2 loop).

The PLL2 phase detector is similar to PLL1 detector and compares the line flyback pulse at HFLB (pin 1) with the oscillator sawtooth voltage. The control currents are independent of horizontal frequency. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of HDRV (pin8) output pulse.

EWDRV (pin 11) provides a complete geometry drive waveform. The horizontal size, pincushion, , corner correction, and trapezium correction are controlled by the registers HPIN, HSIZE, HCOR and HTRAP.

The VSYNC (pin14) is the input for vertical synchronization signal it can be separated TTL or extract from composite sync. with positive or negative polarity. The widely synchronization range from 50 to 160Hz.

The amplitude of the differential output currents at VOUT1 and VOUT2 can be adjusted via register VSIZE. Register VPOS provides a DC shift at the sawtooth output VOUT1 and VOUT2 (pin 13 and pin 12) and the EW drive output EWDRV (pin11) in such a way, that the whole picture moves vertically while maintaining the correct geometry.

The horizontal moiré (also known as video moiré) can be cancelled by controlling register HMOIRE and cancelled vertical moiré (scan moiré) by controlling register VMOIRE.

The B+ function block can be used for buck converter in feed forward mode. It provides a frequency independent pulse width to control the deflection circuit.

## 4. Horizontal deflection:

The horizontal output signal 7503 pin 8 (limited at very low amplitude around 1.4Vp-p) directly fed to driver stage 7601, after boost to about 150Vp-p and amplifies current drive capability it drives output transistor 7602 to reach expected deflection current. The horizontal linearity orrection circuits is composed by 5 segments S-cap. switch (7614, 7615, 7616, 7617 & 7635) and one current controllable linearity coil 5606 to get optimised linearity.

The B+ control output signal is modulated with geometry control and size control signal together, it directly feed to buck converter 7605 via buffer stage 7603, 7604 to supply an adequate deflection voltage to output stage. The horizontal raster position control circuits is composed by 5603, 6605, 6606, 7606, 7607, 5604, 7608 and 7610 to reach right center position. To correct the tilt symptom while monitor facing the different direction or operating at various place, the rotation coil (plus control ckt. 7611, 7626, 7627...) is needed to against the magnetic field changing.

## 5.0 EHT generator and Vertical output stage:

The EHT generator HVG II - 30 supplies 26KV anode voltage to picture tube. The generator is fully separated from the horizontal deflection.

The output voltage is stabilised at 26KV. The out voltage is kept constant by regulating the supply voltage of the EHT output stage.
The generator is protected against over voltage (x-ray). Over voltage protection, it is activated if EHT exceed 27.5 - 29.5 KV, the generator will be switched off immediately and a restart can only be made by switching the monitor off and on.

EHT generator also supply tertiary voltage for concern circuits like:

| | |
|---|---|
| -150Vdc | : for spot killer |
| +400Vdc | : for vertical dynamic focus |

Under this configuration, stand-by mode just switching off the L4990A to achieve less than 15 Watt consumption.

TDA 4841 vertical differential output pin 12/13 fed to 7404 TDA8177F input pin2/3 and boost to expected deflection current around 1.5Ap-p.

## 6.0 Power supply:

The power supply works at a fixed frequency about 72.6KHz in flyback mode and suitable for universal line input 90-264Vac. The proper PTC for the degaussing part, it working automatically at switch on for about 6 seconds or pushing an external button via OSD under PTC cold condition.

The mains voltage, rectified 6102 (GBU6J) and filtered 2105 (220μF/400V), is applied to the power transformer 5101 which switching the power transistor 7105, transfer the energy to

secondary side. Besides, an auxiliary voltage is obtained from the primary side to supply the power controller TEA1504.

. The power transformer secondary side rectified and filtered out defined voltages : +188V, +84V, -6.3V, +14V,-14V( +8V, and +5V are drop out from +14V). +84V is sensed and subtracted to a stabilized reference voltage; the error signal is amplified and send to PWM circuits via optocoupler, where it is compare with ramp waveform to keep constant voltage output by modulating duty cycle.

The primary current is sensed by the resistor 3115/3116/3117/3118, when current increase to over current threshold point then power shut down immediately. When a short circuits occurs on the outputs , the primary current increase in such a way that the power supply turns off.

An OVP circuits is built inside the power controller, while the voltage Vaux over +14V and output is shut down immediately.

Power management off mode is directly short circuits optocoupler pin 1 to ground via 3161 and 7155, let power supply enter burst mode, it delivery out very low power (less than 5 watt).