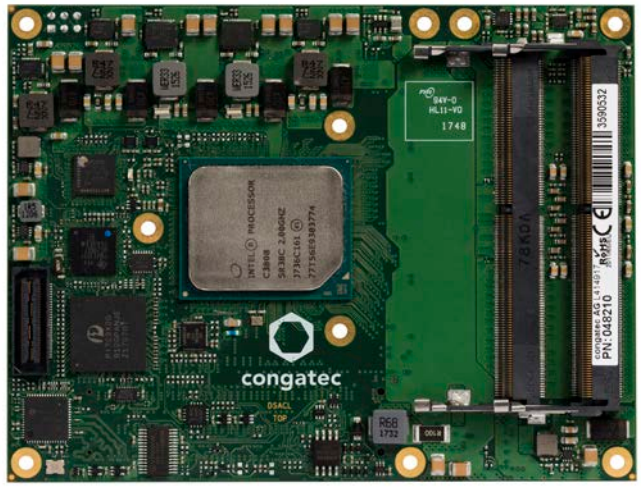

COM Express™ conga-B7AC

Next Generation Intel® Atom® SoCs

User's Guide

Revision 1.5

congatec

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2018-05-11	AEM	• Preliminary release
0.2	2018-08-24	AEM	• Deleted eMMC support from tables 2 “Commercial Variants” and 3 “Industrial Variants” • Added eMMC feature as optional in section 2.1 “Feature Summary” • Corrected the product name in section 5.1.3.1 “PCIe Routing” • Updated table 32 “Power and GND Signal Descriptions” by adding missing GND pins
0.3	2018-09-14	AEM	• Changed the eMMC option to optional in tables 3 “Commercial Variants” and 4 “Industrial Variants” • Corrected rows A-B PCIe root port configuration in table 11 “PCI Express Features”
1.0	2019-06-28	AEM	• Added commercial variant with part number 048205 to table 2 “Commercial Variants” • Updated section 2.5 “Power Consumption” • Updated the drawing in section 2.3 “Mechanical Dimensions” • Added cooling variants to section 4 “Cooling Solutions” and updated the cooling dimensions • Added content to section 9 “System Resources” • Updated section 10.3 “Updating the BIOS” and added section 10.4 “Recovering from External Flash” • Official release
1.1	2019-10-30	AEM	• Changed the maximum memory DIMM capacity to 96 GB in sections 1.2 “Options Information” and 2.1 “Feature List” • Updated section 6.1.5 “Power Loss Control” • Changed RSMRST# to CB_RESET# in section 8.4 “Boot Strap Signals” • Added note about the minimum pulse width required for proper button detection in table 28 “Power and System Management Signal Descriptions”
1.2	2020-07-20	AEM	• Updated the link for power supply implementation guidelines in section 5.1.11 “Power Control” • Added information about the congatec MLF file to section 10 “BIOS Setup Description” • Deleted section 11 “Industry Specifications”
1.3	2020-09-02	AEM	• Updated tables 2 “Commercial Variants” and 3 “Industrial Variants” • Added note about the 10GBASE-KR fill order to section 5.1.4 “Gigabit Ethernet” • Deleted sections 7.1.1 “AHCI” and 7.1.5 “Intel 64 Architecture”; also rearranged section 7 “conga Tech Notes”
1.4	2021-08-02	AEM	• Added Software License Information • Changed congatec AG to congatec GmbH • Updated section 6.4 “congatec Battery Management Interface”
1.5	2022-07-11	AEM	• Added section 1.3 “Supported 10 GbE Configurations”

Preface

This user's guide provides information about the components, features, connectors and BIOS setup menus available on the conga-B7AC. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec GmbH website at www.congatec.com

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Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
Gbps	Gigabit per second
Mbps	Megabit per second
MTps	Megatransfer per second
kHz	Kilohertz
MHz	Megahertz
10GBASE	10 Gbit Ethernet
2500BASE	2.5 Gbit Ethernet
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PEG	PCI Express Graphics
KR	GBASE-KR Ethernet Interface
KX	GBASE-KX Ethernet Interface
PCH	Platform Controller Hub
SM	System Management
BMC	Baseboard Management Controller
N.C	Not connected
N.A	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

1.1 COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express™ modules are available in following form factors:

- Mini 84mm x 55mm
- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

Table 1 COM Express™ 3.0 Pinout Types

Types	Connector Rows	PCIe Lanes	PCI	IDE	SATA Ports	LAN ports	USB 2.0/ USB 3.0	Display Interfaces
Type 1	A-B	Up to 6		-	4	1	8 / 0	VGA, LVDS
Type 2	A-B C-D	Up to 22	32 bit	1	4	1	8 / 0	VGA, LVDS, PEG/SDVO
Type 3	A-B C-D	Up to 22	32 bit	-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 4	A-B C-D	Up to 32		1	4	1	8 / 0	VGA,LVDS, PEG/SDVO
Type 5	A-B C-D	Up to 32		-	4	3	8 / 0	VGA,LVDS, PEG/SDVO
Type 6	A-B C-D	Up to 24		-	4	1	8 / 4 [1]	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32		-	2	5 (1x 1 GbE, 4x 10 GbE)	4/ 4 [1]	-
Type 10	A-B	Up to 4		-	2	1	8 / 2	LVDS/eDP, 1xDDI

[1] *The SuperSpeed USB ports (USB 3.0) are not in addition to the USB 2.0 ports. Up to 4 of the USB 2.0 ports can support SuperSpeed USB.*

The conga-B7AC modules use the Type 7 pinout definition and comply with COM Express 3.0 specification. They are equipped with two high performance connectors that ensure stable data throughput, and support high bandwidth networking.

The COM (computer on module) integrates all the core components of a common PC and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and they provide most of the functional requirements for any embedded PC application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 3.0/2.0, and 10 Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™

modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-B7AC is currently available in nine variants (six commercial and three industrial). The table below shows the different configurations available.

Table 2 Commercial Variants

Part No.		048200	048201	048202	048203	048204	048205
Processor		Intel® Atom® C3958 2.0 GHz 16 Cores	Intel® Atom® C3858 2.0 GHz 12 Cores	Intel® Atom® C3758 2.2 GHz 8 Cores	Intel® Atom® C3558 2.2 GHz 4 Cores	Intel® Atom® C3538 2.1 GHz 4 Cores	Intel® Atom® C3308 1.6 GHz 2 Cores
Turbo Mode		N.A	N.A	N.A	N.A	N.A	2.1 GHz
Intel® Smart Cache		16 MB	12 MB	16 MB	8 MB	8 MB	4 MB
Processor Graphics		None	None	None	None	None	None
DDR4 Memory (ECC or Non-ECC)		2400 MTps dual channel (up to 96 GB)	2400 MTps dual channel (up to 96 GB)	2400 MTps dual channel (up to 96 GB)	2133 MTps dual channel (up to 96 GB)	2133 MTps dual channel (up to 96 GB)	1866 MTps single channel (up to 64 GB)
Gigabit Ethernet		4 x 10GBASE-KR 1 x 1 GbE	4 x 10GBASE-KR 1 x 1 GbE	4 x 10GBASE-KR 1 x 1 GbE	2 x 10GBASE-KR (LAN0–1) 2 x 2500BASE-X (LAN2–3) 1 x 1 GbE	2 x 10GBASE-KR (LAN0–1) 2 x 2500BASE-X [4] (LAN2–3) 1 x 1 GbE	4 x 2500BASE-X [4] (LAN0–3) 1 x 1 GbE
SATA (6 Gbps)		2	2	2	2	2	1
PCIe Lanes	Gen 3	12 lanes	12 lanes	12 lanes	4 lanes	4 lanes	N.A
	Gen 2 [1,2,3]	7 lanes	7 lanes	7 lanes	7 lanes	7 lanes	8 lanes
USB Ports		4 ports (2 x USB 3.0)	4 ports (2 x USB 3.0)	4 ports (2 x USB 3.0)	4 ports (2 x USB 3.0)	4 ports (2 x USB 3.0)	4 ports (1 x USB 3.0)
eMMC		Optional	Optional	Optional	Optional	Optional	Optional
TPM 2.0		Discrete	Discrete	Discrete	Discrete	Discrete	Discrete
Processor TDP		31 W	25 W	25 W	16 W	15 W	9.5 W

Note

1. *PCIe Gen 2 lanes via an onboard PCIe switch.*
2. *COM Express PCIe lane 7 is shared with the 1 GbE.*
3. *Eight PCIe Gen 2 lanes if you disable the 1 gigabit Ethernet via the BIOS setup menu.*
4. *The 2500BASE-X interface is not an IEEE standard.*

Table 3 Industrial Variants

Part-No.		048210	048211	048213
Processor		Intel® Atom® C3808 2.0 GHz 12 Cores	Intel® Atom® C3708 1.7 GHz 8 Cores	Intel® Atom® C3508 1.6 GHz 4 Cores
Turbo Mode		N.A	N.A	N.A
Intel® Smart Cache		12 MB	16 MB	8 MB
Processor Graphics		None	None	None
DDR4 Memory (ECC or Non-ECC)		2133 MT/s dual channel (up to 96 GB)	2133 MT/s dual channel (up to 96 GB)	1866 MT/s dual channel (up to 96 GB)
Gigabit Ethernet		4 x 10GBASE-KR 1 x 1 GbE	4 x 10GBASE-KR 1 x 1 GbE	4 x 2500BASE-X [4] (LAN0–3) 1 x 1 GbE
SATA Ports (6 Gbps)		2	2	2
PCIe Lanes	Gen 3	12 lanes	12 lanes	0 lane
	Gen 2 [1,2,3]	7 lanes	7 lanes	7 lanes
USB Ports		4 ports (2 x USB 3.0)	4 ports (2 x USB 3.0)	4 ports (2 x USB 3.0)
eMMC		Optional	Optional	Optional
TPM 2.0		Discrete	Discrete	Discrete
Processor TDP		24 W	17 W	11.5 W

Note

1. *PCIe Gen 2 lanes via an onboard PCIe switch.*
2. *COM Express PCIe lane 7 is shared with the 1 gigabit Ethernet interface.*
3. *Eight PCIe Gen 2 lanes if you disable the 1 gigabit Ethernet via the BIOS setup menu.*
4. *The 2500BASE-X interface is not an IEEE standard.*

1.3 Supported 10 GbE Configurations

The table below lists the 10 GbE configurations the conga-B7AC supports.

Table 4 Supported 10 GbE configurations

Configurations	conga-B7AC
10GBASE-KR	Supported [1, 2]
Native SFI	Supported [1,2]
Inphi CS4227 - SFI	Supported [1,4]
Intel X557 - 10G-BASE-T	Supported [1,2]
Marvell 88X3310P - 10G-BASE-T	Not supported
Marvell 88E6190 2500BASE-KX	Supported [1, 2, 3]

Note

1. *Appropriate NVM image must be used. For instructions on how to deploy 10GbE LAN NVM and PHY NVM images, refer to congatec CTN 20180726 001 document in the restricted area of our website*
2. *Not validated by congatec*
3. *Not available on all variants. Refer to the product's User's Guide for more information*
4. *Default image on conga-B7AC*

2 Specifications

2.1 Feature List

Table 5 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 7, rev. 3.0 (Basic size 125 x 95 mm)
Processor	Intel® Atom® processor C-3000 product family
Memory	Three memory sockets (two stacked on the top side and one on the bottom side). Supports - DDR4 ECC and non-ECC SODIMM modules - Dual channel (channel 0, DIMM 0 on the bottom side; channel 0, DIMM 1 (upper slot) and channel 1, DIMM 0 (lower slot) on the top side) - Data rates up to 2400 MT/s - Maximum 96 GB capacity (32 GB per slot) **NOTE**: 1 *Post code "19" indicates that no memory module is detected.* 2 *See section 7.3 "DDR4 Memory" for more information.*
congatec Board Controller	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I2C bus, power loss control
Chipset	Integrated in the SoC
Ethernet	Gigabit Ethernet. Supports up to: - 4 x 10GBASE-KR [1] - 4 x 2500BASE-X [1, 2, 3] - 1 x 1 GbE (standard interface) **NOTE**: 1 *Some designs may require a 10 GbE PHY or 2.5 GbE switch on the carrier board.* 2 *The 2500BASE-X interface is not an IEEE standard.* 3 *Available on specific variants only. See section 1.2 "Options Information" for more information.*
Audio	N.A
Graphics	N.A
Peripheral Interfaces	USB Interfaces: - 4 USB ports (2 x USB 3.0) Buses - LPC (no DMA) - I²C (fast mode, 400 KHz, multi-master) - SMBus - SPI 2x SATA® (6Gb/s) PCIe Interfaces - Up to 12 x PCIe Gen. 3 lanes - 8 x PCIe Gen. 2 lanes 2x UART GPIOs
BIOS	AMI Aptio® V UEFI 2.x firmware, 16 MB SPI with congatec Embedded BIOS features.
Onboard Storage	Optional 32 GB eMMC (assembly option)

Power Management	Supports: - ACPI Specification Version 5.0 (Errata A), compliant with battery support. - Hardware power management - System Sleep State Control - Wake events from the Intel Management Engine
Security	Discrete LPC TPM 2.0 (Infineon SLB9665XT2.0); new AES Instructions for faster and better encryption.

Note

Some of the features mentioned above are optional. Check the part number of your module and compare it to the Options Information tables on pages 11 and 12 to determine what options are available on your particular module.

2.2 Supported Operating Systems

The conga-B7AC supports the following operating systems.

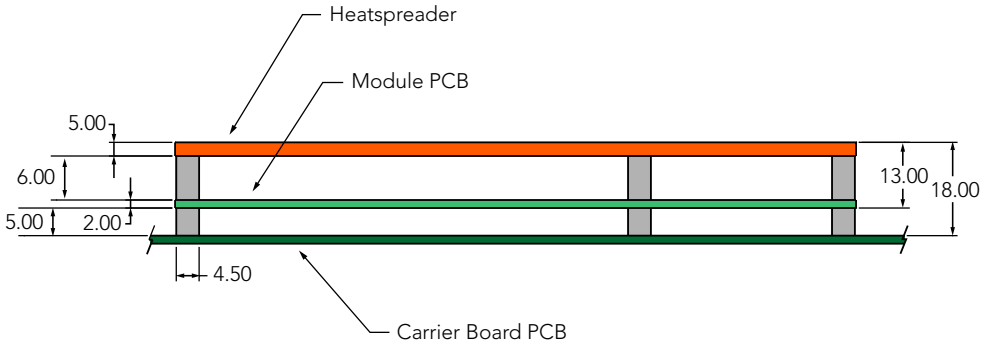
- Microsoft® Windows® Server 2012 R2 and 2016 (64-bit)
- Red Hat Enterprise Linux Server 7.2 and 7.3
- SuSE Linux Enterprise Server 12 SP1
- Fedora 23 and 24
- Ubuntu 16.04 LTS
- CentOS 7.2
- VMware ESXi 6.0
- Hyper-V (virtualized Microsoft Windows Server)
- Linux KVM 6.8 and 7.3

Note

For better system performance, use only 64-bit Operating Systems.

2.3 Mechanical Dimensions

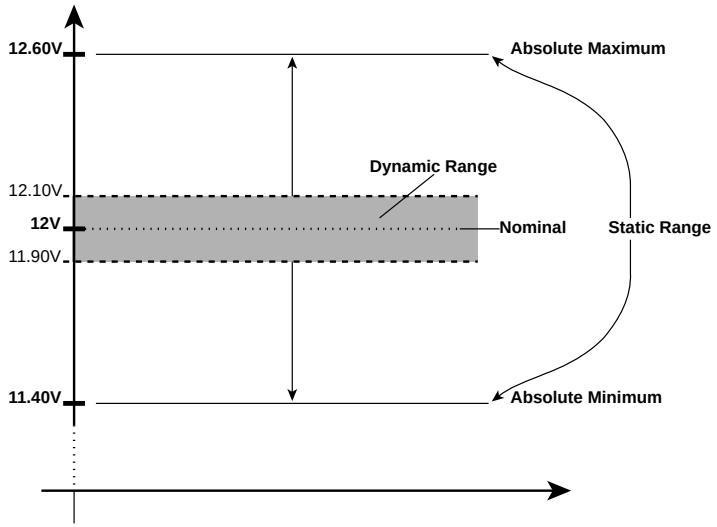
- 95.0 mm x 125.0 mm
- Height approximately 18 or 21 mm (including heatspreader) depending on the carrier board connector that is used. If the 5 mm (height) carrier board connector is used, then approximate overall height is 18 mm. If the 8 mm (height) carrier board connector is used, then approximate overall height is 21 mm



2.4 Supply Voltage Standard Power

- 12 V DC ± 5 %

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 7 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Ampere)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (with derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4 – 12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75 – 5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5 – 3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +12 V
- conga-B7AC COM
- modified congatec carrier board
- conga-B7AC cooling solution
- Microsoft Windows Server 2016 (64 bit)

Note

The CPU was stressed to its maximum workload.

Table 6 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S5	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*

2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 7 Power Consumption Values

The table below provides additional information about the conga-B7AC power consumption. The values are recorded at various operating mode.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64 bit)	CPU			Current (A)			
					Variant	Cores	Freq. /Max. Turbo (GHz)	S0: Min	S0: Max	S0: Peak	S5
048200	3 x 4 GB	B.0	R008	Windows 10	Intel® Atom® C3958	16	2.0 / N.A	1.04	2.55	2.58	N.A
048201	3 x 4 GB	B.0	R008	Windows 10	Intel® Atom® C3858	12	2.0 / N.A	1.06	2.27	2.30	N.A
048202	3 x 4 GB	B.0	R008	Windows 10	Intel® Atom® C3758	8	2.2 / N.A	1.04	2.04	2.05	N.A
048203	3 x 4 GB	B.0	R008	Windows 10	Intel® Atom® C3558	4	2.2 / N.A	0.98	1.38	1.41	N.A
048204	3 x 4 GB	B.0	R009	Windows 10	Intel® Atom® C3538	4	2.1 / N.A	1.02	1.44	1.46	N.A
048205	2 x 4 GB	B.0	R009	Windows 10	Intel® Atom® C3308	2	1.6 / 2.1	0.89	1.06	1.08	N.A
048210	3 x 4 GB	B.0	R009	Windows 10	Intel® Atom® C3808	12	2.0 / N.A	1.00	2.22	2.25	N.A
048211	3 x 4 GB	B.0	R009	Windows 10	Intel® Atom® C3708	8	1.7 / N.A	1.03	1.59	1.62	N.A
048213	3 x 4 GB	B.0	R009	Windows 10	Intel® Atom® C3508	4	1.5 / N.A	1.00	1.25	1.26	N.A

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	1.83 µA
20°C	3V DC	2.05 µA
70°C	3V DC	3.62 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-B7AC.*

2.7 Environmental Specifications

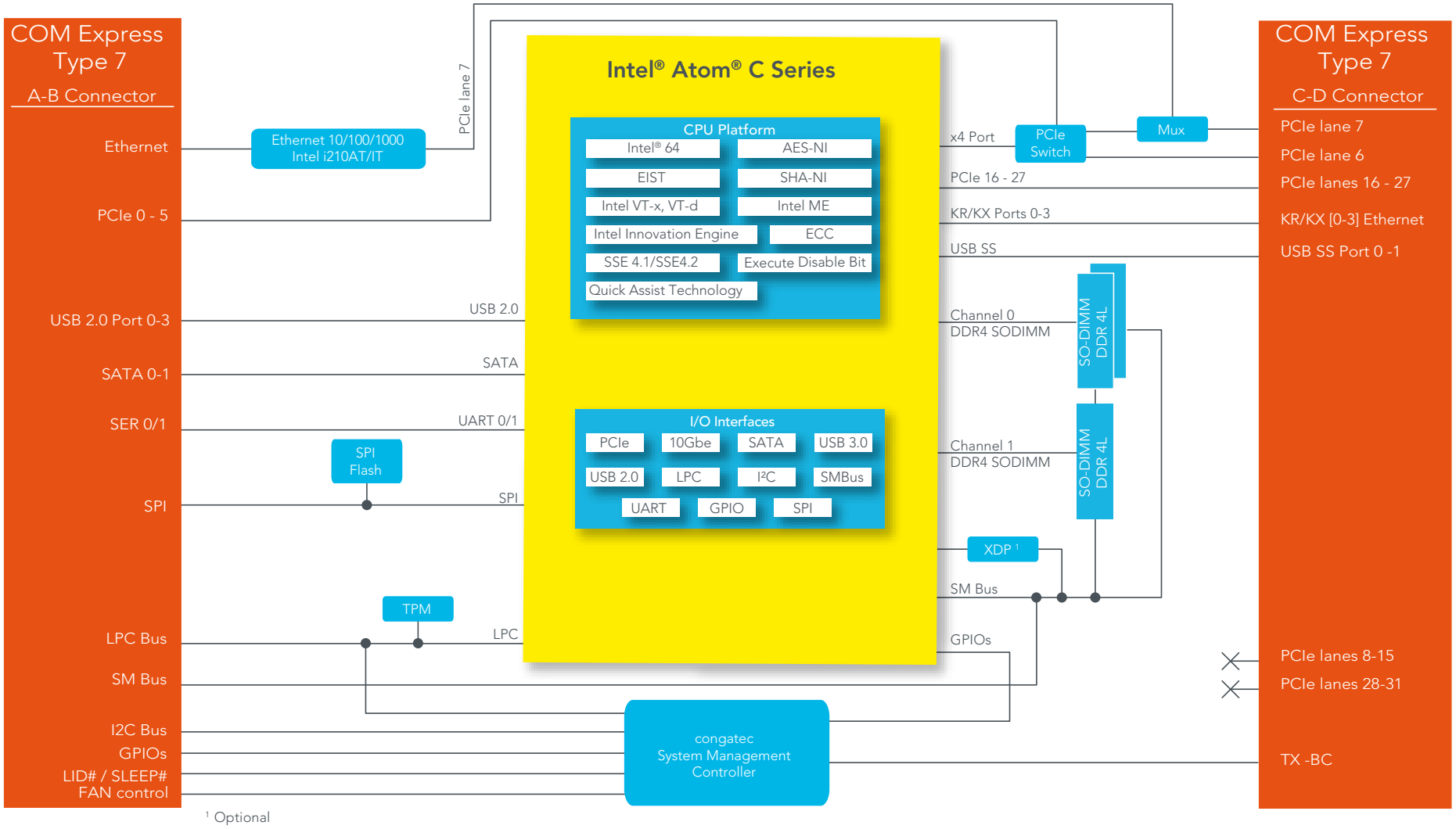
Temperature	Operation: 0° to 60°C	Storage: -20° to 80°C (commercial variants)
Temperature	Operation: -40° to 85°C	Storage: -40° to 85°C (industrial variants)
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-B7AC. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

	Cooling Solution	Part No.	Description
1	HSP	048251	Heatspreader with integrated copper plate and 2.7 mm bore-hole standoffs
		048252	Heatspreader with integrated copper plate and M2.5 mm threaded standoffs
2	CSA	048253	Active cooling solution with integrated copper plate and 2.7 mm bore-hole standoffs
		048254	Active cooling solution with integrated copper plate and M2.5 mm threaded standoffs
3	CSP	048255	Passive cooling solution with integrated copper plate and 2.7 mm bore-hole standoffs
		048256	Passive cooling solution with integrated copper plate and M2.5 mm threaded standoffs

Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*

2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*

Caution

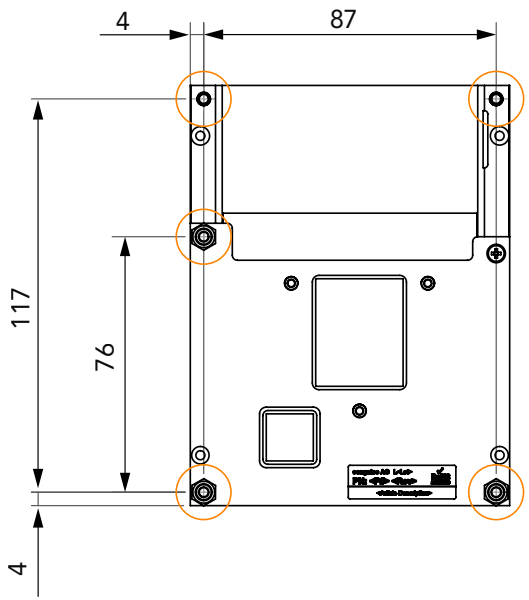
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

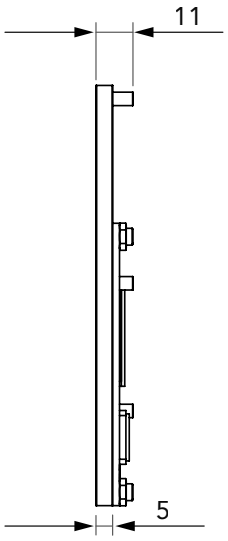
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

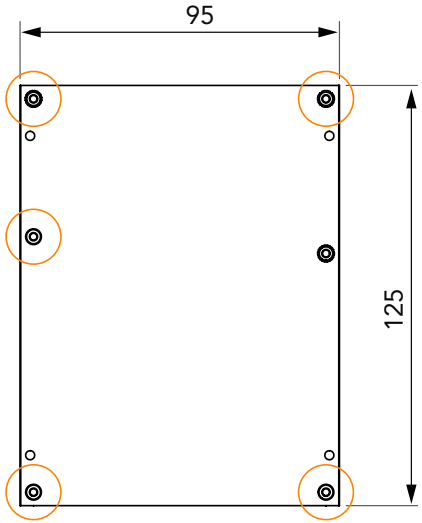
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

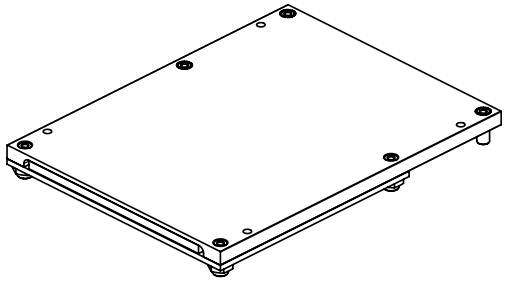
4.1 HSP Dimensions

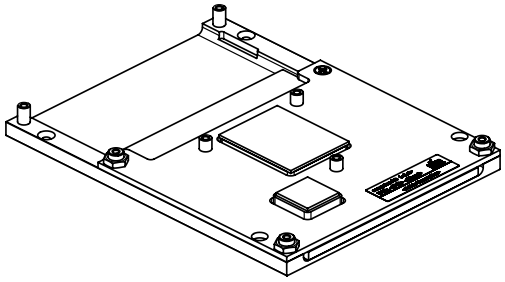




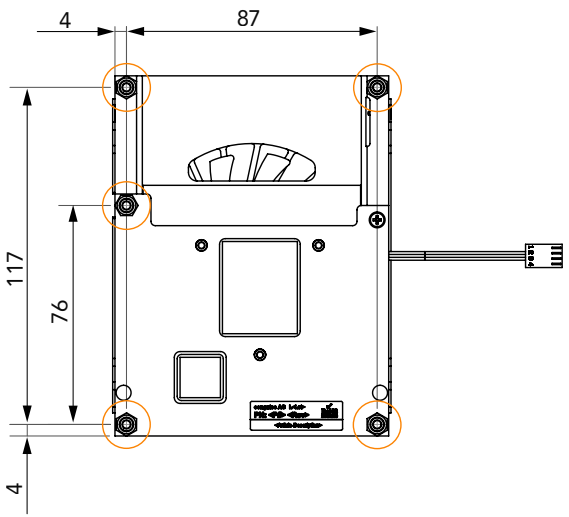


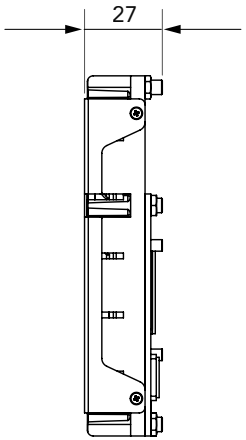
M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

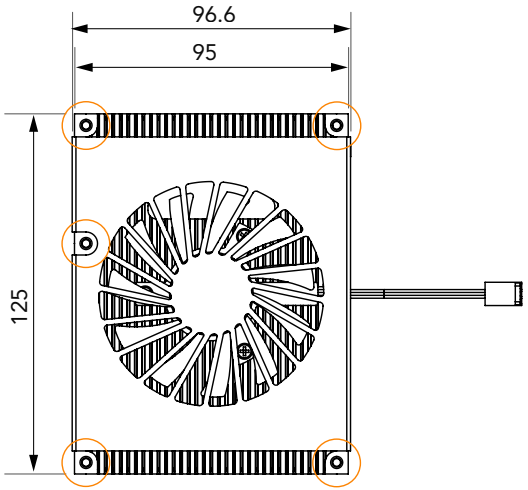


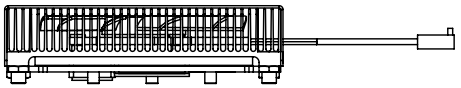


4.2 CSA Dimensions









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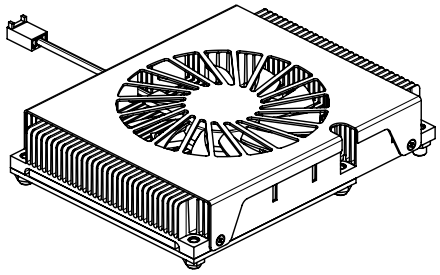
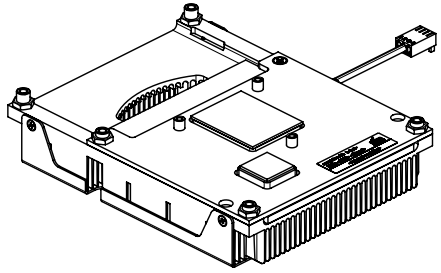
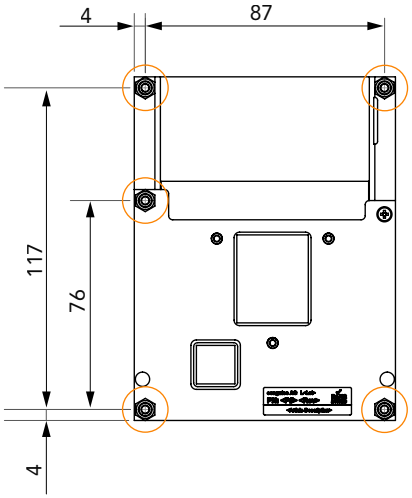
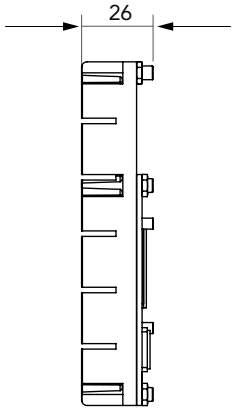
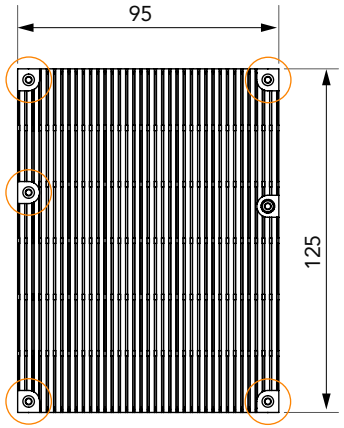


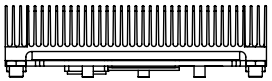


4.3 CSP Dimension









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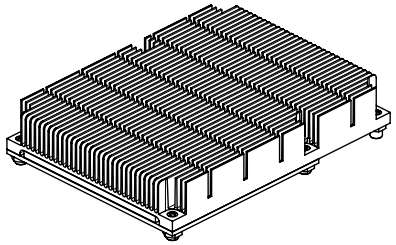
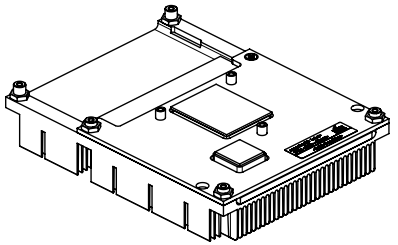




5 Connector Rows

The conga-B7AC is connected to the carrier board via two 220-pin connectors (COM Express Type 7 pinout). These connectors are broken down into four rows. The primary connector consists of rows A - B while the secondary connector consists of rows C–D.

5.1 Primary and Secondary Connector Rows

The following subsystems can be found on the primary and secondary connector rows.

Table 10 Supported Interfaces on Rows A–B and C–D

Interfaces	Rows A–B	Rows C–D
SATA	2	-
USB 2.0	4	-
USB 3.0	-	2
Gigabit Ethernet	1x 1 Gbps	Up to 4 x 10GBASE-KR [1]
PCIe Gen 2	6 lanes	1 lane [2]
PCIe Gen 3	-	Up to 12 lanes
UART	2	-
Buses	SPI, LPC, SMB, I2C	-
congatec System Mgmt.	GPIOs, Fan control, LID#/SLEEP#	-

Note

1. *Some variants have different configurations. See section 1.2 "Options Information" for more information.*
2. *Two lanes if you disable the on-module 1 gigabit Ethernet via the BIOS setup menu.*

5.1.1 Serial ATA™ (SATA)

Table 11 SATA Features

Rows A–B	Rows C–D
Two SATA interfaces with support for - independent DMA operation - data transfer rates up to 6.0 Gbps - RAID and AHCI modes - Serial GPIO (SFF 8485 specification)	None

Note

The interface does not support legacy and native IDE modes.

5.1.2 USB Interface

Table 12 USB Features

Rows A–B	Rows C–D
Four USB 2.0 ports: - ports 0 and 1 can be combined with USB SuperSpeed signals to create USB 3.0 ports - supports data transfers up to 480 Mbps - features single combo controller for USB 2.0/3.0 - supports USB 1.x and USB 2.0 compliant devices	Two USB 3.0 SuperSpeed Tx/Rx differential signals: - each port requires corresponding USB 2.0 differential pairs - supports data transfers up to 5 Gbps - features single combo controller for USB 3.0/2.0 - supports debug capability on either USB 3.0 port

5.1.3 PCI Express™

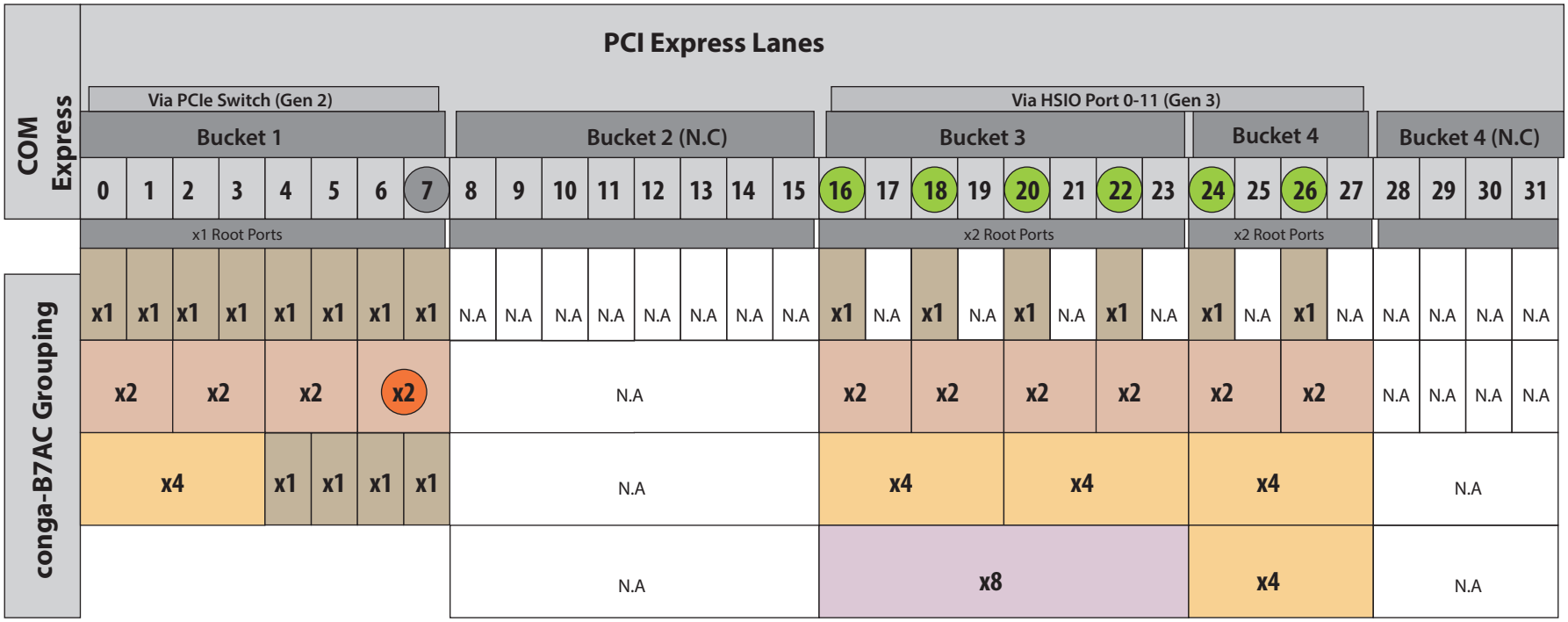
Table 13 PCI Express Features

Rows A–B	Rows C–D
Six PCIe lanes: - no Gen. 3 lanes - six Gen. 2 lanes (0 - 5) with up to 5 GTps - x1 root port with Gen 2 PCIe Switch - maximum 8 x1 downstream PCIe 2.0 ports [3] - possible configuration [3] is 8 x1, 4 x2 and 1 x4 + 4 x1 lane	14 PCIe lanes: - up to 12 Gen. 3 lanes (16 - 27) with up to 8 GTps - up to two Gen. 2 lanes (6 - 7) [1,2] with up to 5 GTps - x2 root ports for Gen 3 lanes

Note

1. *COM Express lane 7 is shared with 1 gigabit Ethernet via a multiplexer. The shared lane is routed to the 1 GbE interface by default.*
2. *To route the shared lane to COM Express lane 7, open the BIOS setup menu and change the default setting via the Advanced -> Module PCIe Configuration submenu.*
3. *Applies to Gen. 2 lanes in both A–B and C–D rows (possible only if 1 gigabit Ethernet interface is disabled).*

5.1.3.1 PCIe Routing



x1 Port

N.A — Not available if the corresponding x1 link is used

7 — PCIe lane 7 is not available if the 1 Gigabit Ethernet is enabled

x2 — 4 x2 link is available only if you disable the 1 gigabit Ethernet

5.1.4 Gigabit Ethernet

Table 14 Gigabit Ethernet Features

Rows A–B	Rows C–D
One 1 GbE [1, 2] interface. Supports: - MDI interface - full-duplex operation at 10/100/1000 Mbps - half-duplex operation at 10/100 Mbps - IEEE 802.3x flow control specification	Up to four LAN controllers [3,5]. Supports: - 10GBASE-KR or 2500BASE-X [4] backplane interfaces, depending on SKU - full-duplex operation at all supported speeds - NC-SI, SMBus and MDIO management interfaces

Note

1. *COM Express PCIe lane 7 is shared with 1 gigabit Ethernet via a multiplexer. The shared lane is routed to the 1 GbE interface by default.*
2. *To route the shared lane to COM Express PCIe lane 7, open the BIOS setup menu and change the default setting in the Advanced -> Module PCIe Configuration submenu.*
3. *No support for half duplex at 10 Mb, 100 Mb, 1 Gb, 2.5 Gb or 10 Gb.*
4. *Available on specific variants only.*
5. *The feature fill order for 10GBASE-KR ports is from low to high.*

5.1.5 General Purpose Serial Interface (UART)

Rows A–B	Rows C–D
Two UART interfaces with support for - low, full and high speed modes - programmable baud rates from 300 bps up to 3.6864 Mbps - legacy or enhanced operating modes - auto-Baud and auto flow control in enhanced operating mode	None

Note

Hardware handshake is not supported.

5.1.6 LPC Bus

The conga-B7AC offers the LPC bus through the integrated PCH. A TPM 2.0 compliant module is connected to the LPC bus.

Note

The LPC bus does not support DMA devices.

5.1.7 I²C Bus

The I²C bus is implemented through the congatec Board Controller, and accessed through the congatec CGOS driver and API. The controller provides a fast-mode multi-master I²C bus that has the maximum bandwidth.

5.1.8 SPI Bus

The conga-B7AC offers the SPI bus for SPI-compatible flash devices. By integrating an off-module flash device (BIOS) on the carrier board, you can boot the conga-B7AC from the carrier board. This is especially useful when evaluating a customized BIOS.

5.1.9 SMBus

The conga-B7AC offers the SM bus for communicating and managing system devices such as thermal sensors, PCIe devices, RAM's serial presence detect.

Note

Make sure the address space of the carrier board SM bus devices does not overlap with the address space of the module devices. For more information, see the COM Express Specification.

5.1.10 GPIOs

The conga-B7AC offers four General Purpose Input signals and four General Purpose Output signals on the A–B connector.

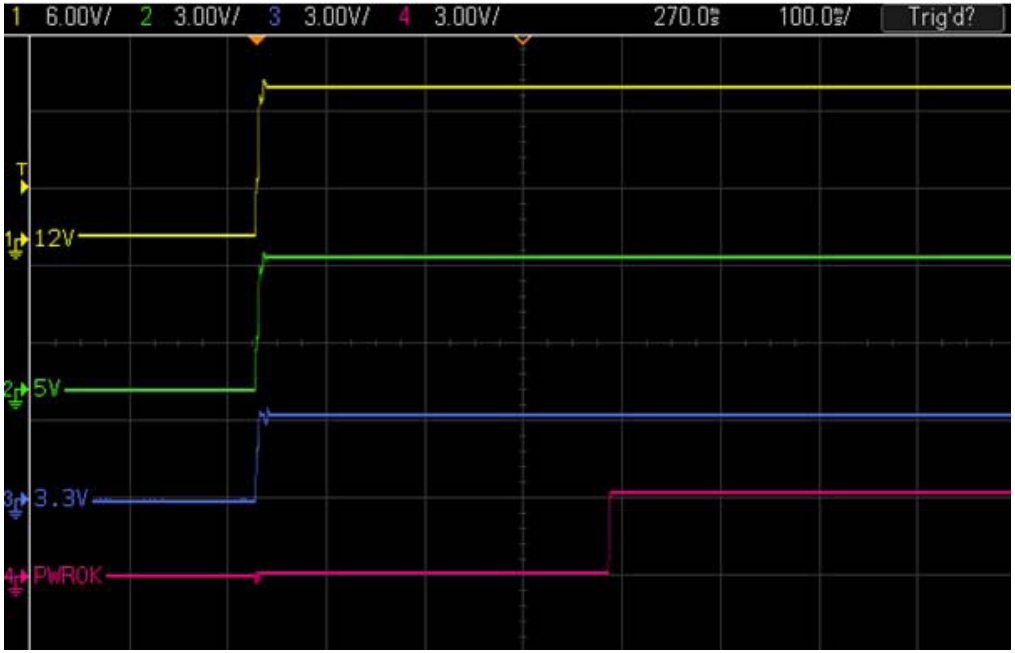
5.1.11 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

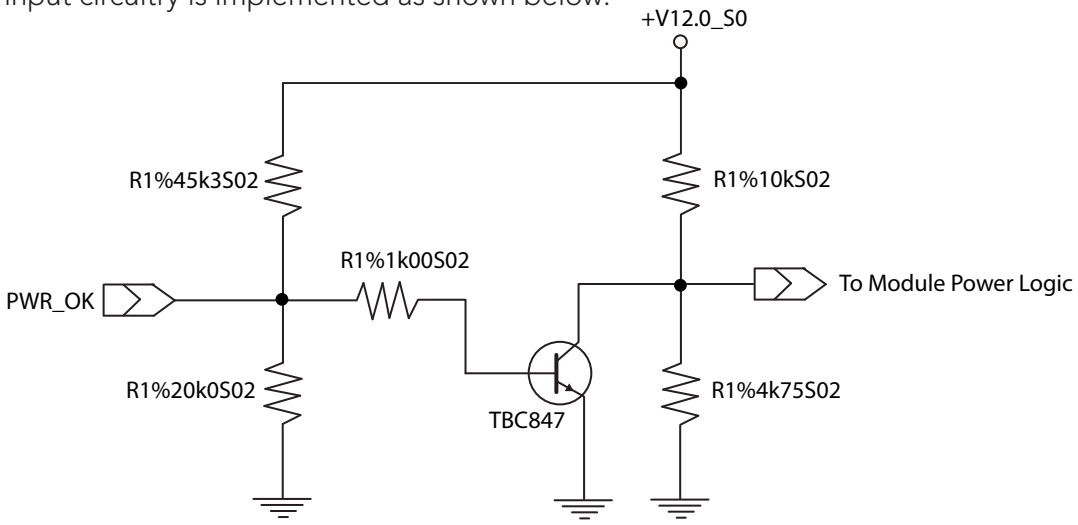
A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-B7AC PWR_OK input circuitry is implemented as shown below:



The voltage divider ensures the input complies with 3.3 V CMOS characteristic. It also makes it possible to use the module on carrier board designs that do not use the PWR_OK signal. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

When considering the above shown voltage divider circuitry and the transistor stage, the voltage measured at the PWR_OK input pin may be only around 0.8 V when the 12 V is applied to the module. Actively driving PWR_OK high is compliant to the COM Express specification but this can cause back driving. Therefore, congatec recommends driving the PWR_OK low to keep the module in reset and tri-state PWR_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1 k resistor to the carrier board 3.3 V power rail.

Note

1. *With this solution, make sure that before the 3.3 V goes up, all carrier board hardware is fully powered and all clocks are stable.*

2. *The conga-B7AC supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-B7AC pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# on the conga-B7AC.*

SUS_S3#

The SUS_S3# (pin A15 on the A–B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this, the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

Note

The SUS_S3# signal may be used to enable ATX power supply, but it does not initiate a "Suspend-to-RAM" state.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A–B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Standard 12V Power Supply Implementation Guidelines

The 12 volt input power is the sole operational power source for the conga-B7AC. Other required voltages are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-B7AC application, be aware that the system may malfunction when a 12V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

The cause of this problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualication phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

5.1.12 Power Management

ACPI

The conga-B7AC supports Advanced Configuration and Power Interface (ACPI) specification, revision 5.0 (Errata A). For more information, see section 7.2 “ACPI Suspend Modes and Resume Events”.

6 Additional Features

6.1 eMMC

The conga-B7AC offers an optional eMMC flash onboard. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology.

The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions."

6.2 congatec Board Controller (cBC)

The conga-B7AC is equipped with Texas Instruments Tiva™ microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 General Purpose Input/Output

The conga-B7AC offers general purpose inputs and outputs for custom system design. These GPIOs are controlled by the cBC.

6.2.3 Watchdog

The conga-B7AC is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-B7AC module does not support watchdog NMI mode.

6.2.4 I²C Bus

The conga-B7AC supports I²C bus. Thanks to the I²C host controller in the cBC, the I²C bus is multi-master capable and runs at fast mode.

6.2.5 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

AC power loss condition occurs when the module loses the standby voltage on the 5V_SB pins. On congatec moduless, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, the module considers this an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.

Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.

6.2.6 Fan Control

The conga-B7AC has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *A four wire fan must be used to generate the correct speed readout.*

2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express Design Guide.*

6.3 OEM BIOS Customization

The conga-B7AC is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below.

6.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.3.4 OEM BIOS Code/Data

With the congatec embedded BIOS, system designers can add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.

Except for custom specific code, this feature can also be used to support Windows 7, Windows 8 OEM activation (OA3.0), verb tables for HDA codecs, PCI/PCIe OpROMs, bootloaders, rare graphic modes and Super I/O controller initialization.

Note

The OEM BIOS code of the new UEFI based firmware is called only when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. Contact congatec technical support for more information on how to add OEM code.

6.3.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-B7AC BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

6.5 API Support (CGOS)

To benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win64, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

6.6 Security Features

The conga-B7AC offers a discrete LPC TPM 2.0 (Infineon SLB9665XT2.0) by default. To use the discrete TPM, ensure that the firmware-based TPM is disabled in the BIOS setup menu via the *Advanced -> Platform Trust Technology -> fTPM*. Save the changes and exit to complete the system configuration changes.

6.7 Suspend to Ram

The conga-B7AC does not support Suspend to RAM feature.

7 conga Tech Notes

The conga-B7AC has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 Intel® Denventon Features

Some of the features the Intel Denventon SoC supports are:

7.1.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software drivers, or operating system support is not required.

Note

1. *Use a properly designed thermal solution for adequate heat dissipation. This solution ensures the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum. The Intel® processor's respective datasheet can provide you with more information about this subject.*

2. *To enable THERMTRIP# to switch off the system automatically, use an ATX style power supply.*

7.1.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits. Intel® Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state. The maximum frequency of Intel® Turbo Boost Technology is dependent on the number of active cores.

The amount of time the processor spends in the Intel Turbo Boost 2 Technology state depends on the workload and operating environment. Any of the following can set the upper limit of Intel® Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 100 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached. For more information about Intel® Turbo Boost 2 Technology visit the Intel® website.

Note

1. *Some variants do not support turbo boost.*

2. *Refer to section 2.5 "Power Consumption" for information about the maximum turbo frequency available for each conga-B7AC variant.*

7.1.3 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

The Intel VT supports RTS Real-Time Hypervisor which has been verified on all current congatec x86 hardware.

Note

congatec supports only RTS Hypervisor. For more information, contact congatec technical support.

7.1.4 Processor Performance Control

The Intel® processors found on the conga-B7AC run at different voltage/frequency states (performance states)—referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully used. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting. You must ensure that the power scheme setting you choose has the ability to support Enhanced Intel® SpeedStep® technology.

7.2 ACPI Suspend Modes and Resume Events

The conga-B7AC BIOS does not support Suspend to RAM (S3). Suspend to Disk (S4) is however supported. The table below lists the events that wake the system from S4.

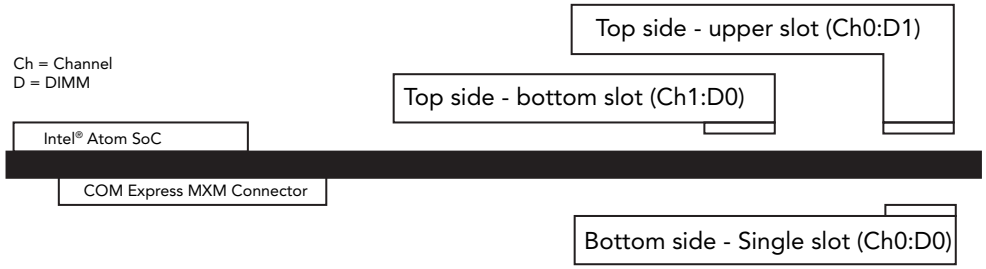
Table 15 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S4-S5
Onboard LAN Event	Device driver must be configured for Wake On LAN support
PCI Express WAKE#	Wakes unconditionally from S4-S5
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device or enable 'Resume On PME#' in the Power setup menu
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Wakes unconditionally from S4-S5
Watchdog Power Button Event	Wakes unconditionally from S4-S5

7.3 DDR4 Memory

The Intel Denventon SoC featured on the conga-B7AC supports ECC and non-ECC DDR4 memory modules, up to 2400 MT/s. The DDR4 memory modules have lower voltage requirements with higher data rate transfer speeds. They operate at a nominal voltage of 1.2 V. With this low voltage system memory interface on the processor, the conga-B7AC offers a system optimized for lowest possible power consumption. The reduction in power consumption due to lower voltage subsequently reduces the heat generated.

The diagram below shows the location of the memory slots on the conga-B7AC.



The following population rules must be observed:

- Populate either channel or both
- No DIMM matching requirements between channels
- Each channel may run at different DIMM timings

Note

Post code "19" indicates that no memory module is detected.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on the conga-B7AC. The pinout of the module complies with COM Express Type 7, rev. 3.0.

The table below describes the terminology used in this section. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors; only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 16 Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
T	Higher voltage tolerance
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0 and 3.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0
REF	Reference voltage output. May be sourced from a module power plane
KR	10GBASE-KR compatible signal
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board

8.1 Connector Signal Descriptions

Table 17 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# [1]	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# [1]	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1# [2]
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF [1]	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	PCIE_TX8+ [1]	B71	PCIE_RX8+ [1]
A17	SATA0_TX-	B17	SATA1_TX-	A72	PCIE_TX8- [1]	B72	PCIE_RX8- [1]
A18	SUS_S4#	B18	SUS_STAT#	A73	GND	B73	GND
A19	SATA0_RX+	B19	SATA1_RX+	A74	PCIE_TX9+ [1]	B74	PCIE_RX9+ [1]
A20	SATA0_RX-	B20	SATA1_RX-	A75	PCIE_TX9- [1]	B75	PCIE_RX9- [1]
A21	GND (FIXED)	B21	GND (FIXED)	A76	GND	B76	GND
A22	PCIE_TX15+ [1]	B22	PCIE_RX15+ [1]	A77	PCIE_TX10+ [1]	B77	PCIE_RX10+ [1]
A23	PCIE_TX15- [1]	B23	PCIE_RX15- [1]	A78	PCIE_TX10- [1]	B78	PCIE_RX10- [1]
A24	SUS_S5#	B24	PWR_OK	A79	GND	B79	GND
A25	PCIE_TX14+ [1]	B25	PCIE_RX14+ [1]	A80	GND (FIXED)	B80	GND (FIXED)
A26	PCIE_TX14- [1]	B26	PCIE_RX14- [1]	A81	PCIE_TX11+ [1]	B81	PCIE_RX11+ [1]
A27	BATLOW#	B27	WDT	A82	PCIE_TX11- [1]	B82	PCIE_RX11- [1]
A28	(S)ATA_ACT#	B28	RSVD [1]	A83	GND	B83	GND
A29	RSVD [1]	B29	RSVD [1]	A84	NCSI_TX_EN	B84	VCC_5V_SBY
A30	RSVD [1]	B30	RSVD [1]	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD [1]	B86	VCC_5V_SBY
A32	RSVD [1]	B32	SPKR [2]	A87	RSVD [1]	B87	VCC_5V_SBY
A33	RSVD [1]	B33	I2C_CK	A88	PCIE_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CK_REF-	B89	NCSI_RX_ER
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	PCIE_TX13+ [1]	B36	PCIE_RX13+ [1]	A91	SPI_POWER	B91	NCSI_CLK_IN
A37	PCIE_TX13- [1]	B37	PCIE_RX13- [1]	A92	SPI_MISO	B92	NCSI_RXD1
A38	GND	B38	GND	A93	GPO0	B93	NCSI_RXD0
A39	PCIE_TX12+ [1]	B39	PCIE_RX12+ [1]	A94	SPI_CLK	B94	NCSI_CRS_DV
A40	PCIE_TX12- [1]	B40	PCIE_RX12- [1]	A95	SPI_MOSI	B95	NCSI_TXD1
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	NCSI_TXD0
A42	USB2-	B42	USB3-	A97	TYPE10# [1]	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	NCSI_ARB_IN
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	NCSI_ARB_OUT
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# [1]	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD [1]	B48	USB0_HOST_PRSNT [1]	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

1. *Not connected.*
2. *Not supported*

Table 18 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PCIE_RX17-	D56	PCIE_TX17-
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PCIE_RX18+	D58	PCIE_TX18+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PCIE_RX18-	D59	PCIE_TX18-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PCIE_RX19+	D61	PCIE_TX19+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PCIE_RX19-	D62	PCIE_TX19-
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	USB_SSRX2- [1]	D9	USB_SSTX2- [1]	C64	RSVD	D64	RSVD
C10	USB_SSRX2+ [1]	D10	USB_SSTX2+ [1]	C65	PCIE_RX20+	D65	PCIE_TX20+
C11	GND(FIXED)	D11	GND (FIXED)	C66	PCIE_RX20-	D66	PCIE_TX20-
C12	USB_SSRX3- [1]	D12	USB_SSTX3- [1]	C67	RAPID_SHUTDOWN [2]	D67	GND
C13	USB_SSRX3+ [1]	D13	USB_SSTX3+ [1]	C68	PCIE_RX21+	D68	PCIE_TX21+
C14	GND	D14	GND	C69	PCIE_RX21-	D69	PCIE_TX21-
C15	10G_PHY_MDC_SCL3	D15	10G_PHY_MDIO_SDA3	C70	GND (FIXED)	D70	GND (FIXED)
C16	10G_PHY_MDC_SCL2	D16	10G_PHY_MDIO_SDA2	C71	PCIE_RX22+	D71	PCIE_TX22+
C17	10G_SDP2	D17	10G_SDP3	C72	PCIE_RX22-	D72	PCIE_TX22-
C18	GND	D18	GND	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PCIE_RX23+	D74	PCIE_TX23+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PCIE_RX23-	D75	PCIE_TX23-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD	D77	RSVD
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PCIE_RX24+	D78	PCIE_TX24+
C24	10G_INT2	D24	10G_INT3	C79	PCIE_RX24-	D79	PCIE_TX24-
C25	GND	D25	GND	C80	GND (FIXED)	D80	GND (FIXED)
C26	10G_KR_RX3+	D26	10G_KR_TX3+	C81	PCIE_RX25+	D81	PCIE_TX25+
C27	10G_KR_RX3-	D27	10G_KR_TX3-	C82	PCIE_RX25-	D82	PCIE_TX25-
C28	GND	D28	GND	C83	RSVD	D83	RSVD
C29	10G_KR_RX2+	D29	10G_KR_TX2+	C84	GND	D84	GND
C30	10G_KR_RX2-	D30	10G_KR_TX2-	C85	PCIE_RX26+	D85	PCIE_TX26+
C31	GND (FIXED)	D31	GND (FIXED)	C86	PCIE_RX26-	D86	PCIE_TX26-
C32	10G_SFP_SDA3 [1]	D32	10G_SFP_SCL3 [1]	C87	GND	D87	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C33	10G_SFP_SDA2	D33	10G_SFP_SCL2	C88	PCIE_RX27+	D88	PCIE_TX27+
C34	10G_PHY_RST_23	D34	10G_PHY_CAP_23	C89	PCIE_RX27-	D89	PCIE_TX27-
C35	10G_PHY_RST_01	D35	10G_PHY_CAP_01	C90	GND (FIXED)	D90	GND (FIXED)
C36	10G_LED_SDA	D36	RSVD [1]	C91	PCIE_RX28+ [1]	D91	PCIE_TX28+ [1]
C37	10G_LED_SCL	D37	RSVD [1]	C92	PCIE_RX28- [1]	D92	PCIE_TX28- [1]
C38	10G_SFP_SDA1	D38	10G_SFP_SCL1	C93	GND	D93	GND
C39	10G_SFP_SDA0	D39	10G_SFP_SCL0	C94	PCIE_RX29+ [1]	D94	PCIE_TX29+ [1]
C40	10G_SDP0	D40	10G_SDP1	C95	PCIE_RX29- [1]	D95	PCIE_TX29- [1]
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	10G_KR_RX1+	D42	10G_KR_TX1+	C97	RSVD	D97	RSVD
C43	10G_KR_RX1-	D43	10G_KR_TX1-	C98	PCIE_RX30+ [1]	D98	PCIE_TX30+ [1]
C44	GND	D44	GND	C99	PCIE_RX30- [1]	D99	PCIE_TX30- [1]
C45	10G_PHY_MDC_SCL1	D45	10G_PHY_MDIO_SDA1	C100	GND (FIXED)	D100	GND (FIXED)
C46	10G_PHY_MDC_SCL0	D46	10G_PHY_MDIO_SDA0	C101	PCIE_RX31+ [1]	D101	PCIE_TX31+ [1]
C47	10G_INT0	D47	10G_INT1	C102	PCIE_RX31- [1]	D102	PCIE_TX31- [1]
C48	GND	D48	GND	C103	GND	D103	GND
C49	10G_KR_RX0+	D49	10G_KR_TX0+	C104	VCC_12V	D104	VCC_12V
C50	10G_KR_RX0-	D50	10G_KR_TX0-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND(FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PCIE_RX16+	D52	PCIE_TX16+	C107	VCC_12V	D107	VCC_12V
C53	PCIE_RX16-	D53	PCIE_TX16-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	RSVD [1]	C109	VCC_12V	D109	VCC_12V
C55	PCIE_RX17+	D55	PCIE_TX17+	C110	GND (FIXED)	D110	GND (FIXED)

Note

1. *Not connected.*

2. *Not supported.*

Table 19 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		
			1000BASE-T	100BASE-TX	10BASE-T			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low				OD 3.3V		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low				OD 3.3V		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low				OD 3.3V		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low				OD 3.3V		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less				REF		Not connected
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 pps signal				I/O		

Table 20 NC-SI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
NCSI_CLK_IN	B91	NC-SI Clock reference for receive, transmit, and control interface	I 3.3V		
NCSI_RXD0 NCSI_RXD1	B93 B92	NC-SI Receive Data (from NC to BMC)	O 3.3V		
NCSI_TXD0 NCSI_TXD1	B96 B95	NC-SI Transmit Data (from BMC to NC)	I 3.3V		
NCSI_CRS_DV	B94	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid	O 3.3V		
NCSI_TX_EN	A84	NC-SI Transmit enable	I 3.3V		
NCSI_RX_ER	B89	NC-SI Receive error	O 3.3V		
NCSI_ARB_IN	B98	NC-SI hardware arbitration input	I 3.3V		
NCSI_ARB_OUT	B99	NC-SI hardware arbitration output	O 3.3V		

Table 21 10 Gigabit Ethernet Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
10G_KR_TX0+ 10G_KR_TX0-	D49 D50	10GBASE-KR ports, transmit output differential pairs 0	O KR		
10G_KR_RX0+ 10G_KR_RX0-	C49 C50	10GBASE-KR ports, receive input differential pairs 0	I KR		
10G_KR_TX1+ 10G_KR_TX1-	D42 D43	10GBASE-KR ports, transmit output differential pairs 1	O KR		
10G_KR_RX1+ 10G_KR_RX1-	C42 C43	10GBASE-KR ports, receive input differential pairs 1	I KR		
10G_KR_TX2+ 10G_KR_TX2-	D29 D30	10GBASE-KR ports, transmit output differential pairs 2	O KR		
10G_KR_RX2+ 10G_KR_RX2-	C29 C30	10GBASE-KR ports, receive input differential pairs 2	I KR		
10G_KR_TX3+ 10G_KR_TX3-	D26 D27	10GBASE-KR ports, transmit output differential pairs 3	O KR		
10G_KR_RX3+ 10G_KR_RX3-	C26 C27	10GBASE-KR ports, receive input differential pairs 3	I KR		
10G_PHY_MDIO_SDA[0:3]	D46 D45 D16 D15	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY	O 3.3V	PU 1K	
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY	I/O OD 3.3V	PU 1K	
10G_PHY_MDC_SCL[0:3]	C46 C45 C16 C15	MDIO Mode: Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY	O 3.3V	PU 1K	
		I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY	I/O OD 3.3V	PU 1K	
10G_PHY_CAP_01	D35	PHY mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module. Based on this input, the actual protocol used is indicated over the dedicated I²C interface	I 3.3V		Not connected
10G_PHY_CAP_23	D34	Phy mode capability pin: Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module. Based on this input, the actual protocol used is indicated over the dedicated I²C interface	I 3.3V		Not connected
10G_SFP_SDA[0:3]	C39 C38 C33 C32	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP module	I/O OD 3.3V	PU 4.7K	10G_SFP_SDA3 is not connected

10G_SFP_SCL[0:3]	D39 D38 D33 D32	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP module	I/O OD 3.3V	PU 4.7K	10G_SFP_SCL3 is not connected
10G_LED_SDA	C36	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs	I/O OD 3.3V	PU 2.2K	
10G_LED_SCL	C37	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs	I/O OD 3.3V	PU 2.2K	
10G_INT[0:3]	C47 D47 C24 D24	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I CMOS	PU 2.2K	
10G_SDP[0:3]	C40 D40 C17 D17	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O 3.3V		
10G_PHY_RST_01	C35	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used)	O 3.3V		
10G_PHY_RST_23	C34	Output signal that resets an Optical PHY on port 2 and port 3 (with copper PHY this signal is not used)	O 3.3V		

Table 22 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair	I SATA		Supports Serial ATA specification, Revision 3.0
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair	O SATA		Supports Serial ATA specification, Revision 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair	I SATA		Supports Serial ATA specification, Revision 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair	O SATA		Supports Serial ATA specification, Revision 3.0
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low	I/O 3.3V		

Table 23 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express Transmit Output Differential Pairs 0	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express Receive Input Differential Pairs 0	I PCIE		
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express Transmit Output Differential Pairs 1	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express Receive Input Differential Pairs 1	I PCIE		
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express Transmit Output Differential Pairs 2	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express Transmit Output Differential Pairs 3	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express Transmit Output Differential Pairs 4	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express Receive Input Differential Pairs 4	I PCIE		
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express Transmit Output Differential Pairs 5	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express Receive Input Differential Pairs 5	I PCIE		
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express Transmit Output Differential Pairs 6	O PCIE		Supports PCI Express Base Specification, Revision 2.0
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express Receive Input Differential Pairs 6	I PCIE		
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express Transmit Output Differential Pairs 7	O PCIE		Supports PCI Express Base Specification, Revision 2.0 Shared with and connected to the GbE controller
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express Receive Input Differential Pairs 7	I PCIE		
PCIE_TX8+ PCIE_TX8-	A71 A72	PCI Express Transmit Output Differential Pairs 8	O PCIE		Not connected
PCIE_RX8+ PCIE_RX8-	B71 B72	PCI Express Receive Input Differential Pairs 8	I PCIE		
PCIE_TX9+ PCIE_TX9-	A74 A75	PCI Express Transmit Output Differential Pairs 9	O PCIE		Not connected
PCIE_RX9+ PCIE_RX9-	B74 B75	PCI Express Receive Input Differential Pairs 9	I PCIE		

PCIE_TX10+ PCIE_TX10-	A77 A78	PCI Express Transmit Output Differential Pairs 10	O PCIE		Not connected
PCIE_RX10+ PCIE_RX10-	B77 B78	PCI Express Receive Input Differential Pairs 10	I PCIE		
PCIE_TX11+ PCIE_TX11-	A81 A82	PCI Express Transmit Output Differential Pairs 11	O PCIE		Not connected
PCIE_RX11+ PCIE_RX11-	B81 B82	PCI Express Receive Input Differential Pairs 11	I PCIE		
PCIE_TX12+ PCIE_TX12-	A39 A40	PCI Express Transmit Output Differential Pairs 12	O PCIE		Not connected
PCIE_RX12+ PCIE_RX12-	B39 B40	PCI Express Receive Input Differential Pairs 12	I PCIE		
PCIE_TX13+ PCIE_TX13-	A36 A37	PCI Express Transmit Output Differential Pairs 13	O PCIE		Not connected
PCIE_RX13+ PCIE_RX13-	B36 B37	PCI Express Receive Input Differential Pairs 13	I PCIE		
PCIE_TX14+ PCIE_TX14-	A25 A26	PCI Express Transmit Output Differential Pairs 14	O PCIE		Not connected
PCIE_RX14+ PCIE_RX14-	B25 B26	PCI Express Receive Input Differential Pairs 14	I PCIE		
PCIE_TX15+ PCIE_TX15-	A22 A23	PCI Express Transmit Output Differential Pairs 15	O PCIE		Not connected
PCIE_RX15+ PCIE_RX15-	B22 B23	PCI Express Receive Input Differential Pairs 15	I PCIE		
PCIE_TX16+ PCIE_TX16-	D52 D53	PCI Express Transmit Output Differential Pairs 16	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX16+ PCIE_RX16-	C52 C53	PCI Express Receive Input Differential Pairs 16	I PCIE		
PCIE_TX17+ PCIE_TX17-	D55 D56	PCI Express Transmit Output Differential Pairs 17	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX17+ PCIE_RX17-	C55 C56	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE_TX18+ PCIE_TX18-	D58 D59	PCI Express Transmit Output Differential Pairs 18	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX18+ PCIE_RX18-	C58 C59	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE_TX19+ PCIE_TX19-	D61 D62	PCI Express Transmit Output Differential Pairs 19	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX19+ PCIE_RX19-	C61 C62	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE_TX20+ PCIE_TX20-	D65 D66	PCI Express Transmit Output Differential Pairs 20	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX20+ PCIE_RX20-	C65 C66	PCI Express Receive Input Differential Pairs 20	I PCIE		

PCIE_TX21+ PCIE_TX21-	D68 D69	PCI Express Transmit Output Differential Pairs 21	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX21+ PCIE_RX21-	C68 C69	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE_TX22+ PCIE_TX22-	D71 D72	PCI Express Transmit Output Differential Pairs 22	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX22+ PCIE_RX22-	C71 C72	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE_TX23+ PCIE_TX23-	D74 D75	PCI Express Transmit Output Differential Pairs 23	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX23+ PCIE_RX23-	C74 C75	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE_TX24+ PCIE_TX24-	D78 D79	PCI Express Transmit Output Differential Pairs 24	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX24+ PCIE_RX24-	C78 C79	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE_TX25+ PCIE_TX25-	D81 D82	PCI Express Transmit Output Differential Pairs 25	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX25+ PCIE_RX25-	C81 C82	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE_TX26+ PCIE_TX26-	D85 D86	PCI Express Transmit Output Differential Pairs 26	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX26+ PCIE_RX26-	C85 C86	PCI Express Receive Input Differential Pairs 26	I PCIE		
PCIE_TX27+ PCIE_TX27-	D88 D89	PCI Express Transmit Output Differential Pairs 27	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX27+ PCIE_RX27-	C88 C89	PCI Express Receive Input Differential Pairs 27	I PCIE		
PCIE_TX28+ PCIE_TX28-	D91 D92	PCI Express Transmit Output Differential Pairs 28	O PCIE		Not connected
PCIE_RX28+ PCIE_RX28-	C91 C92	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE_TX29+ PCIE_TX29-	D94 D95	PCI Express Transmit Output Differential Pairs 29	O PCIE		Not connected
PCIE_RX29+ PCIE_RX29-	C94 C95	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE_TX30+ PCIE_TX30-	D98 D99	PCI Express Transmit Output Differential Pairs 30	O PCIE		Not connected
PCIE_RX30+ PCIE_RX30-	C98 C99	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE_TX31+ PCIE_TX31-	D101 D102	PCI Express Transmit Output Differential Pairs 31	O PCIE		Not connected
PCIE_RX31+ PCIE_RX31-	C101 C102	PCI Express Receive Input Differential Pairs 31	I PCIE		

PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express Lanes	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device

Table 24 USB 2. 0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+ USB1-	B46 B45	USB Port 1, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+ USB2-	A43 A42	USB Port 2, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+ USB3-	B43 B42	USB Port 3, differential data pair	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB		Do not pull this line high on the carrier board
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low	I 3.3VSB		Do not pull this line high on the carrier board
USB0_HOST_ PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high values indicates that a host is present	I 3.3VSB		Not connected

Table 25 USB 3.0 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+ USB_SSRX0-	C4 C3	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX0+ USB_SSTX0-	D4 D3	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX1+ USB_SSRX1-	C7 C6	Additional receive signal differential pairs for the Superspeed USB data path	I		
USB_SSTX1+ USB_SSTX1-	D7 D6	Additional transmit signal differential pairs for the Superspeed USB data path	O		
USB_SSRX2+ USB_SSRX2-	C10 C9	Additional receive signal differential pairs for the Superspeed USB data path	I		Not connected
USB_SSTX2+ USB_SSTX2-	D10 D9	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not connected

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX3+ USB_SSRX3-	C13 C12	Additional receive signal differential pairs for the Superspeed USB data path	I		Not connected
USB_SSTX3+ USB_SSTX3-	D13 D12	Additional transmit signal differential pairs for the Superspeed USB data path	O		Not connected

Table 26 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_CLK	B10	LPC clock output - 24 MHz nominal	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V	PU 10K 3.3V	Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 10K 3.3V	
SUS_STAT#	B18	In LPC mode, SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state	O 3.3V		
ESPI_EN#	B47	This signal is used by the carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The carrier should only float this line or pull it low	I 3.3V		Not connected

Table 27 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for carrier board SPI BIOS flash	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI is provided but not used
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flas	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 3.3VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only	O 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3VSB	PU 10K 3.3VSB	
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device	I 3.3VSB	PU 10K 3.3VSB	

Table 28 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX [1]	A98	General purpose serial port transmitter	O 3.3V-T		
SER0_RX [1]	A99	General purpose serial port receiver	I 3.3V-T	PU 47K5 3.3V	
SER1_TX [1]	A101	General purpose serial port transmitter	O 3.3V-T		
SER1_RX [1]	A102	General purpose serial port receiver	I 3.3V-T	PU 47K5 3.3V	

Note

1. *Pins are protected on the module by a series schotty diode. Therefore, pull-down resistor is required on the carrier board for proper logic level.*

Table 29 I2C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output	I/O 3.3V	PU 2K2 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 2K2 3.3VSB	

Table 30 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		Not supported
WDT	B27	Output indicating that a watchdog time-out event has occurred	O 3.3V	PD 10K	
FAN_PWMOUT [1]	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O OD 3.3V		
FAN_TACHIN [1]	B102	Fan tachometer input	I OD 3.3V	PU 10K 3.3V	Requires a fan with a two pulse output
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM	I 3.3V	PD 1K	

Note

1. *Pins are protected on the module by a series schotty diode. Therefore, pull-down resistor is required on the carrier board for proper logic level.*

Table 31 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. Note: For proper detection, assert a pulse width of at least 16 ms	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low Note: For proper detection, assert a pulse width of at least 16 ms	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to delay the startup of the of module to enable the programming of FPGAs or other configurable devices on the carrier board	I 3.3V		Set by resistor divider to accept 3.3V
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply	O 3.3VSB		Signal may be used to enable ATX power supply but does not initiate a “Suspend-to-RAM” state
SUS_S4#	A18	SUS_S4# pin is tied to SUS_S5# pin. When asserted, it indicates that system is in Soft-Off state	O 3.3VSB		
SUS_S5#	A24		O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity	I 3.3VSB	PU 10K 3.3VSB	Not supported
BATLOW#	A27	Can be used as a power-fail indication	I 3.3VSB	PU 10K 3.3VSB	
LID# [1]	A103	Lid button. Used by the ACPI operating system for a LID switch. Note: For proper detection, assert a pulse width of at least 16 ms	I OD 3.3V	PU 10K 3.3VSB	
SLEEP# [1]	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again. Note: For proper detection, assert a pulse width of at least 16 ms	I OD 3.3V	PU 10K 3.3VSB	

Note

1. *Pins are protected on the module by a series schotty diode. Therefore, pull-down resistor is required on the carrier board for proper logic level.*

Table 32 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs	I 3.3V		Not supported

Note

The conga-B7AC does not support Rapid Shutdown.

Table 33 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation	I 3.3V	PU 10K 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V		

Table 34 SMBus Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O 3.3VSB	PU 2.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system	I 3.3VSB	PU 2.2K 3.3VSB	

Table 35 SDIO / General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins	O 3.3V		
GPO1	B54	General purpose output pins	O 3.3V		
GPO2	B57	General purpose output pins	O 3.3V		
GPO3	B63	General purpose output pins	O 3.3V		
GPI0	A54	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module	I 3.3V	PU 10K 3.3V	

Note

The conga-B7AC does not support SDIO.

Table 36 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V	P		
GND	A1, A11, A21, A31, A38, A41, A51, A57, A60, A66, A70, A73, A76, A79, A80, A83, A90, A100, A110 B1, B11, B21, B31, B38, B41, B51, B60, B70, B73, B76, B79, B80, B83, B90, B100, B110 C1, C2, C5, C8, C11, C14, C18, C21, C25, C28, C31, C41, C44, C48, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110 D1, D2, D5, D8, D11, D14, D18, D21, D25, D28, D31, D41, D44, D48, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane	P		

Table 37 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0#
TYPE1#
TYPE2#</td><td>C54
C57
D57</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1 and Type 10, these pins are don’t care (X).
<table>
<tr><th>TYPE2#</th><th>TYPE1#</th><th>TYPE0#</th><th></th></tr>
<tr><td>X
NC
NC
NC
NC
GND
GND
X</td><td>X
NC
NC
GND
GND
NC
NC
X</td><td>X
NC
GND
NC
GND
NC
GND
X</td><td>Pinout Type 1 (deprecated)
Pinout Type 2 (deprecated)
Pinout Type 3 (deprecated)
Pinout Type 4 (deprecated)
Pinout Type 5 (deprecated)
Pinout Type 6
Pinout Type 7
Pinout Type 10</td></tr>
</table>
The carrier board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The carrier board logic may also implement a fault indicator such as an LED</td><td>PDS</td><td>TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard.
The conga-B7AC is based on the COM Express Type 7 pinout, therefore pins C54 and D57 are connected to GND and pin C57 is not connected</td></tr>
<tr><td>TYPE10#</td><td>A97</td><td>Dual use pin. Indicates to the carrier board that a Type 10 module is installed. Indicates to the carrier that a Rev. 1.0/2.0 module is installed
<table>
<tr><th>TYPE10#</th><th></th></tr>
<tr><td>NC
PD
12V</td><td>Pinout R2.0
Pinout Type 10 pull down to ground with 4.7K resistor
Pinout R1.0</td></tr>
</table>
This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12V on this pin. R2.0 module Types 1-6 will no-connect this pin. R3.0 module types 6 and 7 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7K resistor</td><td>PDS</td><td>Not connected to indicate “Pinout R2.0”</td></tr>
</table>

8.2 Boot Strap Signals

Table 38 Boot Strap Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
10G_INT3	D24	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Can also be used as Software-Definable Pin on the 10 GbE interface	I CMOS	PU 2.2K 3.3V	
10G_SDP3	D17	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O 3.3V	PU 20k 3.3V	
10G_PHY_MDC_SCL[0-3]	C46-C45 C16-C15	Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY	O 3.3V	PU 1K 3.3V	
SER0_TX	A98	General purpose serial port transmitter	O 3.3V-T	PD 20K	
SER1_TX	A101	General purpose serial port transmitter	O 3.3V-T	PU 20K 3.3V	
10G_PHY_MDIO_SDA[0-3]	D46-D45 D16-D15	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY	O 3.3V	PU 1K 3.3V	

Caution

1. *Do not drive the signals listed in the table above until 400 ns after CB_RESET# de-asserts. These signals are used as chipset configuration straps during system reset. In this condition (during reset), the COM Express or chipset internally implemented resistors pull these signals to the correct state.*

2. *No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table during the power-up sequence. External resistors may override the internal strap states and cause the COM Express module to malfunction or cause irreparable damage to the module.*

9 System Resources

9.1 I/O Address Assignment

Table 39 I/O Resources

Address	Device
00 - 1F	Transaction is terminated
20 - 21	8259 PIC
24 - 25	8259 PIC
28 - 29	8259 PIC
2C - 2D	8259 PIC
2E - 2F	LPC
30 - 31	8259 PIC
34 - 35	8259 PIC
38 - 39	8259 PIC
3C - 3D	8259 PIC
40	8254 timer
41	Transaction is terminated
42 - 43	8254 timer
4E - 4F	LPC
50	8254 timer
51	Transaction is terminated
52 - 53	8254 timer
60	PS/2 legacy keyboard/mouse
61	NMI controller
62	LPC
63	NMI controller
64	PS/2 legacy keyboard/mouse
65	NMI controller
66	LPC
67	NMI Controller
70	CPU interface, RTC, power management controller
71	RTC, power management controller
72 - 73	RTC, power management controller
74	RTC, power management controller
75	RTC, power management controller
76 - 77	RTC, power management controller
80	LPC or PCIe root port (port 80h)
81 - 83	Transaction is terminated

84 - 86	LPC or PCIe root port (port 80h)
87	Transaction is terminated
88	LPC or PCIe root port (port 80h)
89 - 8B	Transaction is terminated
8C - 8E	LPC or PCIe root port (port 80h)
8F	Transaction is terminated
90	LPC
91	Transaction is terminated
92	P2SB->ITSS (CPU I/F)
93	Transaction is terminated
94 - 96	LPC
97	Transaction is terminated
98	LPC
99 - 9B	Transaction is terminated
9C - 9E	LPC
9F	Transaction is terminated
A0 - A1	8259 PIC
A4 - A5	8259 PIC
A8 - A9	8259 PIC
AC - AD	8259 PIC
B0 - B1	8259 PIC
B2 - B3	Power management - SMI
B4 - B5	8259 PIC
B8 - B9	8259 PIC
BC - BD	8259 PIC
C0 - DF	Transaction is terminated
E0 - FF	Transaction is terminated
170 - 177	Transaction is terminated
1F0 - 1F7	Transaction is terminated
200 - 207	LPC (gameport)
208 - 20F	LPC (high gameport)
220 - 227	LPC (COM port)
228 - 22F	LPC (COM port)
238 - 23F	LPC (COM port)
278 - 27F	LPC (high gameport)
2E8 - 2EF	LPC (COM port)
2F8 - 2FF	LPC (COM port)
338 - 33F	LPC (COM port)
370 - 375	LPC (floppy drive)
376	Transaction is terminated
377	LPC (floppy drive)
378 - 37F	LPC (parallel port)

3B0 - 3B8	PCIe bridge (VGA)
3BC - 3BE	LPC (parallel port)
3C0 - 3DF	PCIe bridge (VGA)
3E8 - 3EF	LPC (COM port)
3F0 - 3F5	LPC (floppy drive)
3F6	Transaction is terminated
3F7 - 3F7	LPC (floppy drive)
3F8 - 3FF	LPC (COM port)
4D0 - 4D1	8259 PIC
678 - 67F	LPC (parallel port)
778 - 77F	LPC (parallel port)
7BC - 7BE	LPC (parallel port)
A00 - A3F	BMC software wake control
A40 - A4F	BMC mailbox
CA0 - CAF	BMC keyboard controller style interface
CF8 - CFB	Configuration registers
CF9	Software-generated reset
CFC - CFF	Configuration registers
E00 - EFF	Board Controller

9.2 LPC Bus

On the conga-B7AC, the PCI Express acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI bus (and not to the LPC bus). Only specified I/O ranges are forwarded to the LPC bus. In the congatec Embedded BIOS, the following I/O address ranges are sent to the LPC bus:

2Eh - 2Fh

4Eh - 4Fh

62h, 66h

60h, 64h

A00h - A7Fh

E00h - EFFh (always used internally)

Parts of these ranges are not available for customer use if a Super I/O is used on the carrier board. For additional LPC bus resources other than those mentioned above, set the desired I/O ranges in the BIOS setup menu under “LPC Generic I/O Range Decode”.

Note

The LPC Generic I/O Range Decode menu is not yet implemented in the current BIOS. This menu will however be implemented in future BIOS release.

9.3 PCI Configuration Space Map

Table 40 PCI Device Mapping

Bus [2]	Device Number [hex (decimal)]	Function (hex)	Vendor ID (hex)	Device ID (hex)	Device
00	00	0	8086	1980 - 199F	System agent
00	04	0	8086	19A1	GLREG
00	05	0	8086	19A2	Root complex event collector
00	06	0	8086	19A3	Root port for QAT
00	09	0	8086	19A4	PCIe root port 0
00	0A (10)	0	8086	19A5	PCIe root port 1
00	0B (11)	0	8086	19A6	PCIe root port 2
00	0C (12)	0	8086	19A7	PCIe root port 3
00	0E (14)	00	8086	19A8	PCIe root port 4
00	0F (15)	00	8086	19A9	PCIe root port 5
00	10 (16)	00	8086	19AA	PCIe root port 6
00	12 (18)	00	8086	19AC	SMBUS controller - host
00	14 (20)	00	8086	19C0 - 19C7, 19CE, 19CF	SATA
00	15 (21)	00	8086	19D0	USB
00	16 (22)	00	8086	19D1	Root port for LAN 0
00	17 (23)	00	8086	19D2	Root port for LAN 1
00	18 (24)	00	8086	19D3	HECI
00	1C (28)	00	8086	19DB	eMMC
00	1F (31)	00	8086	19DC	LPC
00	1F (31)	02	8086	19DE	PMC
00	1F (31)	04	8086	19DF	SMBus - legacy
00	1F (31)	05	8086	19E0	SPI
r	00	00	8086	19E2	QAT
s	00	00	12D8	2912	PCIe2 switch
t	02	00	12D8	2912	PCIe2 switch
t	03	00	12D8	2912	PCIe2 switch
t	0A	00	12D8	2912	PCIe2 switch
t	0B	00	12D8	2912	PCIe2 switch

Bus [2]	Device Number [hex (decimal)]	Function (hex)	Vendor ID (hex)	Device ID (hex)	Device
t	0C	00	12D8	2912	PCIe2 switch
t	0D	00	12D8	2912	PCIe2 switch
t	0E	00	12D8	2912	PCIe2 switch
t	0F	00	12D8	2912	PCIe2 switch
u	00	00	1A03	1150	BMC [1]
v	00	00	1A03	2000	BMC VGA [1]
x	00	00	8086	1533	GBE
y	00	00	8086	1306, 1307, 15B4, 15C2 - 15C7, 15E4, 15E5, 15C8, 15CE	LAN 0
y	00	01	8086	1306, 1307, 15B4, 15C2 - 15C7, 15E4, 15E5, 15C8, 15CE	
z	00	00	8086	1306, 1307, 15B4, 15C2 - 15C7, 15E4, 15E5, 15C8, 15CE	LAN 1
z	00	01	8086	1306, 1307, 15B4, 15C2 - 15C7, 15E4, 15E5, 15C8, 15CE	

Note

1. *Applies only to the commercial variants of conga-X7/EVAL.*

2. *The bus numbers represented with alphabets "s - z" will vary depending on the system configuration (lane width), the connected PCIe devices (switches or bridges) and where these devices are connected.*

10 BIOS Setup Description

The BIOS setup description of the conga-B7AC can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-B7AC is identified as DSACR1xx, where:

- R is the identifier for a BIOS ROM file
- 1 is the feature number
- xx is the major and minor revision number

The conga-B7AC BIOS binary size is 16 MB.

10.2 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-B7AC features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions— UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated.*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.2.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at http://www.congatec.com.

10.3 Supported Flash Devices

The conga-B7AC supports the following flash devices:

- Winbond W25Q128JVSIQ (16 MB)
- Macronix MX25L12835FM2I-10G (16 MB)
- GigaDevice GD25Q127CSIGR (16 MB)

The flash devices listed above can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.