400G QSFP-DD DR4 Transceiver

ET7502-DR4

Edgecore's QSFP-DD 4*100Gbps transceiver module is designed for optical communication applications over 400 Gigabit Ethernet links of up to 500 m of single mode fiber. This product has 8 independent electrical input/output channels that convert 50Gbps (PAM4) electrical input data to 4 channels of 100Gbps (PAM4) parallel optical signals over 1310 nm wavelengths. The electrical interface of the module is compliant with the 400GAUI-8 interface as defined by IEEE 802.3bs, and compliant with QSFP-DD MSA.

Product Features

- Single 3.3 V power supply
- Power dissipation < 10 W
- Up to 500 m over SMF fiber
- QSFP-DD MSA compliant
- 8x53.125Gbps (PAM4) electrical interface
- MPO-12 connector
- Commercial case temperature range of 0°C to 70°C
- PIN and TIA array on the receiver side
- I2C interface with integrated Digital Diagnostic Monitoring
- RoHS compliant

Applications

- 4 x 100G-DR applications
- Data center
- Infiniband interconnects

Ordering Information

Part Number	Data Rate	Fiber	Distance	Interface	Temp.	DDMI	CMIS
ET7502-DR4	425 Gbps	SMF	500 m	MPO12	0~+70°C	Yes	CMIS4.0 *(note1)

Note 1: CMIS4.0 or later versions

Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Signaling Speed per Lane			53.125		GBd
Modulation Format			PAM4		
Center Wavelength	λC	1304.5	1311	1317.5	nm
Side-mode Suppression Ratio	SMSR	30			dB
Average Launch Power, Each Lane*(note 1)	TxAVG	-2.9		4	dBm
Transmit OMA_{outer} Each Lane*(note 2)	TxOMA	-0.8		4.2	dBm
Launch Power in OMA_{outer} Minus TDECQ, Each Lane		-2.2			dBm
Transmitter and Dispersion Eye Closure, Each Lane	TDECQ			3.4	dB
Average Launch Power of OFF Transmitter, Each Lane				-15	dBm
Extinction Ratio	ER	3.5			dB
$RIN_{21.4}OMA$				-136	dB/Hz
Optical Return Loss Tolerance*				21.4	dB
Transmitter Reflectance*(note 3)				-26	dB

Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Signaling Speed per Lane			53.125		GBd
Modulation Format			PAM4		
Center Wavelength	λC	1304.5	1311	1317.5	nm
Damage Threshold Each Lane*(note 4)		5			dBm
Average Receive Power Each Lane*(note 5)	RxAVG	-5.9		4	dBm
Receive Power (OMA_{outer}) Each Lane	RxOMA			4.2	dBm
Receiver Reflectance				-26	dB
Receiver Sensitivity (OMA_{outer}), Each Lane*(note 6)	SenOMA			-4.4	dBm
Stressed Receiver Sensitivity (OMA_{outer}) Each Lane*(note 7)				-1.9	dBm
Conditions of Stressed Receiver Sensitivity Test: *(note 8)					
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test			3.4		dB
OMAouter of Each Aggressor Lane			4.2		dBm
LOS Assert	LOSA	-15			dBm
LOS De-Assert	LOSD			-10	dBm
LOS Hysteresis		0.5			dB

*Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

*Note 2: Even if the TDECQ <1.4 dB, the OMAouter (min) must exceed these values.

*Note 3: Transmitter reflectance is defined looking into the transmitter.

*Note 4: The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.

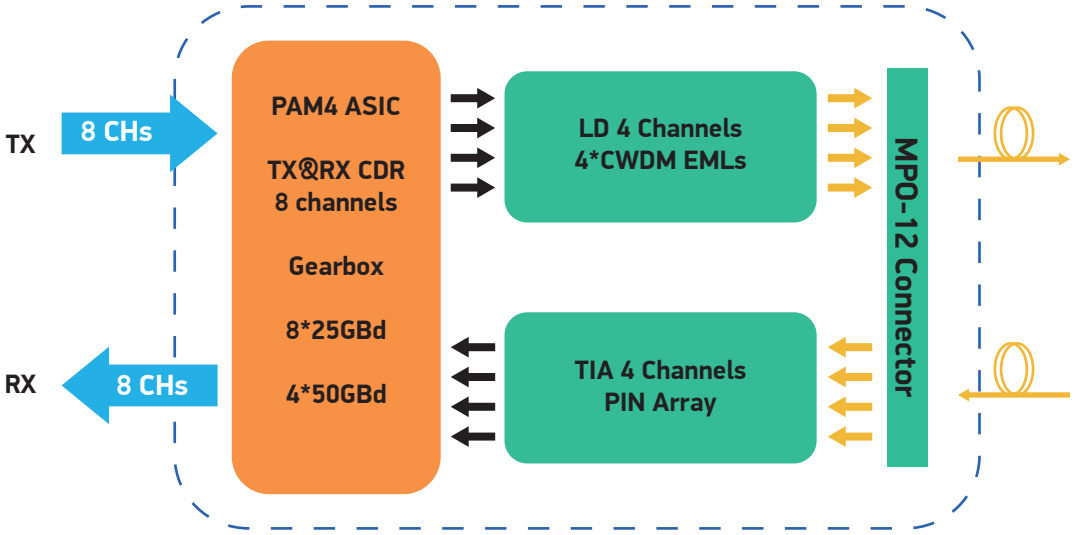
*Note 5: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

*Note 6: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.

*Note 7: Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3bs clause 124.1.1.

*Note 8: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Transceiver Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Damage Threshold	Rxdmg	5		dBm
*Exceeding any one of these values may damage the device permanently.				

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Operating Relative Humidity	RH	5		85	%
Power Dissipation	P_D			10	W

* Power Supply specifications, instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.

Transmitter Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Differential Data Input Swing per Lane*(note 1)		900			mV_{p-p}	
Differential Input Impedance	Zin	90	100	110	ohm	
Stressed Input Parameters						
Eye Width		0.265			UI	@TP4, all 3 PAM4 eyes, 1E-5
DC Common Mode Voltage*(note 2)		-350		2850	mV	

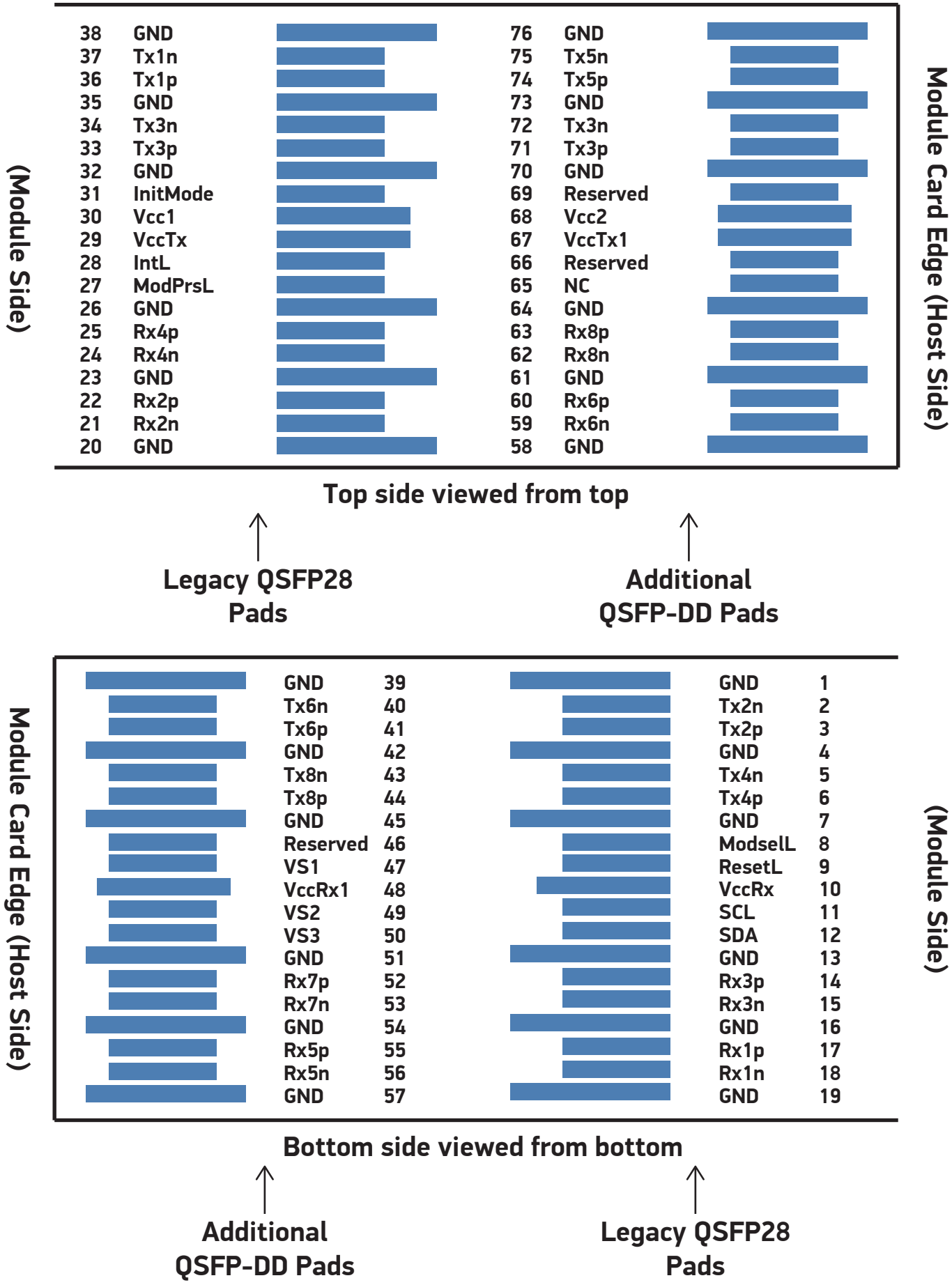
Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Differential Output Amplitude				900	mV_{p-p}	
Differential Output Impedance	Zout	90	100	110	ohm	
Output Rise/Fall Time	t_r/t_f	9.5			ps	20%~80%
Eye Width		0.265			UI	
Eye Height Differential		70			mV	@TP4, all 3 PAM4 eyes, 1E-5

*Note 1: With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

*Note 2: DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

QSFP-DD Transceiver Electrical Pad Layout



Pin Descriptions

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3 V Power Supply Receiver	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	
12	LVCMOS- I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power supply transmitter	2
30		Vcc1	+3.3 V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1

Pin Descriptions

Pin	Logic	Symbol	Description	Note
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3 V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3 V Power Supply	2
68		Vcc2	3.3 V Power Supply	2
69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

*Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted.

*Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination.
The connector Vcc pins are each rated for a maximum current of 1000 mA.

*Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k Ohms and less than 100 pF.

Warranty
Please check www.edge-core.com for the warranty terms in your country.

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