FINITE ELEMENT ANALYSIS

Ansys® LS-DYNA® Performance with AMD EPYC™ 7003 Series Processors

APRIL 2021

AMD EPYC™ 7003 Processors

AMD EPYC™ 7003 Series Processors are the new standard for the modern data center. With high frequencies, high core-counts, high memory bandwidth and capacity, and up to 256MB of L3 cache, AMD EPYC 7003 series processors enable exceptional HPC performance. Built on the x86 architecture innovations of the record setting EPYC 7002 series processors[1], EPYC 7003 series processors carry on the tradition of delivering balanced performance.

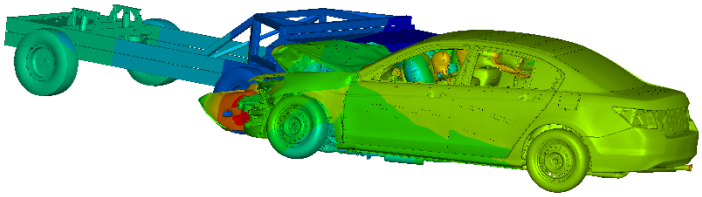

Figure 1: Courtesy of Ansys

Along with the high memory bandwidth achieved with support for 8 channels DDR4-3200 memory, EPYC 7003 processors also synchronize the data fabric clock to match the memory clock speeds, further improving both memory bandwidth and latency. Support for up to 4TB of memory per socket enhances the ability to handle very large datasets.

Extra-large caches, reaching up to 256MB per CPU and up to 32 MB per core, help to efficiently utilize up to 64 cores per CPU. The large caches drive performance, but also enable exceptional scalability on many key workloads. 128-160 lanes of PCIe® Gen4 offered by EPYC 7003 Series CPUs push the ability to efficiently access high-speed network interface cards, high-speed storage, and multiple accelerators.

AMD EPYC 7003 Series Processors are designed to bring faster time-to-value by delivering performance and scalability, while also helping keep your data secure. AMD Infinity Guard helps your organization take control of security and decrease risks to your most important assets – your data[2].

EPYC 7003 series processors raise the bar once again for workload performance, helping to reduce time to insight and delivering improved business outcomes.

AMD EPYC 7003 FOR HPC

3rd Generation EPYC Processors help HPC workloads scale across on-premise clusters and can bring HPC-level performance to the cloud for time-sensitive projects.

Check with your cloud provider about their AMD EPYC based cloud instances and ask them about helping to secure your workload in the cloud with encrypted memory.

"ZEN 3" CORE & SECURITY

Support for up to:

- 64 physical cores, 128 threads
- 256MB of L3 cache per CPU
- 32 MB of L3 cache per core
- 4 TB of DDR4-3200 memory
- 128-160 PCIe® Gen 4 lanes

Infinity Guard security

- Secure Boot
- SME
- SEV-SNP

SCALE OUT AND SCALE UP

Scaling is critical to HPC applications. AMD EPYC 7003 processors provide high bandwidth between nodes with support for PCIe® Gen 4 enabled network devices and accelerators. Within a node, take advantage of up to 64 cores, 8 memory channels of DDR4-3200, and up to 256 MB of L3 cache-per-CPU.

Ansys® LS-DYNA®

Collaboration between AMD and Ansys offers high performance and scalability for Finite Element Analysis (FEA) workloads, helping customers to test designs without having to tool or experimentally test prototypes, saving time and expense.

EPYC 7003 Series Processor Architecture Quick Look

The AMD EPYC 7003 Series Processor retains the proven Multi-Chip Module (MCM) chiplet architecture of prior successful AMD EPYC server processors while making further improvements. One of the most important upgrades is the new "Zen 3" core. The "Zen 3" core is manufactured using a 7nm process and designed to provide a significant instructions per cycle (IPC) uplift over prior generation "Zen 2" cores. Like EPYC 7002 Series processors, each core supports Simultaneous Multi-Threading (SMT), allowing up to 2 threads per core. In a typical 2-socket system with 64-core processors, EPYC 7003 Series processors offer up to 128 physical cores per system and up to 256 threads per system.

The L3 cache was also improved in the Gen 3 EPYC processors. EPYC 7003 Series CPUs took the same total L3 cache as the prior generation (up to 256MB/CPU) and created significantly more cache sharing between cores. The Gen 3 EPYC processors now offer a unified 32MB of L3 cache per compute die. Up to 8 cores per compute die can now share 32MB of unified L3 cache with this generation of processors.

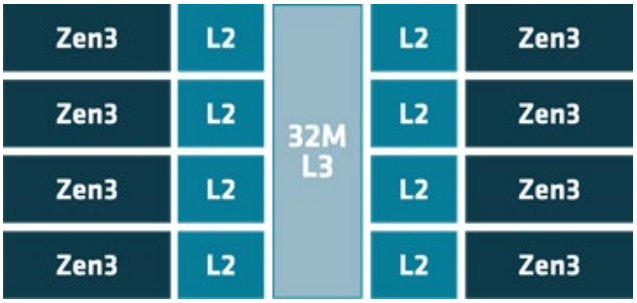

Figure 2: EPYC 7003 Series processor L3 cache layout

The new L3 Cache design can increase the cache hit to miss ratio over the previous design. Improved cache sharing also allows larger blocks to fit directly into the cache whereas previously they would fall into the main memory. Improvements made in the cache fetching and eviction policies manage data more efficiently. All these benefits result in an uplift on HPC workloads in addition to the core and memory improvements.

EPYC 7003 Series CPU Options and Recommendations by Segment

AMD EPYC 7003 Series CPUs offer 19 different CPU configurations. Below is a table of each CPU with a summary of their features. For driving up per-core performance, pay special attention the 7xF3 processors, which offer the highest cache and frequencies at their respective core-counts of the EPYC 7003 series processors.

HPC applications come in a wide range of unique characteristics. There is no one-size fits all CPU for the HPC market. Below are the general recommendations. You are encouraged to talk to your AMD sales representative for more detailed guidance and CPU suggestions based on your unique environment and needs.

Model	# CCDs	Cores / Threads	Base Freq (GHz)	Max Boost Freq (up to GHz)[3]	Default TDP (W)	cTDP (W)	L3 Cache (MB)	NPS	2P/1P
7763	8	64 / 128	2.45	3.50	280W	225-280W	256	1,2,4	2P/1P
7713	8	64 / 128	2.00	3.675	225W	225-240W	256	1,2,4	2P/1P
7713P								1,2,4	1P
7663	8	56 / 112	2.0	3.5	240W	225-240W	256	1,2,4	2P/1P
7643	8	48 / 96	2.3	3.6	225W	225-240W	256	1,2,4	2P/1P
75F3	8	32 / 64	2.95	4.0	280W	225-280W	256	1,2,4	2P/1P
7543	8	32 / 64	2.8	3.7	225W	225-240W	256	1,2,4	2P/1P
7543P								1,2,4	1P
7513	4	32 / 64	2.6	3.65	200W	165-200W	128	1,2,4	2P/1P
74F3	8	24 / 48	3.2	4.0	240W	225-240W	256	1,2,4	2P/1P
7453	4	28 / 56	2.75	3.45	225W	225-240W	64	1,2,4	2P/1P
7443	4	24 / 48	2.85	4.0	200W	165-200W	128	1,2,4	2P/1P
7443P								1,2,4	1P
7413	4	24 / 48	2.65	3.6	180W	165-200W	128	1,2,4	2P/1P
73F3	8	16/ 32	3.5	4.0	240W	225-240W	256	1,2,4	2P/1P
7343	4	16 / 32	3.2	3.9	190W	165-200W	128	1,2,4	2P/1P
7313	4	16 / 32	3.0	3.7	155W	155-180W	128	1,2,4	2P/1P
7313P								1,2,4	1P
72F3	8	8 / 16	3.7	4.1	180W	165-200W	256	1,2,4	2P/1P

Table 1: AMD EPYC 7003 CPU Options

Listed in the table below are a few examples of different HPC market segments, a general sense of the characteristics and sensitivities of applications per segment, and specific AMD EPYC 7003 Series processor recommendations per segment.

Segment	Sensitivity	Example Applications	Recommended Models	Comments
FEA Explicit	Frequency & Cache	LS-DYNA	75F3 | 7543 74F3 | 73F3	Look for CPUs with high frequencies, and large caches. Mid core-counts help increase performance per core to help maximize software investment.
FEA Implicit		Mechanical		
CFD	Memory BW & Cache	Fluent, CFX	75F3 | 7543 74F3	Look for CPUs with 256 MB of cache. Large caches help relieve the potential memory bandwidth bottleneck if using high core counts. Look for mid core-count CPUs for per-core licensed codes.
EDA	Frequency & Cache	RedHawk	73F3 | 72F3	This market segment is dominated by low core-counts to drive up the frequency and cache per core, helping maximize software investment.

Table 2: HPC Segment Recommendations

Ansys LS-DYNA

Ansys develops, markets, and supports engineering simulation software used to predict how product designs will behave in real-world environments. As the global leader in engineering simulation, they continually advance simulation solutions by developing or acquiring the very best technologies, integrating them into a unified simulation platform capable of complex, Multiphysics solutions and providing system services, including high-performance computing (HPC) and cloud solutions, to manage simulation processes and data.

LS-DYNA is a general-purpose multiphysics, finite element analysis program capable of simulating complex real-world problems. It is used by the automotive, aerospace, construction, military, manufacturing, and bioengineering industries.

LS-DYNA is widely used by the automotive industry to analyze vehicle designs. LS-DYNA is designed to predict a car's behavior in a collision and the effects of the collision upon the car's occupants. With LS-DYNA, automotive companies and their suppliers can test car designs without having to tool or experimentally test a prototype, thus saving time and expense.

Test Methodology

This document focuses on performance and scaling of the AMD EPYC 7003 Series Processors as well as comparison with the Intel® Xeon® Gold 6258R.

Testing was performed on dual-socket AMD EPYC™ 7413, AMD EPYC™ 74F3, AMD EPYC™ 7543, and AMD EPYC™ 75F3-based systems. The compute nodes were each populated with 1 DIMM per channel of 64-GB, dual-rank, DDR4-3200 DIMMs from Micron® for a total of 1TB of memory per node. A Mellanox® ConnectX-6 200 Gb/s HDR InfiniBand adapter, utilizing EPYC processors' support for PCIe Gen 4, is also populated on each EPYC processor-based system.

Testing was also run on a dual-socket Intel Xeon Gold 6258R-based platform. The 6258R was selected because it offers the highest frequency of the highest core-count (28c) in the Intel Xeon Gold family of processors. The Intel platforms were populated with 1 DIMM per channel of 64-GB, dual-rank, DDR4-2933 DIMMS (768GB total memory), matching the maximum memory speed supported for this processor.

LS-DYNA uses a standard set of automotive crash simulation models to measure performance. These models are specifically created to reflect real-world workloads to give a standard basis of comparison across various computer systems and architectures. The single-node performance tests in this document are using the neon, 3-cars, and car2car models. Scalability testing was performed using the much larger ODB-10M model. The ODB-10M model was shortened to a termination time of 30ms to reduce overall test duration. The ODB-10M model has 10M cells and is the largest and most representative of today's real-world car crash simulation models available from the standard LS-DYNA benchmarks. These models provide a standard baseline for comparing single-node performance and scalability of LS-DYNA.

LS-DYNA performance is typically measured in elapsed time. To show relative performance comparisons, elapsed time is converted to performance (1/elapsed time), then used to show the relative performance comparison (AMD Perf/Intel Perf, higher is better).

Every benchmark was run a minimum of 3 iterations, with average core solver rating used in the brief. Results of each benchmark were also confirmed to have <1% variability between all runs.

System Configuration

AMD System Configuration				
CPUs	2 x AMD EPYC 7413	2 x AMD EPYC 74F3	2 x AMD EPYC 7543	2 x AMD EPYC 75F3
Frequency: Base | Boost[3]	2.65 GHz | up to 3.6 GHz	3.2 GHz | up to 4.0 GHz	2.8 GHz | up to 3.7 GHz	2.95 GHz | up to 4.0 GHz
Cores	24 cores/socket (48c/node)		32 cores/socket (64 per node)	
L3 Cache	128 MB	256 MB		
Memory	1TB (16x) Dual-Rank DDR4-3200 64GB DIMMs, 1DPC			
NIC	Mellanox ConnectX-6 HDR 200Gb InfiniBand x16 (OFED-4.5-1.0.1)			
Storage: OS | Data	1 x 256 GB SATA | 1 x 1 TB NVMe			
BIOS and Settings	SMT=off, X2APIC=on, IOMMU=off, APBDIS=1, Fixed SOC P-state=0, Determinism=power, NPS=4, DF C-states=off, PIO, EPIO, TSME=off, PCIe 10 bit tag=on			
OS Settings	clear caches before every run, NUMA balancing 0, randomize_va_space 0, cc6 disabled, Governor=Performance			

Table 3: AMD EPYC System Configuration

Intel System Configuration	
CPUs	2 x Intel Xeon Gold 6258R
Frequency: Base | Turbo	2.7 GHz | 4.0 GHz
Cores	28 cores per socket (56 per node)
L3 Cache	38.5 MB
Memory	768 GB (12x) Dual-Rank DDR4-2933 64GB DIMMs, 1DPC
NIC	Mellanox ConnectX-6 HDR 200Gb InfiniBand x16 (OFED-4.5-1.0.1)
Storage: OS | Data	1 x 256 GB SATA | 1 x 1 TB NVMe
BIOS and Settings	3.3a: Power Management=Extreme Performance, Hyper-threading=Off, SNC=On, ADDDC=Off
OS Settings	clear caches before every run, NUMA balancing 0, randomize_va_space 0

Table 4: Intel System Configuration

Software	
Solver Version	Ansys LS-DYNA **2021 R1**
MPI	Intel MPI 2019
OS	SLES 12 SP 5

Table 5: Software

LS-DYNA Single-Node Performance

Single-node performance is a critical starting point for evaluating HPC performance. This section shows relative performance comparisons of individual systems.

LS-DYNA performance is affected by many aspects of the CPU. LS-DYNA specifically scales very well with frequency, cores, memory bandwidth, and cache size.

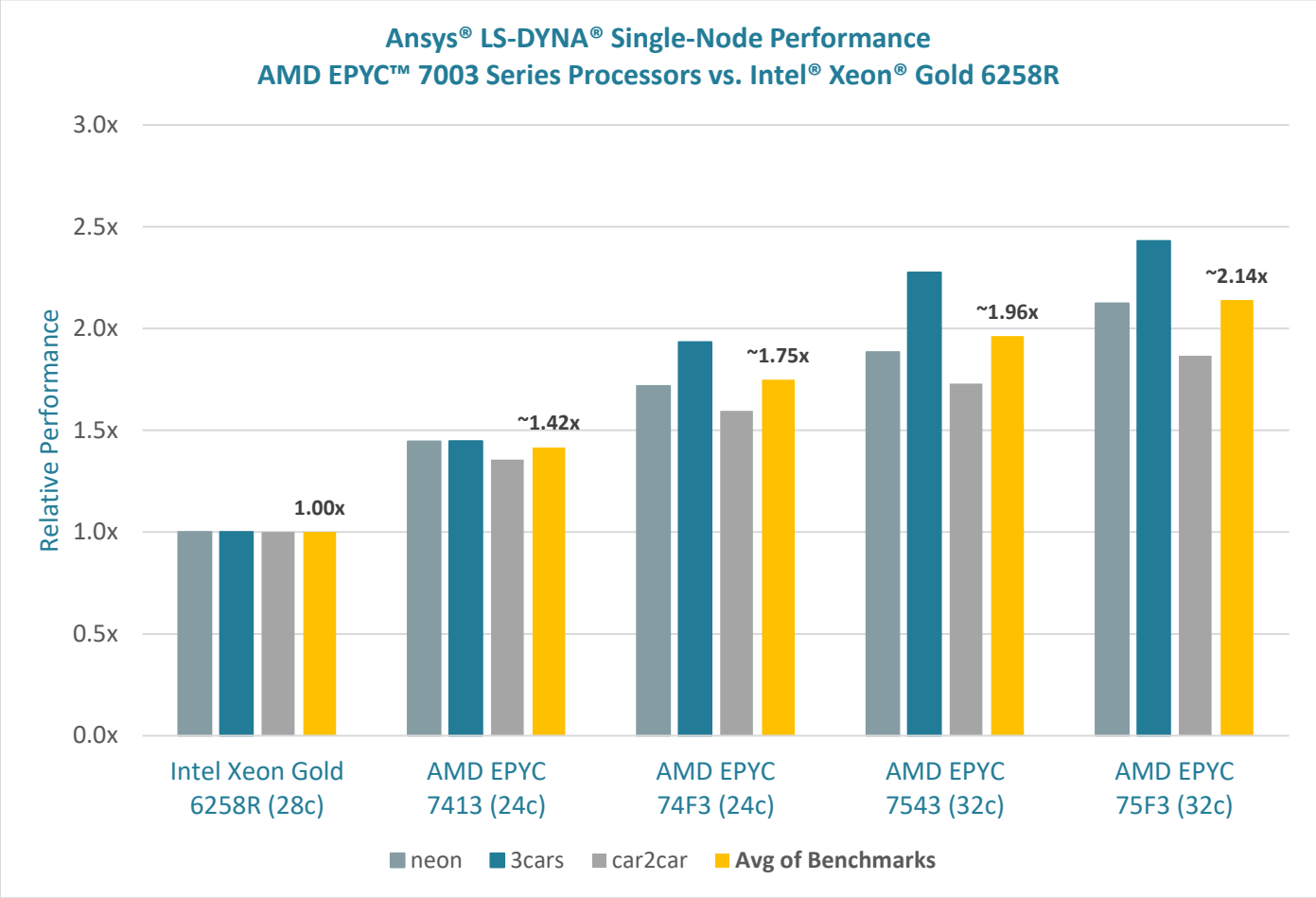

Figure 3: Ansys LS-DYNA Single-Node Performance - See Page 5 for system configurations.

All AMD EPYC processors tested outperform the Intel Xeon Gold 6258R in all benchmarks. A balance of high memory bandwidth, large caches, and high frequency yields great results:

- The 32-core AMD EPYC 75F3, base frequency 2.95GHz and max boost of up to 4.0GHz, showed the highest performance. It significantly outperforms the Intel Xeon 6258R-based system by an average of up to 2.14x.
- The 32-core AMD EPYC 7543 also demonstrates exceptional performance with a base frequency of 2.8GHz and a max boost of up to 3.7GHz. The large cache (the same 256MB total cache as the 75F3), helps to deliver incredible performance, with an average of up to 1.96x higher performance vs. the Intel Xeon 6258R-based system.
- The 24-core AMD EPYC 74F3, with a base frequency of 3.2GHz and max boost up to 4.0GHz, maintains an average uplift of up to 1.75x, despite having 4 fewer cores than the Intel Xeon Gold 6258R-based system.
- With a base frequency of 2.65GHz and max boost frequency of up to 3.6GHz, the 24-core AMD EPYC 7413 still outperforms the 28-core Intel Xeon Gold 6258R by an incredible average of up to 1.42x.

LS-DYNA Per-Core Performance

Understanding workload performance at the core level provides a better understanding of the potential TCO of a hardware purchase:

- *Maximize Software Investment:* Many software vendors, including Ansys, offer per-core software licensing. It may be beneficial, depending on your specific situation, to maximize performance per-core to help minimize your TCO. Understanding how performance relates to core counts helps right-size how many licenses are required and enables running simulations at higher fidelity.
- *Precise Installation Sizing:* Core-level performance makes it easier to fine-tune decision-making when sizing the application footprint of your hardware purchase.

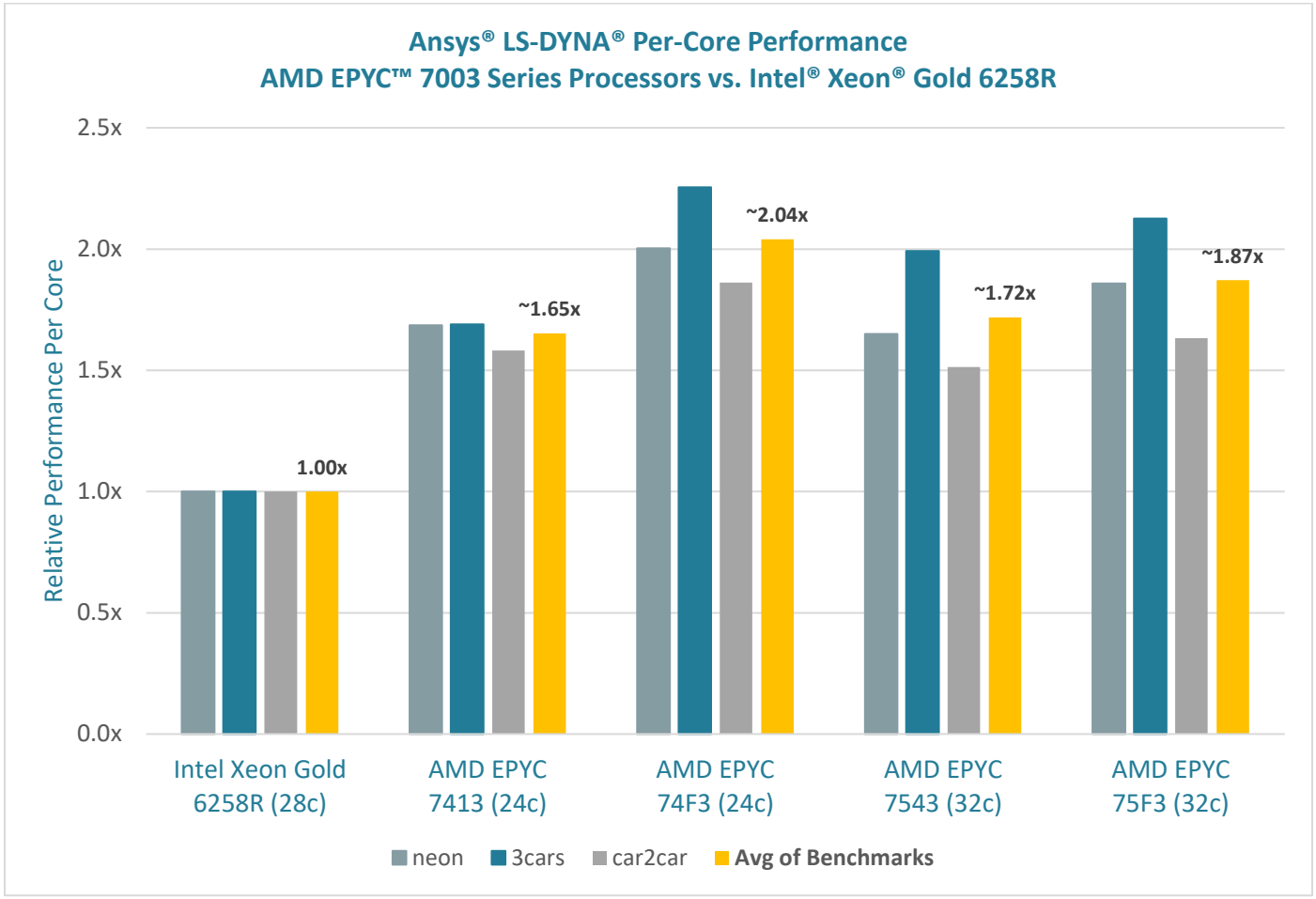

Figure 4: Ansys LS-DYNA Per-Core Performance - See Page 5 for system configurations.

All AMD EPYC 7003 Series processors tested deliver truly exceptional per-core performance:

- The 24-core EPYC 74F3 stands out with exceptional per-core performance – delivering on average up to 2.04x the performance per-core vs. the Intel Xeon Gold 6258R.
- The lower frequency, lower cache 24-core EPYC 7413 (128MB L3 Cache) still delivers dominant per-core performance, with an average uplift of ~1.65x over Intel Xeon Gold 6258R.
- 32 core EPYC processors also significantly outperform Intel Xeon Gold 6258R-based systems on a per-core performance basis.

Ansys LS-DYNA Multi-Node Scaling

LS-DYNA scales exceptionally well on AMD EPYC 7003 series processors. The chart below shows scaling of the AMD EPYC 75F3 CPU in two-socket platforms vs. linear scaling running the OSB-10M benchmark. At 32-cores per processor, each node has 64 physical cores for a total of 256 cores at 4 nodes.

FEA Explicit workloads generally do not scale linearly, however LS-DYNA exhibits very good scaling. The speedup is ~1.88 at 2 nodes (128 cores), and with 4 nodes (256 cores), the speedup stays very high at ~3.27.

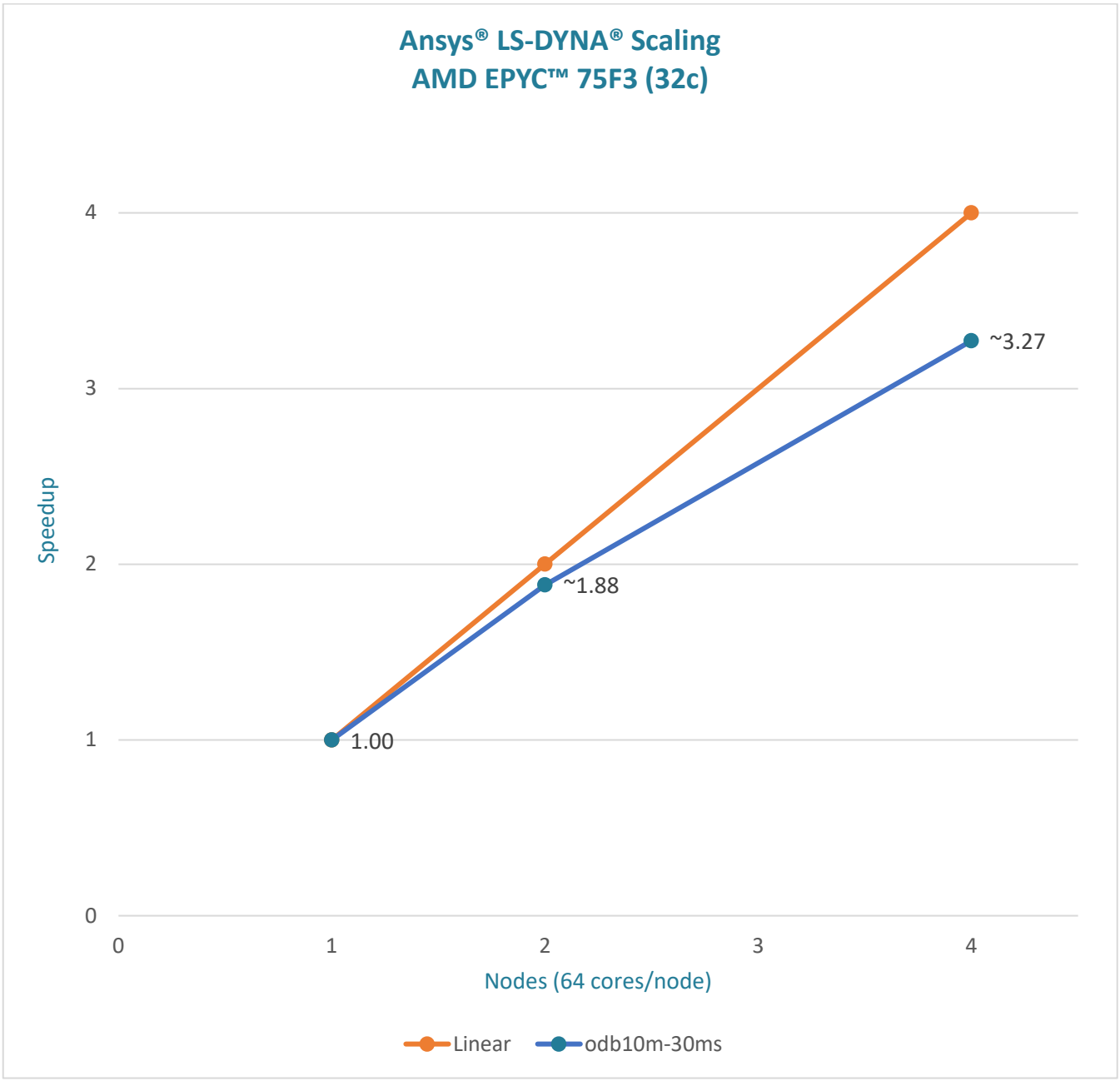

Figure 5: Ansys LS-DYNA Multi-Node Scaling - See Page 5 for system configuration.

Conclusion and Recommendations

Whether you are scaling-out to higher node-counts, or driving more density into your clusters, AMD EPYC 7003 Series processors give you more levers to tilt the performance balance your way. This provides new opportunities for more density in your datacenter, and for even more demanding workloads.

- *Per-Node Performance*: All AMD EPYC processors tested delivered exceptional per node performance results. The 75F3 stands out, delivering on average up to 2.14x higher performance than the Intel Xeon Gold 6258R.
- *Per-Core Performance*: The AMD EPYC 74F3 processor stands out in per-core performance, delivering an average up to 2.04x higher performance per core than the Intel Xeon Gold 6258R.
- *Scalability*: LS-DYNA scalability on the AMD 75F3 processor is exceptional. At 4 nodes (256 cores) LS-DYNA exhibited a speedup of ~3.27.

Ansys LS-DYNA Finite Element Analysis application is architected to deliver accuracy, performance, and scalability. The automotive industry relies upon LS-DYNA to accurately simulate cars' behavior in collisions, allowing increased safety, reduced development costs, and quicker time to production.

Together, AMD and Ansys empower the development of fast, accurate FEA Explicit simulations running on cost-effective clustered systems.

RELATED LINKS

- Ansys*
- Ansys and AMD*
- Ansys LS-DYNA*
- High Performance Computing (HPC) Tuning Guide for AMD EPYC™ 7003 Series Processors
- AMD EPYC™ Processors
- AMD EPYC Technical Briefs and Tuning Guides

*Links to third party sites are provided for convenience and unless explicitly stated, AMD is not responsible for the contents of such linked sites and no endorsement is implied.

FOOTNOTES

1. For a complete list of world records see http://amd.com/worldrecords. EPYC-22
2. AMD Infinity Guard features vary by EPYC™ Processor generations. Infinity Guard security features must be enabled by server OEMs and/or Cloud Service Providers to operate. Check with your OEM or provider to confirm support of these features. Learn more about Infinity Guard at https://www.amd.com/en/technologies/infinity-guard . GD-183
3. For AMD EPYC processors is the maximum frequency achievable by any single core on the processor under normal operating conditions for server systems. EPYC-18