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5 RF Signal Chain Discourse: Properties and Performance Metrics

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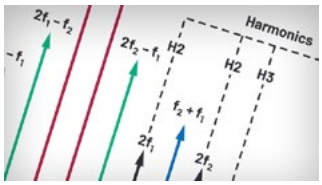

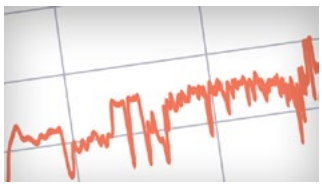

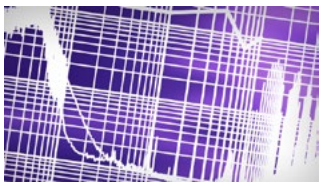

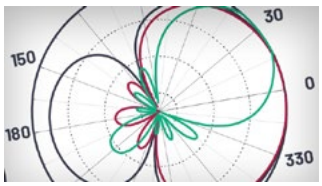

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RF Signal Chain Discourse: Properties and Performance Metrics

Anton Patyuchenko, Field Applications Engineer

Introduction

It was not so long ago from the historical perspective, at the dawn of the 20th century, that the RF engineering underpinning any RF signal chain was a new emerging discipline. Today RF technology and radio frequency devices are so deeply ingrained in our lives that it is inconceivable how modern civilization could survive without them. There are countless examples of societal spheres that are heavily reliant on RF signal chains, which is the focus of our discourse.

However, before we delve into it, we need to understand what the term RF actually means. At first glance, this may seem like an easy question. We all know that RF stands for radio frequency, and a common definition ties this term to a specific range of frequencies extending from MHz to GHz portions of the electromagnetic spectrum. Yet, if we take a closer look at its acknowledged definitions and compare them, we come to realize that all of them define the actual boundaries of the RF portion of the spectrum differently. This becomes even more puzzling in light of the fact that we may often encounter a broader usage of this term in other contexts unrelated to specific frequencies at all. Then what is RF?

A consistent basis for its definition conveying more than one sense can be established by focusing on the distinguishing features of the RF, which include phase shift, reactance, dissipation, noise, radiation, reflections, and nonlinearity.[1] This basis represents a modern all-inclusive definition that does not rely on a single aspect or specific numerical values to distinguish RF from other terms. The term RF can be applied to any circuit or a component sharing a number of these features that underlie its definition.

Now that we have set the context for our discussion, we can move on to its main subject and consider the RF signal chain depicted in its generic form in Figure 1. Its representation uses a distributed-elements circuit model to account for the phase shift across the circuit, which is not negligible at shorter RF wavelengths, making the lumped circuit approximation inapplicable to these types of systems. An RF signal chain may include a broad variety of discrete components such as attenuators, switches, amplifiers, detectors, synthesizers, and other RF analog parts, along with high speed ADCs and DACs as well. All these components are combined to serve a specific application whose overall indicative performance will be determined by the composite performance of its constituent discrete parts.

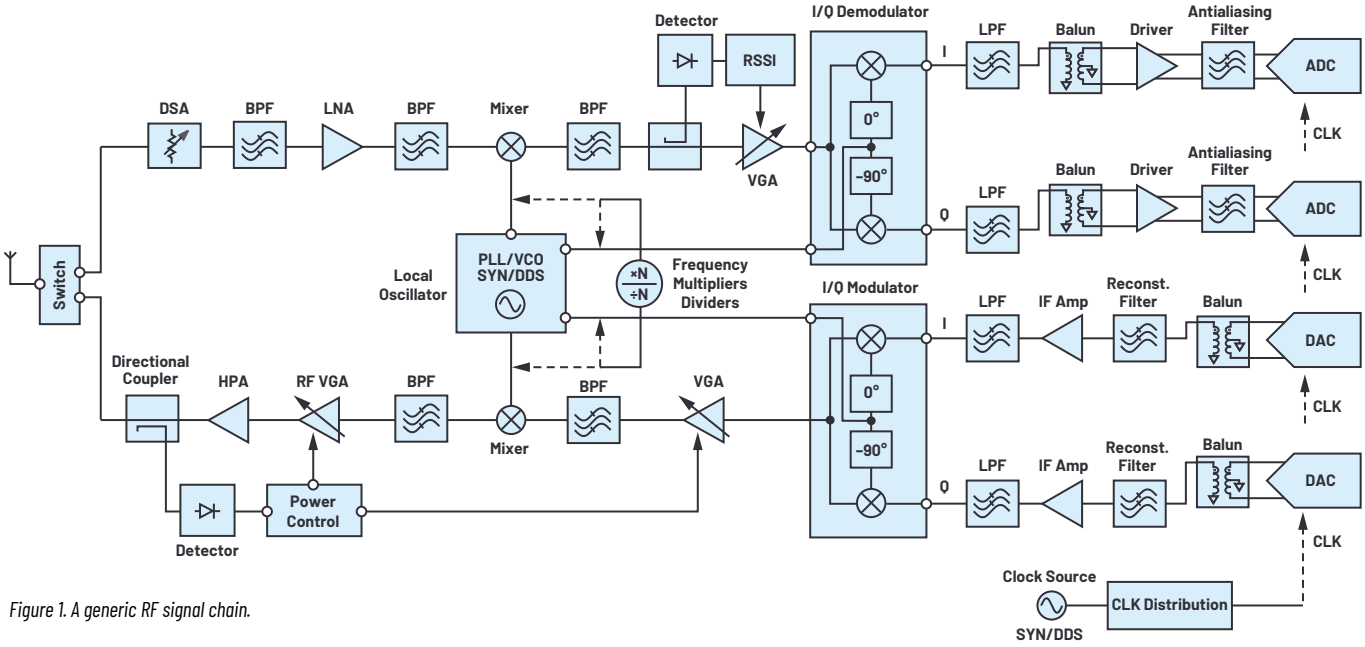

Figure 1. A generic RF signal chain.

Therefore, in order to design a system that would meet specific requirements imposed by the target application, an RF system engineer must attain a substantial system-level perspective and have consistent understanding of the key notions and principles underlying it. The importance of this knowledge has motivated the creation of this discourse, which consists of two parts. The goal of the first part is to provide a concise guidance on the main properties and metrics used to characterize RF devices and quantify their performance. The goal of the second part is to give a well-structured overview of a broad range of individual components and their types that can be used to develop RF signal chains for desired applications. In this article, we will focus on the first part of our discourse and consider the main properties and performance metrics associated with RF systems.

Introduction to RF Terminology

There is a wide range of specifications used for characterization of complete RF systems and their discrete building blocks. Depending on the application or use case, some of these characteristics might be of primary importance while the others are instead less critical or irrelevant. It is certainly not possible to perform a full comprehensive analysis of such a complex subject within the scope of this article. Nevertheless we will attempt to give a concise yet comprehensive overview of the most common RF performance aspects by following the common thread that should shape their complex constellation into a balanced and easy to understand guide to properties and characteristics of RF systems.

Fundamental Properties

Scattering matrix (or S-matrix) is the basic term one needs to know to describe the behavior of an RF system. An S-matrix allows us to represent even the most complex RF network as a simple N-port black box. A common example of a 2-port RF network (for example, an amplifier, filter, or attenuator) is shown in Figure 2, where V_n^+ is a complex amplitude of the voltage wave incident on port n, and V_n^- is a complex amplitude of the voltage wave reflected from port n.[2] When all its ports are terminated in matched loads, we can describe this network by the scattering matrix which elements, or S-parameters, quantify how RF energy propagates through the system in terms of a relationship between these voltage waves. Let us now use S-parameters to express the main properties of a typical RF network.

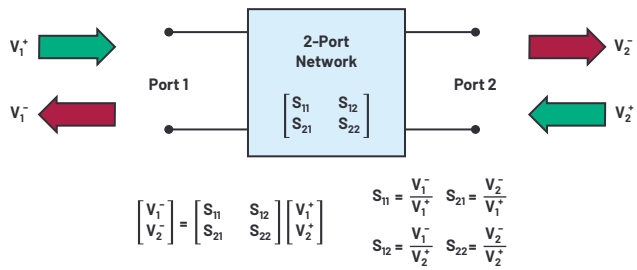

Figure 2. A 2-port network described by its S-matrix.

S_{21} is equivalent to the transmission coefficient from Port 1 to Port 2 for the case when the network is matched (S_{12} can be defined similarly). Its magnitude $|S_{21}|$ in logarithmic scale describes the ratio of the output power to the input power, which is known as gain or scalar logarithmic gain. This parameter is the key attribute of an amplifier and other RF systems in which it can take also negative values. Negative gain indicates intrinsic or mismatch losses usually expressed by its reciprocal quantity known as insertion loss (IL), which is a typical attribute of attenuators and filters.

If we now consider the incident and reflected waves at the same port, we can define S_{11} and S_{22} as shown in Figure 2. These terms are equivalent to the reflection coefficient $|\Gamma|$ at the corresponding port for the case when the other port is terminated in matched load. Using Equation 1, we can relate the magnitude of the reflection coefficient to return loss (RL):

$$RL = -20\ log(|\Gamma|) \quad (1)$$

Return loss describes a ratio of the power incident on the port to the power reflected back to the source. Depending at which port we estimate this ratio, we can distinguish between input and output return loss. Return loss is always a non-negative quantity that indicates how well the input or output impedance of the network is matched to the impedance seen at the port toward the source.

It is important to note that this simple relation of the IL and RL to the S-parameters is valid only for the case when all ports are matched, which is the main condition for the definition of S-matrix that describes the network itself. If the network is not matched it will not change its intrinsic S-parameters, but it may certainly change the reflection coefficients seen at its ports as well as the transmission coefficients between them.[2]

Frequency Range and Bandwidth

All these fundamental quantities that we have just described will continuously change across the frequency range, which is the basic characteristic common to all RF systems. It defines the frequencies at which these systems are operable and brings us to one more crucial performance measure—bandwidth (BW).

Although this term may refer solely to signal properties, some of its forms are used to describe RF systems that process these signals. In its general definition, bandwidth defines a range of frequencies confined by a certain criterion. However, it may have different meanings that vary depending on the specific application context. To make our discourse more complete, let us give brief definitions to some variations of its meaning:

- 3 dB BW is a span of frequencies at which signal power level is above half its maximum value.
- Instantaneous BW (IBW), or real-time BW, defines the maximum continuous bandwidth that a system is able to generate or acquire without retuning.
- Occupied BW (OBW) is a range of frequencies containing a specified percentage of the total integrated signal power.
- Resolution BW (RBW) in its general meaning describes the minimum separation between two frequency components that can still be resolved. For instance, in spectrum analyzer systems, it is the frequency span of the final filter stage.

These are just a few examples of various types of bandwidth definitions; however, regardless of its meaning, the bandwidth of an RF signal chain is largely determined by its analog front end as well as the sampling rate and bandwidth of a high speed analog-to-digital or digital-to-analog converter.

Nonlinearities

It needs to be mentioned that characteristic properties of an RF system vary not only across different frequencies, but also across different power levels of a signal. The fundamental properties we described in the beginning of this article are typically expressed using small signal S-parameters, which do not account for nonlinear effects. However, in a general case, a continuous increase in power level passing through an RF network often results in more pronounced nonlinear effects, ultimately degrading its performance.

When we talk about an RF system or a component with good linearity, we usually mean that the key metrics describing its nonlinear performance meet the requirements of our target application. Let us consider some of these key metrics that are commonly used to quantify nonlinear behavior of RF systems.

The first parameter we should consider defines the point at which a common device transitions from linear into nonlinear mode: the output 1 dB compression point (OP1dB). This is the output power level at which the gain of a system decreases by 1 dB. This is an essential characteristic of any power amplifier that sets operation of the device toward the level of saturation defined by the saturated output power (P_{SAT}). Power amplifiers generally belong to the final stages of a signal chain, and therefore these parameters usually define the output power range of an RF system.

Once the system is in a nonlinear mode, it starts distorting a signal, producing spurious frequency components, or spurs. Spurs are measured relative to the level of a carrier signal in dBc, and they can be classified into harmonics and intermodulation products (see Figure 3). A harmonic is a signal found at integer multiples of the fundamental frequency (for example, H1, H2, H3 harmonics), whereas the intermodulation products are signals that appear when two or more fundamental signals are present in a nonlinear system. If the first fundamental signal is at the frequency f_1 and the second is at f_2, then second-order intermodulation products are found at their sum and difference frequencies $f_1 + f_2$ and $f_2 - f_1$ as well as $f_1 + f_1$ and $f_2 + f_2$ (the latter are already known to us as H2 harmonics). The combination of the second-order intermodulation products and the fundamental signals results in third-order intermodulation products, two of which ($2f_1 - f_2$ and $2f_2 - f_1$) are especially critical since they are close to the original signals and therefore are not easy to filter. The output spectrum of a nonlinear RF system with spurious frequency components represents intermodulation distortion (IMD), which is an important term describing nonlinearity of the system.[2]

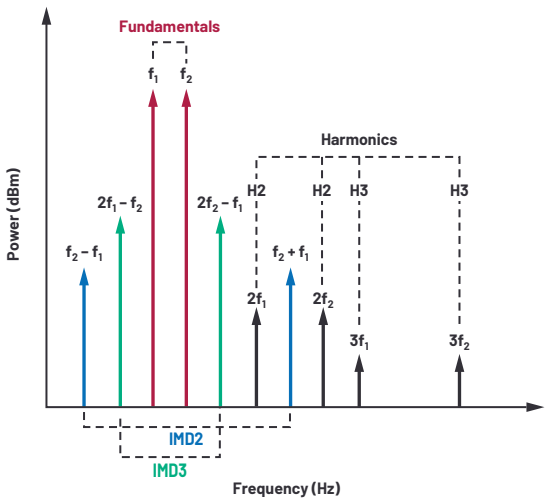

Figure 3. Harmonics and intermodulation products.

Spurious components associated with the second-order intermodulation distortion (IMD2) and third-order intermodulation distortion (IMD3) cause interference to the desired signals. The key figure of merit used to quantify the level of its severity is the intercept point (IP). We can distinguish the second-order (IP2) and third-order (IP3) intercept points. As depicted in Figure 4, they define hypothetical points for the input (IIP2, IIP3) and output (OIP2, OIP3) signal power levels at which the power of the corresponding spurious components would reach the same level of fundamental components. Although the intercept point is a purely mathematical concept, it is the paramount measure of RF system tolerance to nonlinear effects.

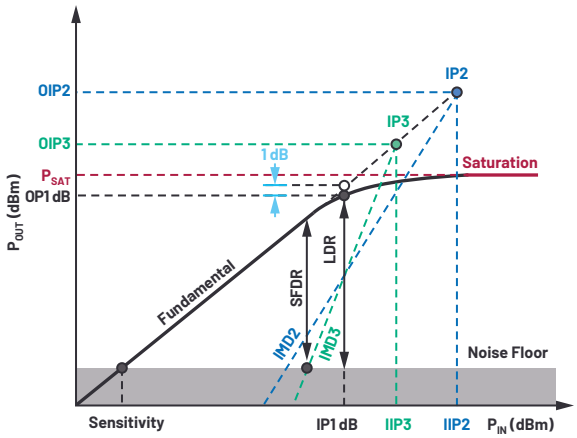

Figure 4. Definition of nonlinear characteristics.

Noise

Let us now consider another important attribute inherent to every RF system—noise. This term describes a fluctuation in an electrical signal that encompasses many different aspects. Depending on its spectrum and the way it affects a signal and mechanisms generating it, the noise can be categorized into many different types and forms. However, despite the existence of many different variations of noise sources, we do not need to delve into their physical properties in order to describe their ultimate impact on system performance. We can rely on a simplified noise model of a system that uses a single theoretical noise generator described by the key figure of merit known as noise figure (NF). It quantifies the degradation of the signal-to-noise ratio (SNR) caused by the system and defined as the logarithmic ratio of SNR at the output to that at the input. Noise figure expressed in a linear scale is called noise factor. This is the key attribute of any RF system that can govern its overall performance.

In the case of a simple linear passive device, the noise figure is equal to its insertion loss defined by $|S_{21}|$. In more complex RF systems consisting of multiple active and passive components, described by their individual noise factors, F_i, and power gains, G_i, the noise cascades down the signal chain according to the Friis formula (assuming that the impedances are matched at each stage):

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \quad (2)$$

From this we can conclude that the first two stages in an RF signal chain are the main contributors to the overall noise figure of the system. This is why the components with the lowest noise figure, such as low noise amplifiers, are used at the front ends of receiver signal chains.

If we now consider devices or systems used specifically for signal generation, for characterization of their noise performance, it is more common to refer to signal properties affected by their noise sources. These properties are phase jitter and phase noise, which are interrelated terms indicating signal stability in time (jitter) and frequency domain (phase noise). Which one is preferred depends usually on the application—for instance, in RF communications it is common to use the term phase noise, while in digital systems we will often see the term jitter. Phase jitter defines small fluctuations in the phase of a signal, while the phase noise describes its spectral representation, which is characterized by the noise power level relative to the carrier contained in 1 Hz bandwidth at various offsets from the carrier, and considered to be uniform across this bandwidth (see Figure 5).

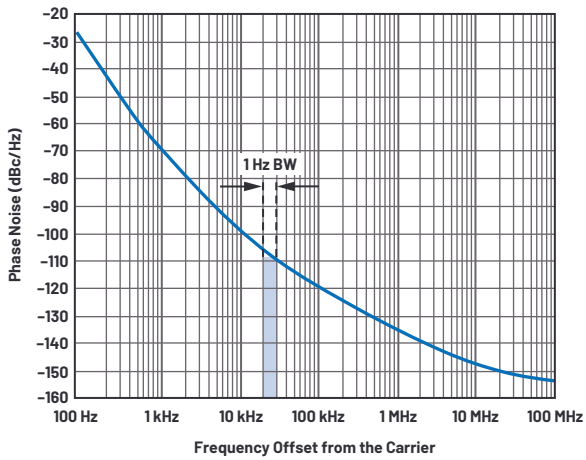

Figure 5. An example of a phase noise characteristic.

Multifold Derivatives

The most important figures of merit that we have considered so far underlie a broad range of derivative parameters utilized for performance quantification of RF signal chains in various application domains. For example, the combination of the terms noise and spurious results in the definition of the term dynamic range (DR). It describes the operating range for which a system has desirable characteristics. As shown in Figure 4, if this range is limited at the low end by noise and at the high end by the compression point, we talk about the linear dynamic range (LDR); and if its high end is defined by the maximum power level for which intermodulation distortion becomes unacceptable, we talk about the spurious-free dynamic range (SFDR). It should be noted that, depending on the application, actual definitions of the terms LDR and SFDR may vary.[2]

The lowest signal level that a system can handle to produce an output signal with a specified SNR defines another important characteristic typical for receiver systems known as sensitivity. It depends primarily on the system noise figure and signal bandwidth. The noise inherent to the receiver limits its sensitivity as well as other system specifications. For instance, phase noise or jitter in data communication systems will result in deviation of the constellation points in the eye diagram from their ideal locations, degrading the system's error vector magnitude (EVM) and contributing to higher bit error rate (BER).

Conclusion

There are numerous properties and performance metrics that can be used for the characterization of RF signal chains. They address different system aspects, and their importance and relevance may vary from one application to another. Although it is not possible to consider all of them in one article, substantial understanding of the fundamental characteristics discussed in this part of our discourse will allow an RF engineer to easily translate them into some of the key requirements and specifications of the target application whether it is a radar, communication, measurement, or any other RF system.

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References

[1] M. S. Gupta. "What Is RF?" *IEEE Microwave Magazine*, Vol. 2, No. 4. December 2001.

[2] David M. Pozar. *Microwave Engineering*, 4th Edition. Wiley, 2011.

About the Author

Anton Patyuchenko received his Master of Science in microwave engineering from the Technical University of Munich in 2007. Following his graduation, Anton worked as a scientist at German Aerospace Center (DLR). He joined Analog Devices as a field applications engineer in 2015 and is currently providing field applications support to strategic and key customers of Analog Devices specializing in RF applications. He can be reached at anton.patyuchenko@analog.com.

CTSD Precision ADCs—Part 3: Inherent Alias Rejection Made Possible

Abhilasha Kawle, Analog Design Manager and
Smita Choudhury, Design Evaluation Manager

In Part 3 of our CTSD precision ADCs article series, we will highlight the alias free nature of CTSD ADCs, which improves the immunity to interferers without any added peripheral design. Part 1 showcased a new class of easy to use, alias free precision ADCs based on continuous-time sigma-delta (CTSD) architecture that offers simple, compact signal chain solutions. Part 2 demystified the CTSD technology for signal chain designers. This article compares the design complexity behind alias rejection solutions for currently available precision ADC architectures. We will illustrate a theory to explain the inherent alias rejection of the CTSD ADC architecture. We also showcase how signal chain design can be simplified and discuss the extended advantages of CTSD ADCs. Finally, we will introduce new measurement and performance parameters to quantify alias rejection.

In many applications like sonar arrays, accelerometers, vibration analysis, etc., signals outside the signal bandwidth of interest are observed that are termed as interferers. The key challenge for signal chain designers is that the ADC sampling phenomenon causes these interferers to alias into the signal bandwidth of interest (in-band) and degrade the performance. Apart from this, in applications like sonar, the interferers aliasing in-band could be misinterpreted as an input signal, causing misdetection of objects around the sonars. The solutions to reject these aliases are one of the reasons why traditional ADC signal chain designs are quite complex. The unique inherent alias rejection property of CTSD ADCs provides a new simplified solution. Before arriving at this groundbreaking solution, our first stop for this article is at understanding the concept of aliasing.

Revisiting the Nyquist Sampling Theorem

To understand the concept of aliasing, let's have a quick recap of the Nyquist sampling theorem. One could analyze a signal in either the time domain or frequency domain. In the time domain, the sampling of an analog signal is represented mathematically as multiplication of the signal—for example, x(t) with an impulse train, δ(t), having time period T_s.

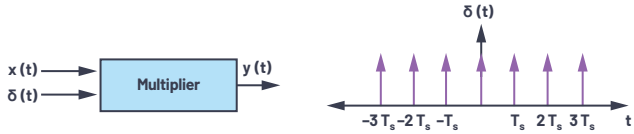


Figure 1. The time domain representation of a sampling process.

Equivalently in the frequency domain, the sampled output can be expressed using a Fourier series as,

$$Y(f) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(f - nf_s) \text{ where, } f_s = \frac{1}{T_s},\ n = 0, \pm1, \pm2, \ldots \quad (1)$$

Equation 1 simply means that if the frequency axis is unfurled, images of the input signal are formed at every integer multiple of sampling frequency, f_s.

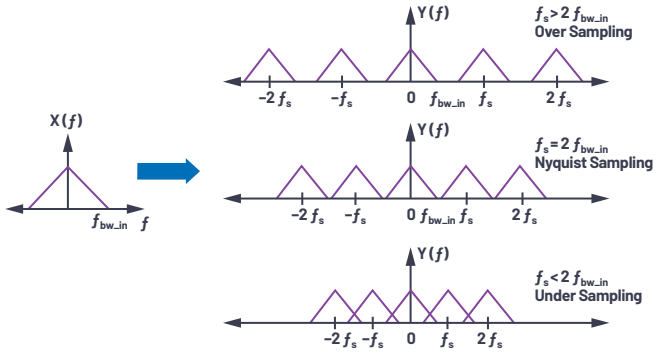


Figure 2. A representation of X(f) after being sampled by different sampling frequencies.

Equation 1 indicates that the signal content of X(f) at frequencies $f = n \times f_s - f_{IN}$, where n = 0, ±1, ±2, … …, will manifest itself at f_{IN} after sampling, similar to the under-sampling scenario in Figure 2, which illustrates the sampling phenomenon under various conditions.

$$\begin{aligned} Y(f) &= \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(f - nf_s) \\ &= \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(f_{in})\ \forall f = n \times f_s - f_{IN} \end{aligned} \quad (2)$$

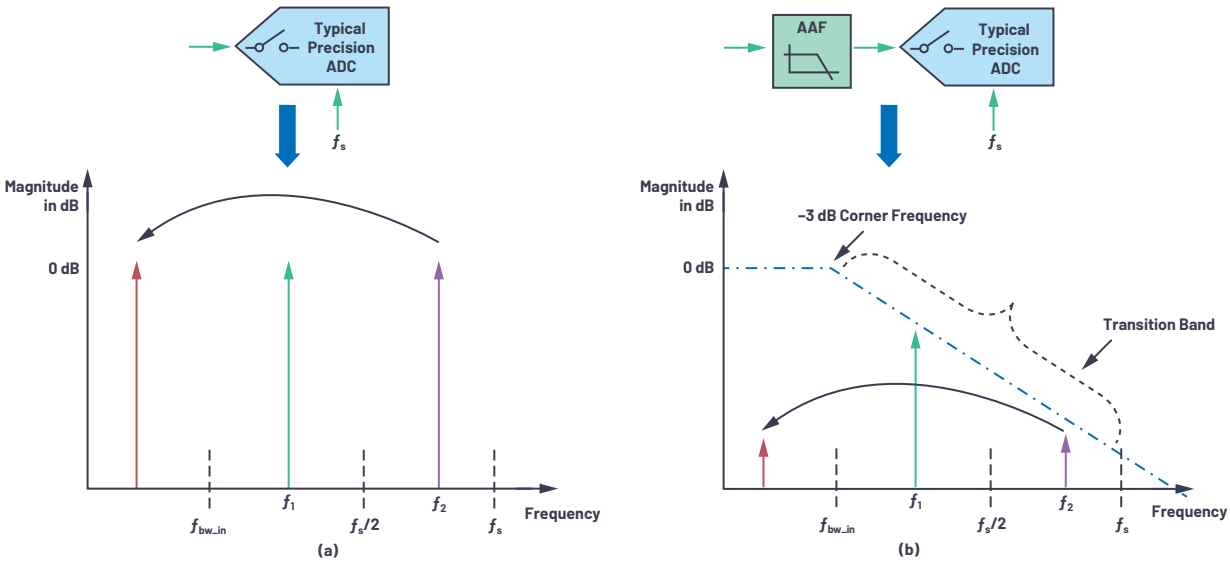


Figure 3. (a) Applying the sampling theorem to understand aliasing and (b) using the antialiasing filter to attenuate the aliasing frequencies.

In summary, the Nyquist theorem states that any signal greater than half the sampling frequency, folds or mirror backs to frequency less than $f_s/2$ and can potentially fall into the frequency band of interest.

Assume an ADC is sampling at frequency f_s and there are two out-of-band tones/interferers in the system, f_1 and f_2 at the ADC input as shown in Figure 3. Applying the Nyquist theorem, we can infer that since the frequency of tone f_1 is less than $f_s/2$, after sampling, its frequency remains the same. While the frequency of tone f_2 is greater than $f_s/2$, it will alias itself in the frequency band of interest, f_{bw_in}, and degrade the performance of the ADC in this region, as shown in Figure 3a.

This theory can also be extended to any noise beyond $f_s/2$, which also folds back and manifests itself in-band to increase the in-band noise floor and degrade performance.

An Incumbent Solution for Aliasing

A simple solution to avoid this performance degradation due to out-of-band (OOB) tone or noise foldback is to attenuate any signal content beyond $f_s/2$ before being sampled by the ADC using a low-pass filter, which is known as an antialiasing filter (AAF). Figure 3b shows the transfer function of a simple AAF and illustrates the attenuation-to-alias tone at frequency f_2 before it folds back in-band. The main characteristics of this AAF would be the order of the filter and –3 dB corner frequency. They are determined by pass-band flatness, the absolute attenuation required at certain frequencies (like sampling frequency) and the slope of attenuation required beyond input bandwidth (also called transition band). A few common filter architectures are Butterworth, Chebhesev, Bessel, and Sallen-Key, which can be implemented using passive RC and op amps. Filter design tools are available to assist signal chain designers with AAF design for given architecture and requirements.

Let's take an example application to understand the antialiasing filter requirements. In a submarine system, the sonar sensor emits sound waves and analyzes the echoes underwater to estimate the position and distance of surrounding objects. The sensor has input bandwidth of 100 kHz and the system detects any tone of magnitude >–85 dB at the ADC input as a valid source of echo. So, any interference from out-of-band would need to be attenuated by at least –85 dB by an ADC to avoid detection as input by the sonar system. For these requirements, in the next section we will build and compare the alias rejection solutions for different ADC architectures.

In traditional ADC architectures, such as successive approximation register (SAR) and discrete-time sigma-delta (DTSD) ADCs, the sampling circuit is at the analog input of the ADC, indicating that an AAF is required before the ADC input, as shown in Figure 3b.

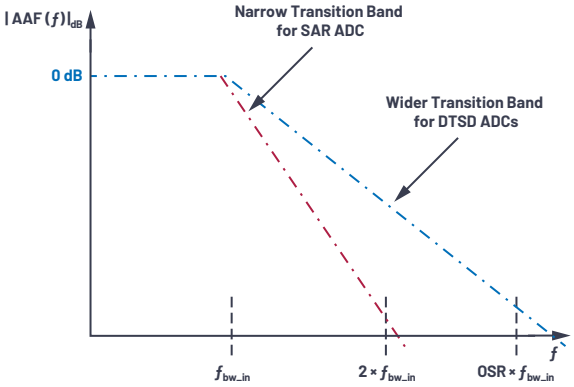
AAF Requirements for SAR/Nyquist Sampling ADCs

SAR ADCs generally have a sampling frequency set to two or four times the analog input frequency (f_{IN}). The AAF for such an ADC would need to have a narrow transition band beyond frequency f_{IN}, implying a very high order filter is required. From Figure 4, we can see that a SAR ADC with a sampling frequency of approximately 1 MHz requires a fifth-order Butterworth filter to get –85 dB rejection for frequencies greater than 100 kHz. In terms of filter implementation, as the order of filter increases, the number of passives and op amps required increases. This means an AAF for SAR ADCs requires significant power consumption and area budget in signal chain design.

AAF Requirements for DTSD ADCs

Sigma-delta ADCs are oversampled ADCs where sampling is much higher than the analog input frequency. And the region of aliasing to be considered for AAF design is $f_s \pm f_{IN}$. The transition band requirement for the filter would be from f_{IN} to very high f_s. This is a wider transition band in comparison with a SAR ADC AAF, showing that the order of AAF required is also lower. Figure 4 shows that, for a 6 MHz sampling frequency DTSD ADC, to get –85 dB rejection for frequencies around f_s – 100 kHz, a second-order AAF is generally required.

In a practical scenario, interferers or noise could be anywhere in the frequency band and not restricted to being around sampling frequency f_s. Any frequency tone less than $f_s/2$, like the tone at frequency f_1 in Figure 3, wouldn't manifest into in-band to degrade the ADC performance. Though the AAF may attenuate the tone f_1 to a certain extent, it is still present in the ADC output and is unnecessary information that must be processed by the external digital controller. Could this tone be further attenuated so that it is not seen at the ADC output? One solution could be to use an AAF with a narrow transition band beyond frequency f_{IN}, but then the filter design complexity would increase. Alternative solutions are on-chip digital filters that are part of sigma-delta modulator loops.



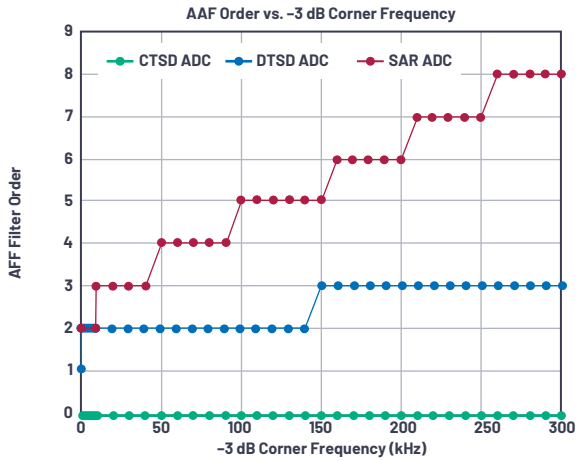


Figure 4. The complexity of an AAF vs. an ADC architecture vs. frequency band of interest.

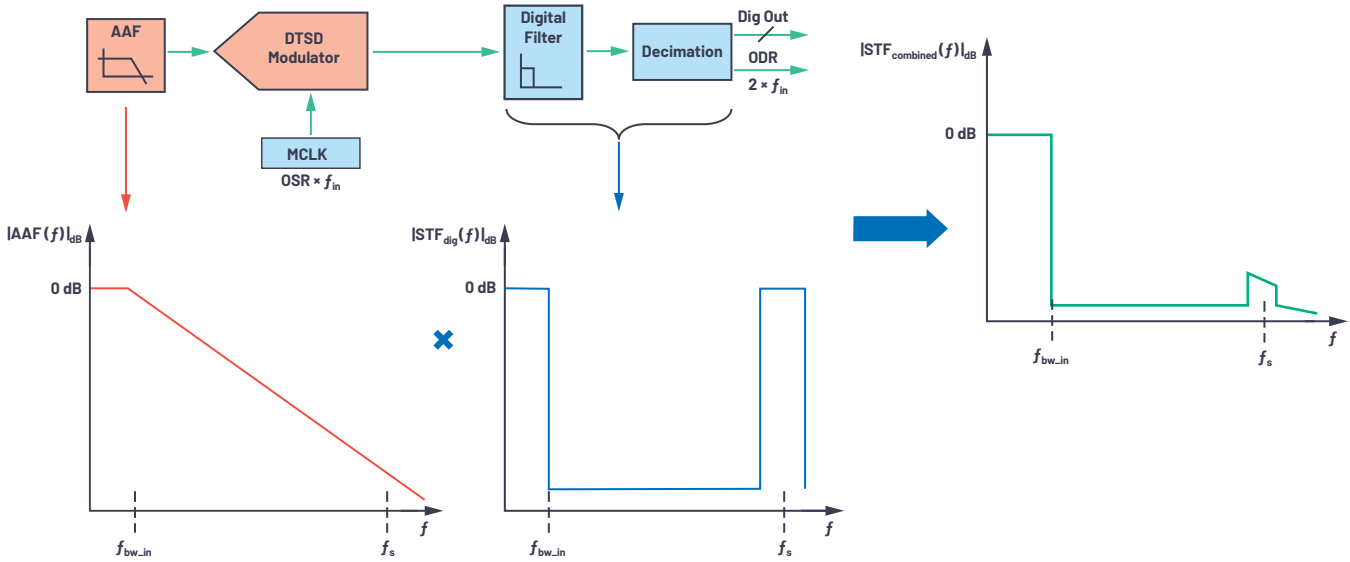


Figure 5. The STF of a DTSD ADC with an AAF at the front end and digital filters at the back end.

Digital Filters of Sigma-Delta Modulator Loops

In sigma-delta ADCs, because of oversampling and noise shaping, the modulator output contains a lot of redundant information and thus requires a large amount of processing by the external digital controller. This redundant information processing can be avoided if modulator data is averaged, filtered, and provided at a lower output data rate (ODR), which is generally $2 \times f_{IN}$. Decimation filters are used to convert the sampling rate from f_s to the required lower ODR. Sample rate conversion using a digital filter will be explained in future articles, but the key point here is that a discrete-time sigma-delta modulator is usually partnered with an on-chip digital filter. The combined signal transfer function (TF) for interferers with the analog filter in front and digital filter on the back end of a modulator is shown in Figure 5.

In conclusion, the AAF for a DTSD ADC is designed based on the attenuation required for tones around alias region f_s. And the tones in a non-aliasing region like f_1 are completely attenuated by the on-chip digital filters.

Back-End Digital Filter vs. Front-End Analog Filter

A SAR ADC requires a narrow transition band in an AAF, while a sigma-delta ADC requires a narrow transition band in a digital filter. Digital filters are low power and easy to integrate on-chip. Also, programming the order, bandwidth, and transition band of a digital filter is much simpler than with an analog filter.

Oversampling is advantageous in that it allows the use of a wide transition analog filter combined with a narrow transition digital filter on the back end, providing an optimized solution in terms of power, space, and immunity to interferers.

With the use of DTSD ADCs, the AAF requirements, though relaxed, add design complexity to meet settling time requirements after every sampling event to avoid performance degradation of a signal chain. The challenge for signal chain designers is to fine-tune the AAF to balance between alias rejection and output settling requirements.

The new class of precision CTSD ADCs simplifies the signal chain design by eliminating the need for front-end analog filter design.

The Inherent Alias Rejection of CTSD ADCs

In Part 2 of this series, a first-order CTSD modulator was built from a closed-loop resistive inverting amplifier, as shown in Figure 6. A CTSD modulator follows the same concept of oversampling and noise shaping as a DTSD modulator counterpart to achieve the desired performance, and has a resistive input rather than a switched capacitor input. The modulator building blocks include a continuous-time integrator, followed by a quantizer that samples and digitizes the integrator output and a feedback DAC that closes the loop at the input. Any noise at the input of a quantizer is noise shaped by the integrator's gain transfer function.

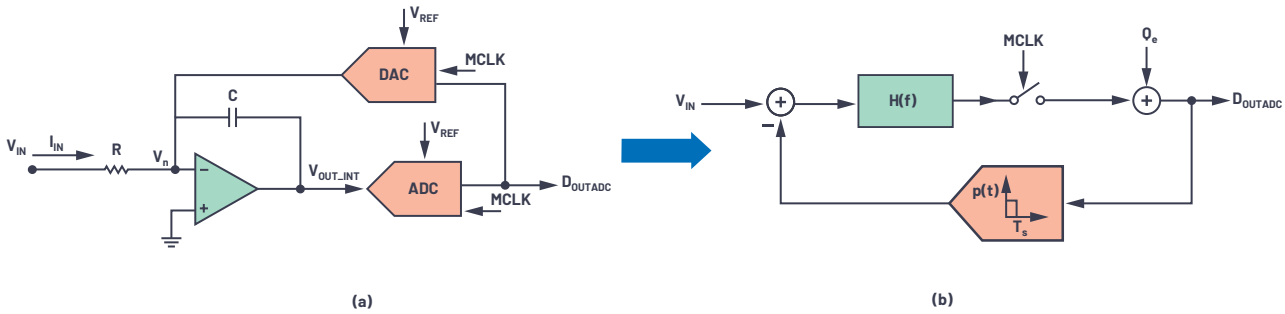


Figure 6. (a) The building blocks of a CTSD modulator loop and (b) a simplified block representation for mathematical analysis.

Expanding on the information from Part 2, a simplified block representation for a CTSD modulator loop can be drawn with the following mathematical models:

- The integrator transfer function is generalized as H(f) and is also known as a loop filter. For a first-order integrator, H(f) = 1/2πRC .
- The functionality of the ADC is sampling and quantization. So, a simplified ADC model for analysis uses a sampler followed by an additive quantization noise source.
- The DAC is a block that multiplies in the input in the present clock cycle with a constant. So, it's a block with an impulse response that is constant during the sampling clock period and 0 the rest of the time.

The equivalent block diagram with these simplified models is shown in Figure 6b and is widely used for sigma-delta performance analysis. The transfer function from V_{IN} to V_{OUT} is called signal TF (STF) and the Q_e to output is termed as noise TF (NTF).

One reasonable explanation about the inherent alias rejection property of a CTSD modulator loop would be that sampling occurs not directly at the input of the modulator but after the loop filter, H(f) as shown in Figure 6a. But to get a complete picture, a linear model without a sampler would be used to understand the concepts and the analysis would be extended to loop with the sampler.

Step 1: STF and NTF Analysis Using a Linear Model

Ignoring the sampler for analysis simplification, the linear model would be as shown in Figure 7. The STF and NTF for this loop can be represented as

$$V_{OUTADC} = V_{IN} \times \frac{H(f)}{1 + H(f)} + Q_e \times \frac{1}{1 + H(f)} = V_{IN} \times STF(f) + Q_e \times NTF(f) \quad (3)$$

From Equation 3, the STF can be rewritten as

$$STF(f) = H(f) \times NTF(f) \quad (4)$$

The frequency bandwidth of interest is low frequency, so mathematically it can be represented as f⟶0, while high frequency can be represented as f⟶∞. The magnitude of STF and NTF in dB as a function of frequency when plotted would be as shown in Figure 7.

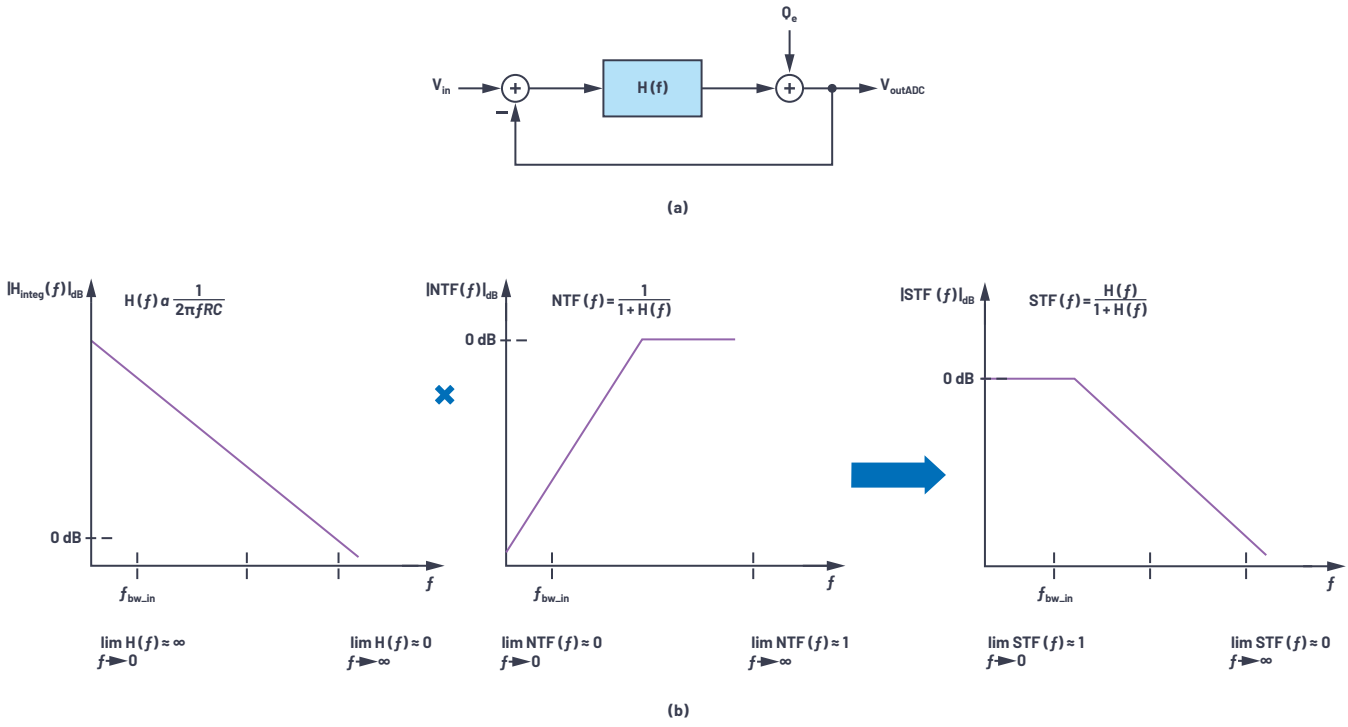


Figure 7. (a) A linear model for simplified analysis and (b) STF(f) = H(f) × NTF(f).

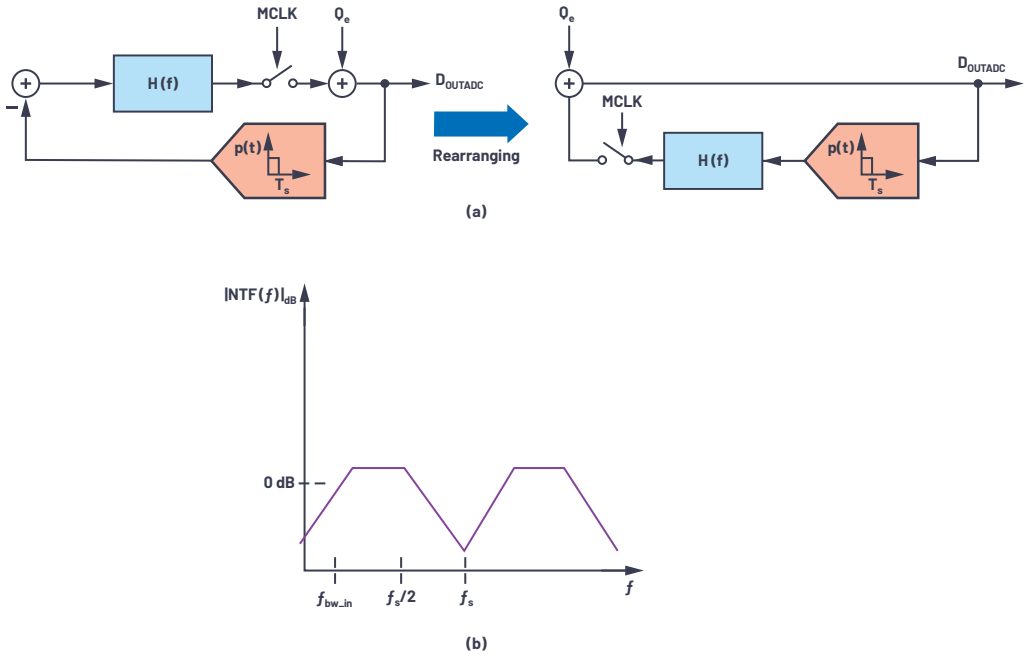


Figure 8. (a) A CTSD modulator loop diagram with input = 0 V and (b) an NTF of a modulator loop.

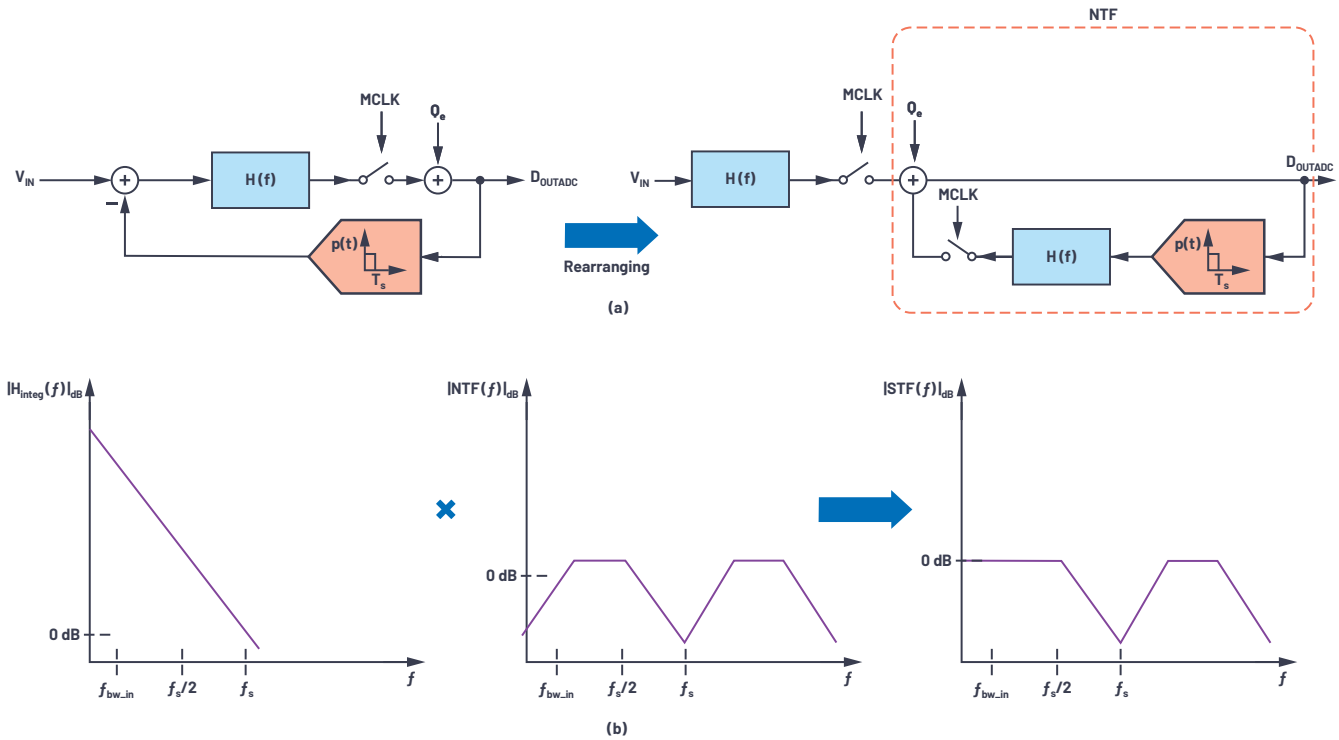


Figure 9. Rearrangement of the modulator loop to illustrate the inherent alias rejection.

The NTF resembles a high-pass filter and the STF resembles a low-pass filter with flat 0 dB magnitude for the frequency band of interest and attenuation for higher frequencies that is equivalent to AAF TF. Mathematically, the signal passes through H(f), which has a high gain, low-pass filter profile and then is processed by the NTF loop. Now this understanding can be extended to loop with the sampler by first understanding the NTF block representation.

Step 2: Block Diagram Representation for NTF

With input V_{IN} set to 0 V, the block diagram of the modulator loop can be rearranged as shown in Figure 8a and used for NTF representation. With the sampler in the loop, the NTF response would be similar to a linear model, but with replicated images at every multiple of f_s, as shown in Figure 8b.

Step 3: Rearranging the Modulator Loop to Visualize Upfront Filtering Action

If the loop filter H(f) and sampler of the modulator loop are moved to the input and feedback is as shown in Figure 9, there is no change with regards to the transfer function from input to output. The right side of this rearranged block diagram represents the NTF.

Similar to the linear model from Step 1, in the sampled equivalent system the input signal traverses through high gain H(f), and then is sampled and processed through the NTF loop. The transversal of a signal through a loop filter creates a low-pass filter profile before it is sampled. This profile leads to the inherent alias rejection of a CTSD modulator. Thus, the STF for a CTSD modulator loop is as shown in Figure 9.

Step 4: Complete STF with a Digital Filter

To reduce the redundant high frequency information, the CTSD modulator is partnered with on-chip digital decimation filters and the combined alias rejection TF is shown in Figure 10. Alias from around f_s is attenuated by the inherent alias rejection property of a CTSD while intermediate interferers are attenuated by a digital filter.

Figure 4 compares the order of AAF required for SAR ADCs, DTSD ADCs, and CTSD ADCs for –80 dB rejection at the sampling frequency vs. the input signal bandwidth. The order and, hence, complexity of AAF with SAR ADCs is the highest, while CTSD ADCs don't require an external AAF as alias rejection is inherent to their design.

The Signal Chain Advantages Made Possible by a CTSD Architecture

In certain multichannel applications like sonar beamforming and vibration analysis, the phase information between channels is important. For example, the phases between channels need to be accurately matched with a requirement of 0.05° at 20 kHz.

For traditional ADC signal chains, the AAFs are designed using passive RC and op amps. The filter causes a certain magnitude and phase droop in-band that would be a function of corner frequency. For good channel-to-channel phase matching, all the channels need to have the same droop, which indicates the corner frequency of the filters for each channel need to be finely controlled and matched. A second-order Butterworth filter designed for –80 dB rejection at 16 MHz (sampling frequency) and f_{3dB} of 160 kHz (input bandwidth) could have phase mismatch of ±0.15° at 20 kHz with error tolerance of as low as 1% on the absolute values of RC. The availability of lesser error tolerance RC passives is limited and increases the bill of material (BOM).

Since the AAF is eliminated in a CTSD ADC signal chain, the channel-to-channel magnitude and phase matching is inherently achieved in the frequency band of interest. The phase mismatch is limited by on-chip mismatches of analog modulator loop design, which could be as low as ±0.02° at 20 kHz.

Measuring and Quantifying the Inherent Alias Rejection

New functional checks to measure the alias rejection are introduced in the ADC data sheet of AD4134, which is a precision ADC based on the CTSD ADC architecture. The frequency of the analog input signal of the ADC is swept, and the impact of each out-of-band input signal is calculated by measuring the magnitude of tone folded back, if any, for the test frequency, with respect to the magnitude of the applied tone.

Figure 11 shows the alias rejection of AD4134 for out-of-band frequencies in the performance bandwidth of 160 kHz with a sampling frequency of 24 MHz. For a frequency of 23.84 MHz (f_s – 160 kHz), alias rejection is –85 dB, which is the alias rejection specification of the ADC. It can also be observed that the rejection is better than –100 dB for other intermediate frequencies. Further details on inherent alias rejection with options to further increase this rejection can be found in the AD4134 data sheet.

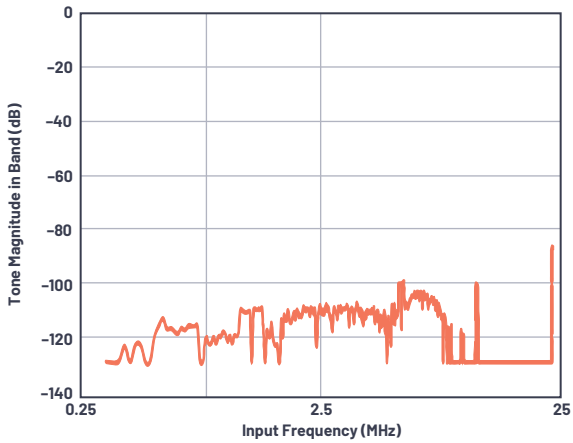


Figure 11. Alias rejection vs. the out-of-band frequency.

The CTSD ADC concepts explained so far can help signal chain designers envision the unique properties of the resistive input, resistive reference, and inherent alias rejection of this architecture. An easy to drive input and reference coupled with the elimination of AAF design for CTSD ADC signal chains, has led to a new simplified ADC front-end design for various applications. Look for the next part of this series to learn more about these simplified precision signal chain designs!

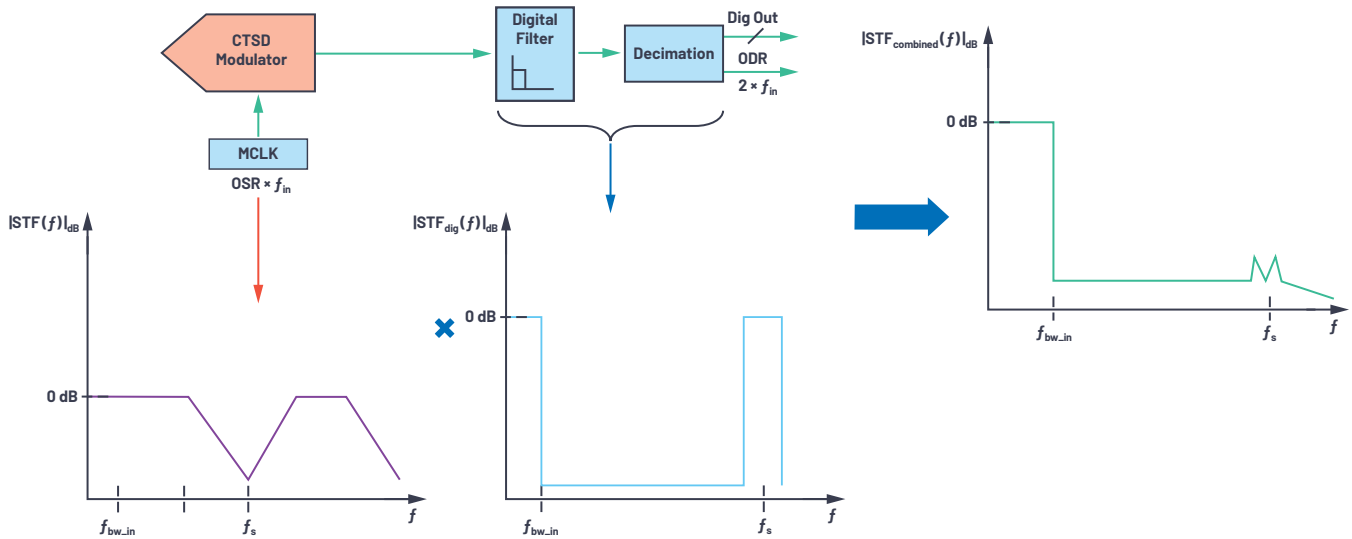


Figure 10. A CTSD modulator loop with back-end digital filters.

Acknowledgements

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References

Antialiasing Filter Design Tool

Filter Design Tutorial

Kawle, Abhilasha and Wasim Shaikh. "CTSD Precision ADCs—Part 1: How to Improve Your Precision ADC Signal Chain Design Time." *Analog Dialogue*, Vol. 55, No. 1, February 2021.

Kawle, Abhilasha. "CTSD Precision ADCs—Part 2: CTSD Architecture Explained for Signal Chain Designers." *Analog Dialogue*, Vol. 55, No. 1, March 2021.

Kester, Walt. "MT-002: What the Nyquist Criterion Means to Your Sampled Data System Design." Analog Devices, Inc., 2009.

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Optimizing Power Systems for the Signal Chain—Part 2: High Speed Data Converters

Patrick Errgy Pasaquian, Senior Applications Engineer, and
John Martin Dela Cruz, Applications Engineer

Introduction

In Part 1 of this power system optimization series, we examined how power supply noise sensitivity can be quantified and how these quantities can be connected to real effects in the signal chain. The question was asked: What are the real noise limits to achieve superior performance of high performance analog signal processing devices? Noise is just one measurable parameter in designing a power distribution network (PDN). As noted in Part 1, a pure focus on minimizing noise can come at the cost of increased size, higher cost, or lower efficiency. Optimizing a power distribution network improves these parameters, while lowering noise to necessary levels.

This article builds on the generalized overview of the effects of power supply ripple in high performance signal chains. Here, we dive deeper into the details of optimizing power distribution networks for high speed data converters. We compare a standard PDN to an optimized PDN to see where gains can be made in space, time, and cost. Subsequent articles will explore specific optimization solutions for other signal chain devices, such as RF transceivers.

Power System Optimization for the AD9175 Dual 12.6 GSPS High Speed Digital-to-Analog Converter

The AD9175 is a high performance, dual, 16-bit digital-to-analog converter (DAC) that supports DAC sample rates up to 12.6 GSPS. The device features an 8-lane, 15.4 Gbps JESD204B data input port; a high performance, on-chip DAC clock multiplier; and digital signal processing capabilities targeted at single-band and multiband direct to radio frequency (RF) wireless applications.

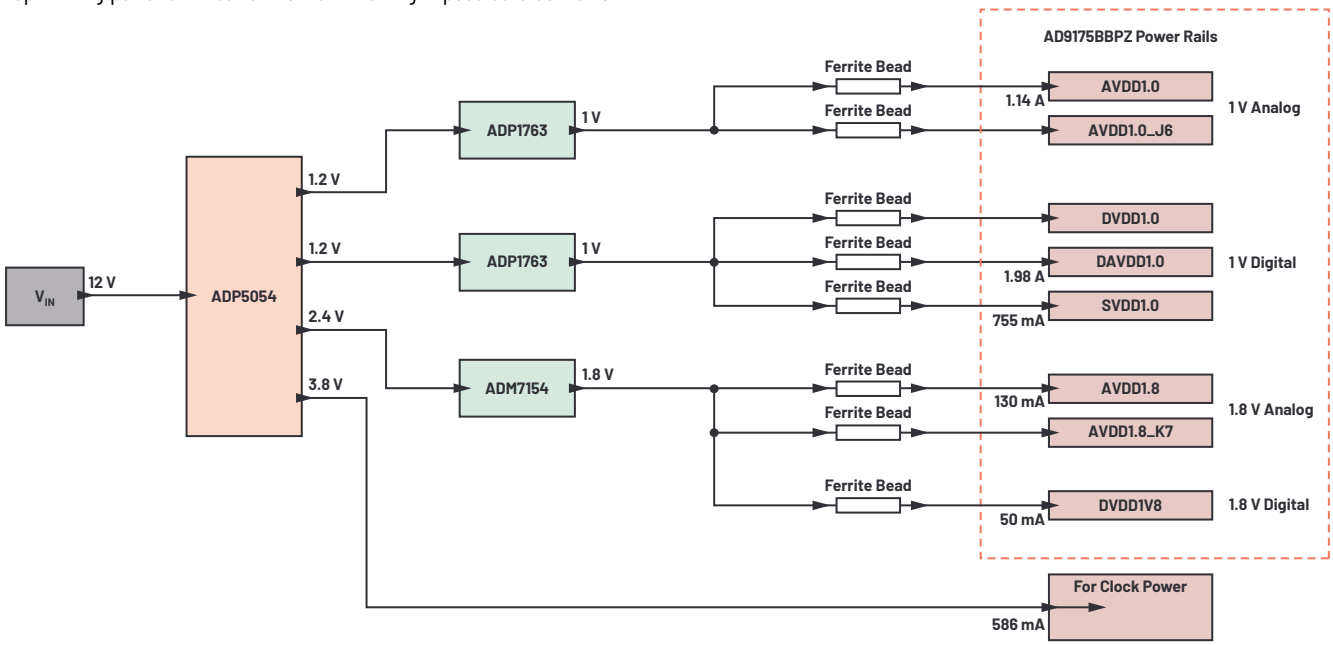


Figure 1. Standard PDN of an AD9175 high speed DAC, which comes on the off-the-shelf evaluation board.

Let's look at optimizing a PDN for this dual high speed DAC. Figure 1 shows the standard power distribution network for the AD9175 high speed DAC as installed on the off-the-shelf evaluation board. The PDN comprises an ADP5054 discrete quad switcher and three low dropout (LDO) postregulators. The goal is to see if this PDN can be improved and simplified, while ensuring its output noise does not cause any significant degradation in the DAC performance.

The AD9175 requires eight power rails, which can be collected into four groups, namely:

- 1 V analog (two rails)
- 1 V digital (three rails)
- 1.8 V analog (two rails)
- 1.8 V digital (one rail)

Analysis: Noise Requirements

Before we can optimize anything, we must understand the power supply sensitivity of these rails. We will focus on the analog rails, as they tend to be more sensitive to noise than the digital rails.

The power supply modulation ratio (PSMR) of the analog rails is shown in Figure 2. Note that the 1 V analog rails are relatively more sensitive at the 1/f frequency region, while the 1.8 V analog rails are more sensitive in the range of switching converter operating frequencies (100 kHz to around 1 MHz).

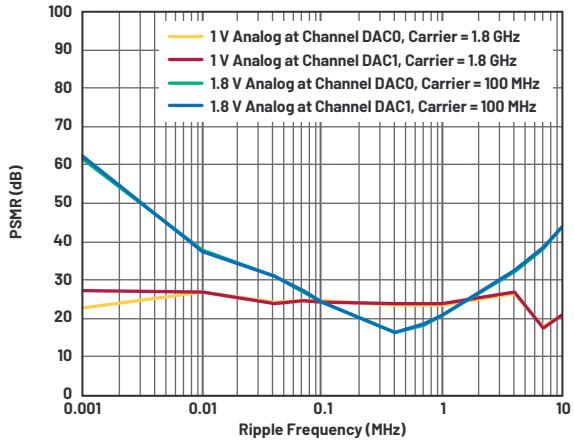


Figure 2. AD9175 high speed DAC PSMR at 1 V analog and 1.8 V analog rails.

One approach to optimization is to use a low noise switching regulator with an LC filter. Figure 3 shows the conducted spectral output of the LT8650S Silent Switcher® regulator (with and without an LC filter) with spread spectrum frequency modulation (SSFM) mode off. As discussed in Part 1, SSFM reduces the switching frequency noise amplitude but introduces noise peaks in the 1/f region due to the triangular modulation frequency. This added noise would exceed the maximum allowable ripple threshold for this rail as the 1/f noise already has a small margin from that threshold. Thus, SSFM is not recommended to be used in this case. The maximum allowable voltage ripple threshold represents the power supply ripple level at which when exceeded, sideband spurs in the DAC carrier signal appear above the 1 µV p-p noise floor of the DAC output spectrum. It can be seen from these results that the 1/f noise of the switching regulator does not exceed the maximum allowable ripple threshold of the 1 V analog rail. Also, an LC filter is sufficient to knock down the fundamental switching ripple and harmonics of LT8650S below the maximum allowable ripple threshold.

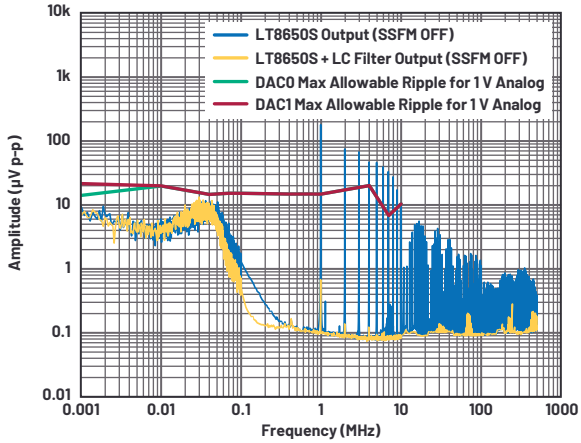


Figure 3. LT8650S conducted spectral output vs. maximum allowable ripple threshold for the 1 V analog rail.

Figure 4 shows the conducted spectral output of the LT8653S (with and without an LC filter). Also shown is the maximum allowable voltage ripple for the 1.8 V rail that will not produce spurs in the 1 µV p-p noise floor of the AD9175 output spectrum. It can be seen that the 1/f noise of the LT8653S does not exceed the maximum allowable ripple threshold, and an LC filter is sufficient to knock down the fundamental switching ripple and harmonics of LT8653S below the maximum allowable ripple threshold.

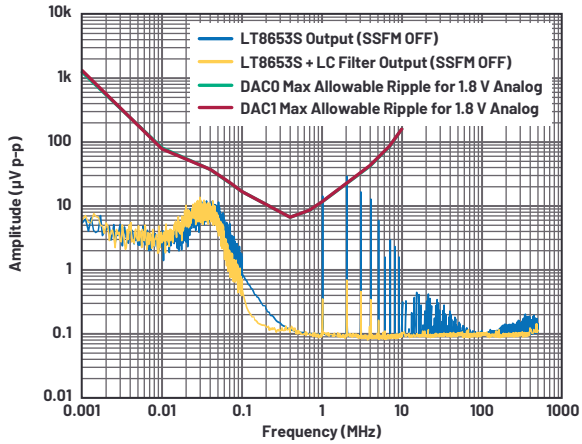


Figure 4. LT8653S conducted spectral output vs. maximum allowable ripple threshold for the 1.8 V analog rail.

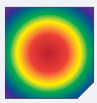
Results: Optimized PDN

Figure 5 shows an optimized power distribution network of AD9175. The goal is to raise efficiency and reduce space requirements and power loss over the PDN in Figure 1 while achieving AD9175 superior dynamic performance. The noise goals are based on the maximum allowable ripple threshold shown in Figure 3 and Figure 4.

The optimized power distribution network consists of LT8650S and LT8653S Silent Switcher regulators followed by LC filters on the analog power rails. In this PDN, the 1 V analog rail is powered by the V_{OUT1} of the LT8650S followed by an LC filter; the 1 V digital rail is directly powered by the V_{OUT2} of the same LT8650S, no LC filter required. For the AD9175, the digital rails are less sensitive to power supply noise, so directly powering these rails is possible without degrading the DAC dynamic performance. The LT8653S with LC filter directly powers the 1.8 V analog and 1.8 V digital rails.

Table 1 compares the performance of the optimized PDN to the standard PDN shown in Figure 1—a quad buck switcher with three LDO regulators. The component area reduction of the optimized solution is 70.2% over the standard. Furthermore, efficiency is increased to 83.4% (from 69.2%) with an overall power saving of 1.0 W.

Table 1. Comparison of an AD9175 Optimized PDN to the Standard PDN

	Standard PDN (Figure 1)	Optimized PDN (Figure 5)	Improvement of the Optimized PDN from the Standard PDN
Component Area	142.4 mm² 	42.4 mm² 	70.2%
Overall Efficiency	69.2% 	83.4% 	14.2%
Power Loss	1.8 W 	0.8 W 	1.0 W

To verify that the noise performance of the optimized PDN did not degrade the dynamic performance of the DAC, the AD9175 is evaluated in terms of phase noise and inspecting the DAC output spectrum of sideband spurs around the carrier.[1] Phase noise results are comparable between the standard PDN and optimized PDN, as shown in Table 2. The output spectrum of AD9175 has a clean carrier frequency with no visible sideband spurs, as shown in Figure 6.

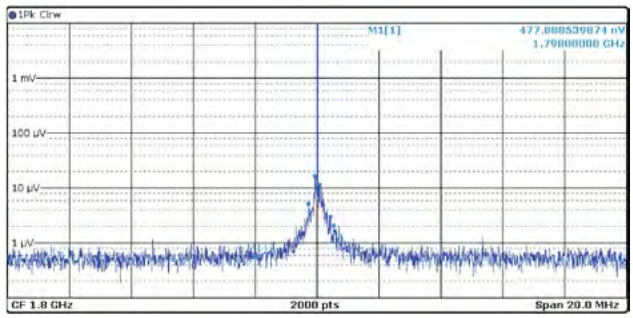


Figure 6. AD9175 output spectrum (at 1.8 GHz, –7 dBFS carrier) using the optimized PDN.

Table 2. AD9175 Phase Noise Performance Using the Standard PDN and Optimized PDN

Frequency Offset	Phase Noise (dBc/Hz)			
	Standard PDN (Figure 1)		Optimized PDN (Figure 5)	
	DAC0	DAC1	DAC0	DAC1
1.0 kHz	–91	–91	–91	–91
10.0 kHz	–99	–99	–99	–99
100.0 kHz	–110	–110	–110	–110
600.0 kHz	–125	–125	–125	–125
1.2 MHz	–134	–134	–134	–134
1.8 MHz	–137	–137	–137	–137
6.0 MHz	–148	–148	–148	–148

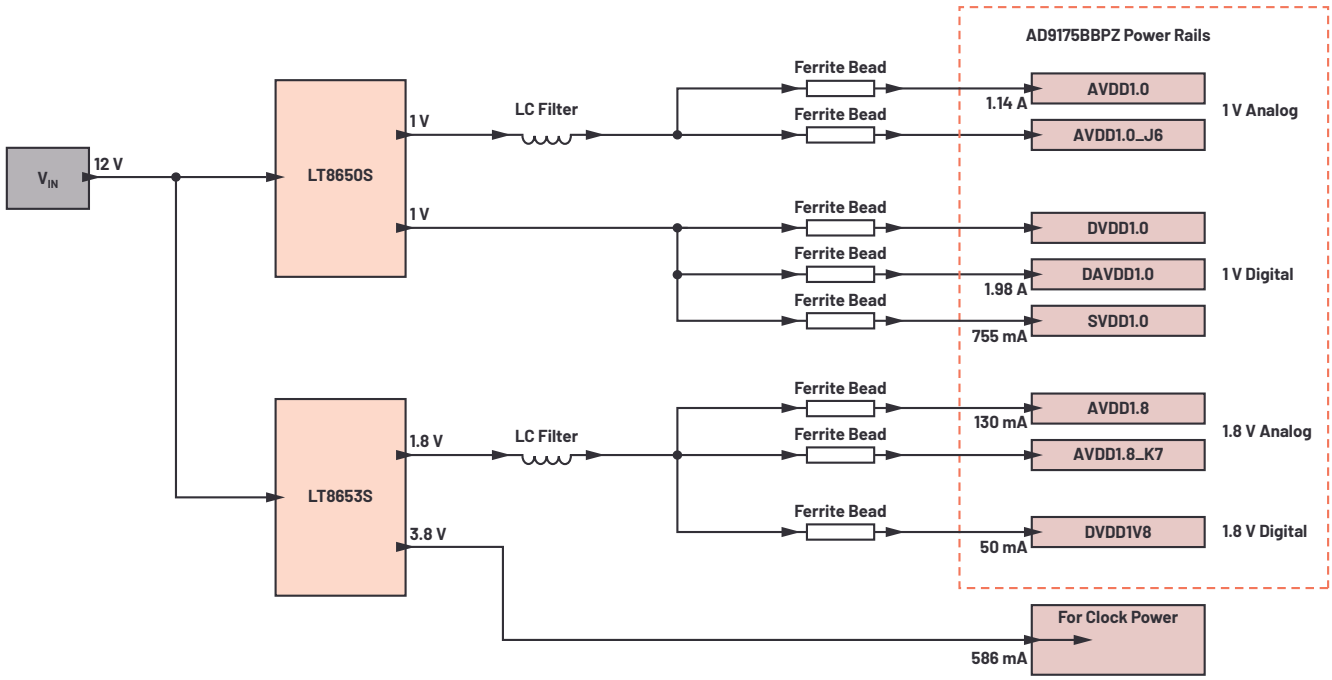


Figure 5. Optimized PDN for an AD9175 high speed DAC.

Power System Optimization for the AD9213 10.25 GSPS High Speed Analog-to-Digital Converter

The AD9213 is a single, 12-bit, 6 GSPS or 10.25 GSPS, radio frequency (RF) analog-to-digital converter (ADC) with a 6.5 GHz input bandwidth. The AD9213 supports high dynamic range frequency and time domain applications requiring wide instantaneous bandwidth and low conversion error rates (CER). The AD9213 features a 16-lane JESD204B interface to support maximum bandwidth capability.

Figure 7 shows a standard power distribution network for the AD9213 high speed ADC—as found on the off-the-shelf evaluation board—consisting of an LTM4644-1 µModule® quad switcher and two linear regulators. This solution is fairly space efficient and energy efficient, but can it be improved? As noted throughout this series, the first step to optimization is quantifying the sensitivity of AD9213—that is, realistically setting the limits of PDN output noise so it does not cause significant degradation in the ADC performance. Here we'll look at an alternate PDN solution using two µModule regulators and compare its performance against the standard off-the-shelf solution.

The AD9213 10 GSPS ADC requires 15 different power rails, collected into four groups:

- 1 V analog (three rails)
- 1 V digital (six rails)
- 2 V analog (two rails)
- 2 V digital (four rails)

Analysis: Noise Requirements

The optimized solution we're exploring replaces an LTM4644-1 µModule quad switcher and two linear regulators with two µModule regulators, the LTM8024 and the LTM8074, and a single LDO postregulator.

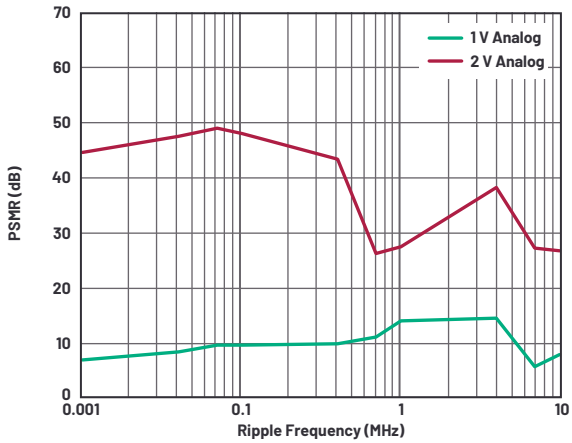


Figure 8. AD9213 high speed ADC PSMR of 1 V analog and 2 V analog rails at a 2.6 GHz carrier frequency.

Figure 8 shows the PSMR results for 1 V analog and 2 V analog power rails of the AD9213 at a 2.6 GHz carrier frequency. The 1 V analog rail is more sensitive than the 2 V analog rail due to a lower PSMR.

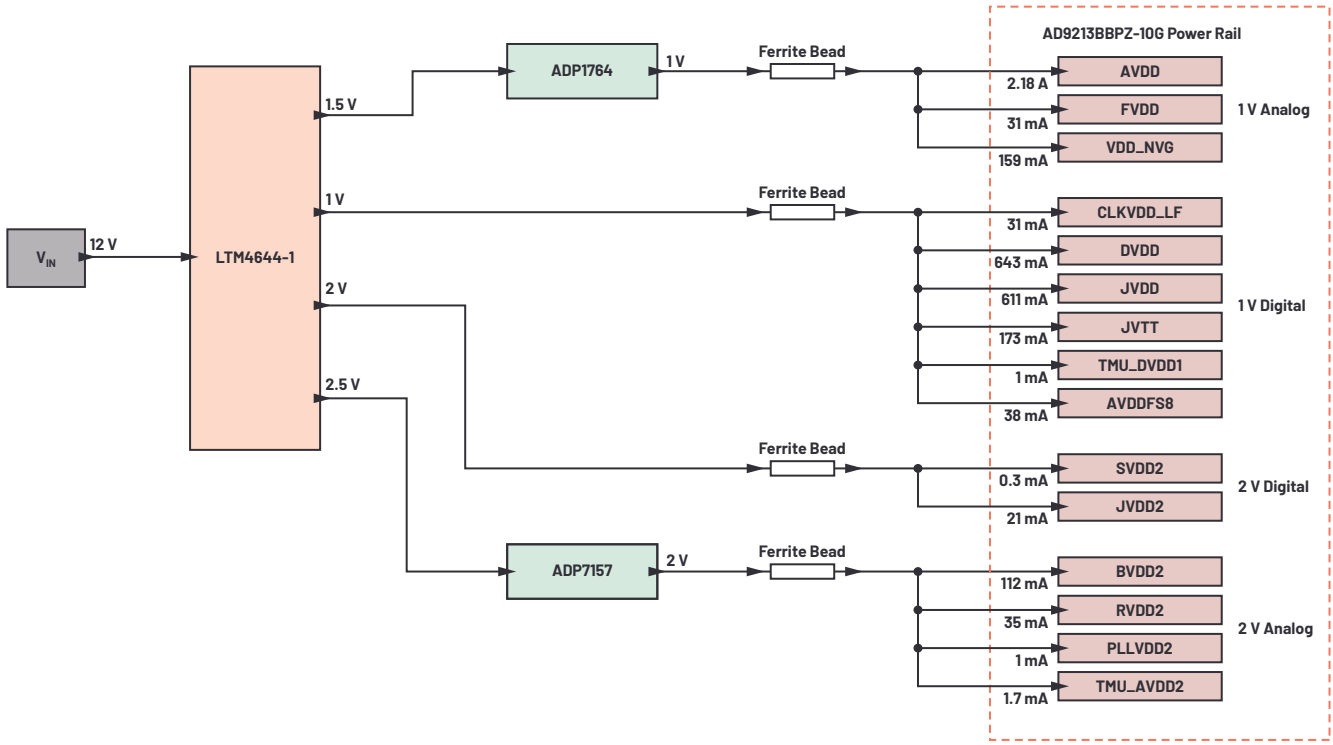


Figure 7. Standard PDN of an AD9213 high speed ADC, which comes on the off-the-shelf evaluation board.

Figure 9 shows the spectral output of the LTM8024 (with and without an LDO regulator) in forced continuous mode (FCM). Also shown is an overlay of the maximum allowable voltage ripple threshold that will not produce spur in the -98 dBFS noise floor of the AD9213 output spectrum. The unfiltered 1/f noise and fundamental switching spur of LTM8024 output exceed the maximum allowable ripple threshold when directly powering the 1 V analog rail.

Adding an ADP1764 LDO postregulator to the LTM8024 reduces the 1/f noise and fundamental switching ripple and its harmonics down to the maximum allowable ripple threshold, which is also shown in Figure 9. Some overhead voltage is required at the input of the linear regulator. In this case, a 1.3 V output is used from the LTM8024 to the input of the postregulator. This 300 mV meets the recommended headroom voltage specification of the LDO regulator while minimizing power loss in it; this is slightly better than the 500 mV in the standard solution.

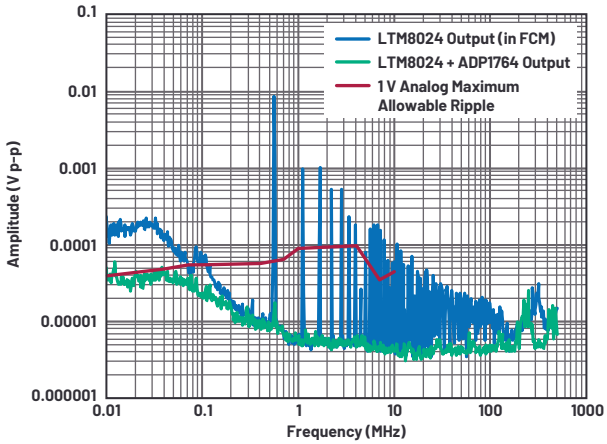


Figure 9. The LTM8024 spectral output vs. the maximum allowable ripple threshold for the 1 V analog rail.

Addressing the 2 V rails: Figure 10 shows the spectral output of the LTM8074 µModule regulator (with and without an LC filter) in FCM. The maximum allowable voltage ripple threshold is also shown. This threshold represents the power supply ripple level at which when exceeded, sideband spurs in the ADC carrier signal appear above the -98 dBFS noise floor of the AD9213 output spectrum. Here, similar to the 1 V analog rail, the regulator switching spurs exceed the maximum allowable ripple threshold when directly powering the 2 V analog rail. An LDO regulator is not required, though. Instead, an LC filter at the LTM8074 output reduces the switching spur below the maximum allowable ripple threshold.

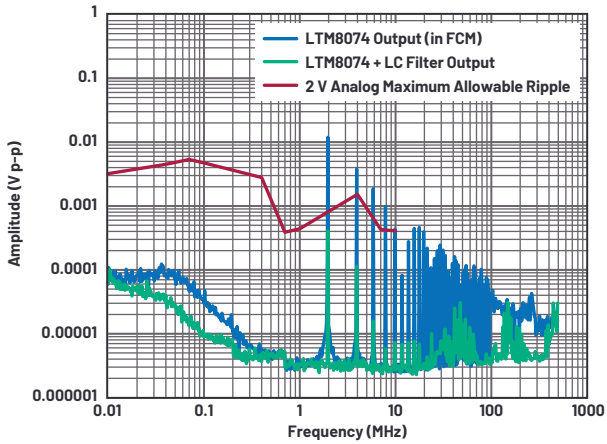


Figure 10. The LTM8074 spectral output vs. the maximum allowable ripple threshold for the 2 V analog rail.

Results: Optimized PDN

Figure 11 shows the optimized power distribution network resulting from the power supply sensitivity evaluation results. Like the standard solution, it uses three power ICs; in this case, an LTM8024, LTM8074, and ADP1764. In this solution, the LTM8024 µModule regulator V_{OUT1} is postregulated by the ADP1764 to power the relatively sensitive 1 V analog rail. The 1 V digital rail is directly powered by V_{OUT2} of LTM8024. Much like the AD9175 DAC, the AD9213's digital rails are less sensitive to power supply noise, so directly powering these rails is possible without degrading the ADC dynamic performance. The LTM8074 with LC filter powers the 2 V analog and 2 V digital rails.

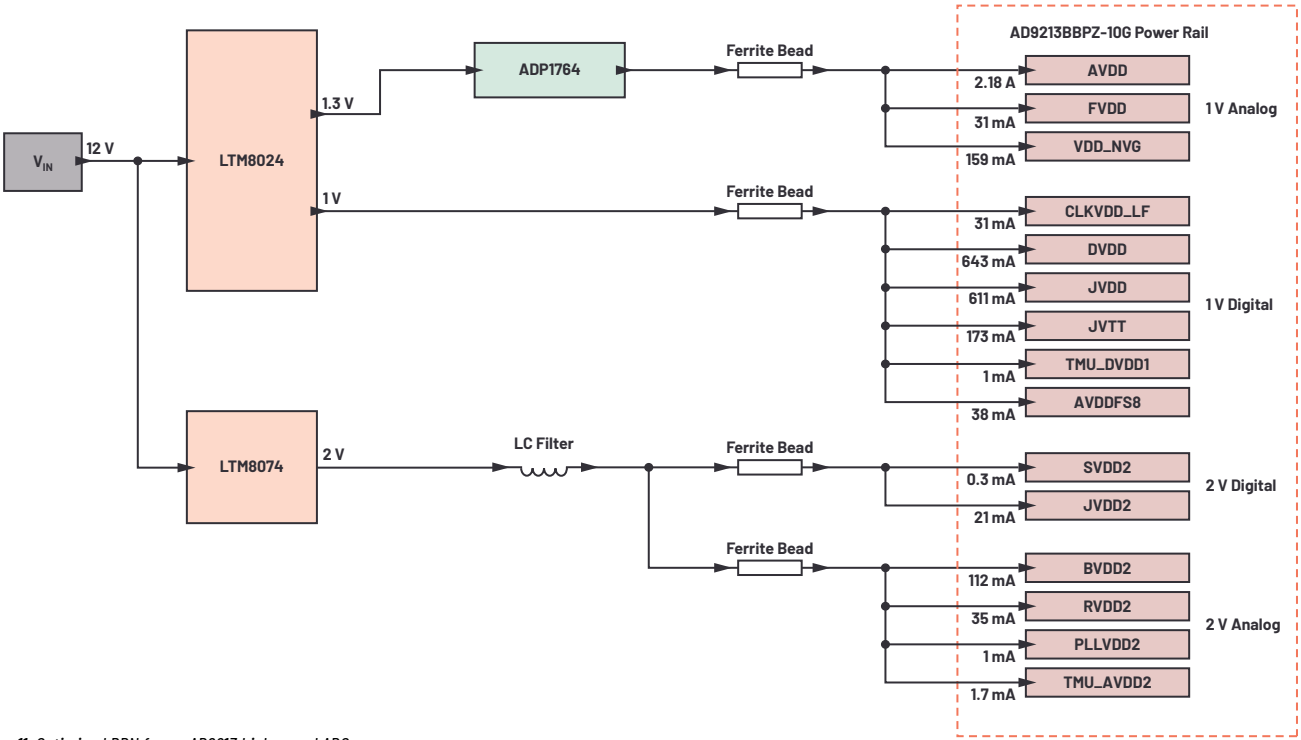
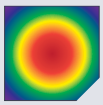


Figure 11. Optimized PDN for an AD9213 high speed ADC.

Table 3 compares the performance of the optimized PDN to the standard off-the-shelf PDN. As shown in Figure 7, the standard PDN uses a quad buck switcher with two LDO regulators. The component area reduction is 15.4% and the efficiency has increased to 73.5% (from 63.1%) with an overall power saving of 1.0 W.

Table 3. An Optimized PDN vs. a Standard PDN for the AD9213 High Speed ADC

	Standard PDN (Figure 7)	Optimized PDN (Figure 11)	Improvement of the Optimized PDN from the Standard PDN
Component Area	153.0 mm^2 	129.5 mm^2 	15.4%
Overall Efficiency	63.1% 	73.5% 	10.4%
Power Loss	2.5 W 	1.5 W 	1.0 W

To verify the performance of the optimized PDN, the AD9213 is evaluated in terms of SFDR and SNR, and by inspecting the FFT output spectrum of the sideband spurs around the carrier. The SNR and SFDR performance show results that are within data sheet specifications limits, as shown in Table 4. Figure 12 shows the FFT output spectrum of AD9213, and features a clean carrier frequency with no visible sideband spurs.

Table 4. AD9213 Dynamic Performance at 2.6 GHz Carrier Using the Optimized PDN of Figure 11

ADC Parameter	Evaluation Results	Data Sheet Specifications		
		Min	Typ	Max
SNR (dBFS)	52.6	50.1	52.3	–
SFDR (dBFS)	72.0	60.0	76.0	–

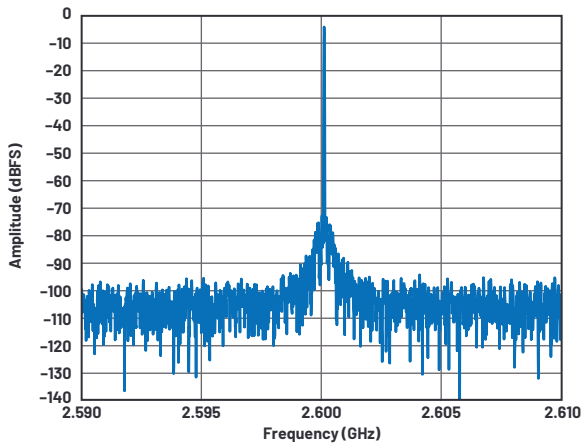


Figure 12. The FFT spectrum for the AD9213 (at 2.6 GHz, –1 dBFS carrier) using the optimized PDN of Figure 11.

Conclusion

Off-the-shelf evaluation boards for high performance data converters are set up with power distribution networks designed to meet the noise requirements of these signal processing ICs. Even with the careful considerations made in the design of the evaluation board, there is room for improvement of the power distribution networks. Here we examined two PDNs: one for a high speed DAC and one for a high speed ADC. We made improvements in space requirements, efficiency, and the especially important thermal performance over the standard PDNs. Further improvements could be made in certain parameters with alternate designs or currently unavailable devices. Stay tuned for further entries in this power system optimization series, including PDN optimization for RF transceivers.

References

[1] Patrick Errgy Pasaquian and Pablo Perez, Jr. "Optimizing Power Systems for the Signal Chain—Part 1: How Much Power Supply Noise Is Tolerable?" *Analog Dialogue*, Vol. 55, No. 1, March 2021.

Delos, Peter. "Power Supply Modulation Ratio Demystified: How Does PSMR Differ from PSRR?" Analog Devices, Inc., December 2018.

Delos, Peter and Jarrett Liner. "Improved DAC Phase Noise Measurements Enable Ultralow Phase Noise DDS Applications." *Analog Dialogue*, Vol. 51, No. 3, August 2017.

Eco, Jefferson and Aldrick Limjoco. "Ferrite Beads Demystified." *Analog Dialogue*, Vol. 50, No. 1, February 2016.

Jayamohan, Umesh. "High Speed ADC Power Supply Domains RAQ." *Analog Dialogue*, Vol. 52, No. 2, May 2018.

Jayamohan, Umesh. "Powering GSPS or RF Sampling ADCs: Switcher vs. LDO." Analog Devices, Inc., November 2015.

Limjoco, Aldrick, Patrick Errgy Pasaquian, and Jefferson Eco. "Silent Switcher µModule Regulators Quietly Power GSPS Sampling ADCs in Half the Space." Analog Devices, Inc., October 2018.

"The Essential Guide to Data Conversion." Analog Devices, Inc.

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RAQ Issue 188: Mitigation Strategies for Tricky FM Band Conducted EMI

Gengyao Li, Applications Engineer,
Dongwon Kwon, Staff Design Engineer, and
Keith Szolusha, Applications Director

Question:

How do I suppress tricky conducted FM band emissions from switching power supplies?

Answer:

Although EMI shields and ferrite clips are often a sought-after EMI solution, they can be expensive, bulky, and sometimes insufficient. FM band EMI noise can be reduced by understanding where it is coming from and employing circuit and PCB design techniques to suppress it at the source.

EMI performance of power supply networks is critical in noise-sensitive systems such as automotive circuits, especially when switch-mode power supplies (SMPS) are involved. Engineers can invest significant time to reduce conducted emissions (CE) and radiated emissions (RE). In particular, when measuring CE, the FM band (76 MHz to ~108 MHz) can be the most difficult region to achieve a passing result. Designers might need to spend significant time to do so. Why is the CE noise in the FM band so difficult to mitigate?

Low frequency (AM band) CE is dominated by differential-mode (DM) noise. High frequency (FM band) CE is dominated by common-mode (CM) noise.[1] Common-mode noise current is generated by nodes with changing voltages on the PCB.

The current leaks through stray capacitance to reference ground and back to input plus and minus cables (see Figure 1). Due to the complexity of stray capacitance around the PCB, it is not practical to simulate stray capacitance and estimate FM band conducted EMI. It is best to test the board in an EMI chamber.

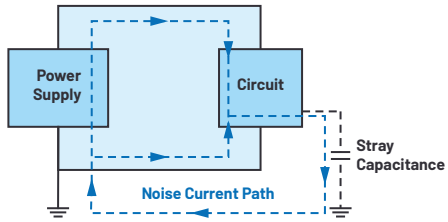

Figure 1. A conducted emission, common-mode noise current path.

There are proven methods in the lab that reduce FM band EMI effectively, including changing switching frequency, switching slew rate, switch node layout, hot loop layout, inductors, and even the location of input cables and load. The efficacy of each method could vary from board to board.

This article examines a number of simple, low cost ways to reduce FM band conducted EMI on a board—without using ferrite clips or shields. The results are verified by performing current probe CE tests, in a certified EMI chamber, on a board featuring the LT3922-1 in an automotive HUD LED driver, as shown in Figure 2.

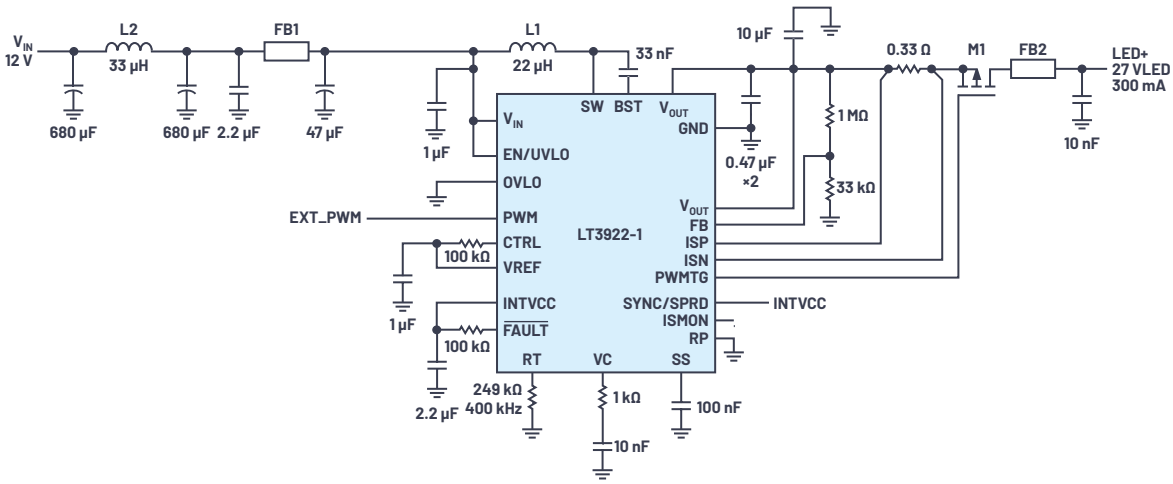

Figure 2. A simplified schematic of the LT3922-1 automotive HUD LED driver.

In this test, CE is measured with a current probe method in CISPR 25 EMI setup, as shown in Figure 3. CE can be tested by either the voltage probe method or current probe method, but the current probe method standard is generally considered the stricter of the two. Instead of measuring the voltage output from the LISNs, the current CE method utilizes a high bandwidth current probe to measure CM noise signals propagating through the power cord or harness, at distances of 50 mm and 750 mm from the DUT. Peak and average CE data is collected at each sweep and compared against published standards limits.

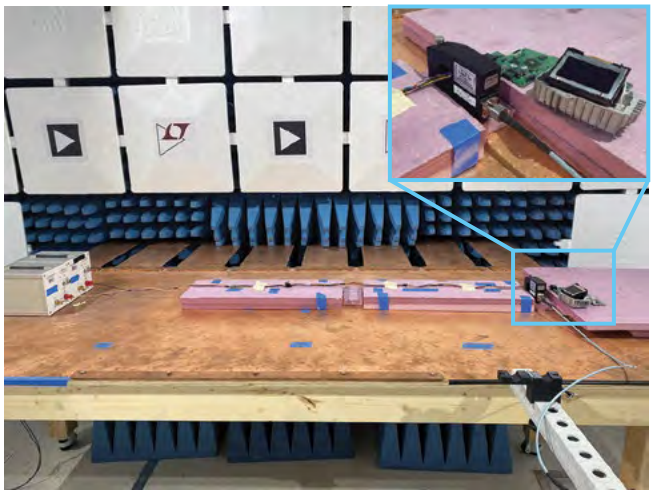

Figure 3. CISPR 25 current probe conducted emissions (CE) setup in EMI testing chamber (50 mm).

For the current probe method, FM band average CE limits described in CISPR 25 Class 5 are as low as –16 dBµA. Here, we present several effective approaches to improving results in the FM band under current probe testing for CE. Many of these methods can be applied to improve results in voltage method CE testing as well.

All the tests in this study feature SSFM enabled, unless otherwise specified. With SSFM, EMI spikes at the switching frequency and its harmonics are reduced.

Common-Mode Choke Suppresses FM Band EMI Noise

CM noise current, which is generated during switching, leaks into the reference ground through stray capacitance and comes back through input supply and return paths in the same direction. By increasing the common-mode impedance in the loop with a CM choke, unwanted CM noise can be suppressed.

Figure 4 shows 50 mm and 750 mm average current probe CE results, comparing the original circuit without the choke and with the choke installed before the LED driver circuit. The ambient noise floor is also shown for reference. FM band CE (76 MHz to ~108 MHz) was reduced by more than 8 dBµA.

Table 1. Specs Comparison of Inductors Tested

Part Number	3L UPIMFS0603-220M	Würth 74437346220	Coilcraft XEL5050-223
Magnetically Shielded	Yes	Yes	Yes
Pad Exposure	Exposed	Exposed	Hidden
Core Material	Metal dust	Iron powder	Composite

Inductors Make a Difference

Fast changing voltages and currents are applied to the main inductor, making it an electromagnetic antenna. Therefore, inductors can be a source for the FM band CE noise. EMI test results can be improved through a number of inductor-related methods. For instance, the assembly orientation of the inductor can make a difference.[2] Shielded inductors usually have lower emissions than unshielded ones, and some core materials limit H-field and E-field radiation more than others. For example, iron powder and metal alloy powder inductors have less E-field shielding effectiveness at frequencies above 1 MHz. MnZn and NiZn have better performance at higher switching frequencies.[2,3] Inductors with exposed pads perform worse than hidden pad inductors. Connecting the long lead of the inner coil winding to the high dV/dt (switch) node can increase E-field radiation dramatically.

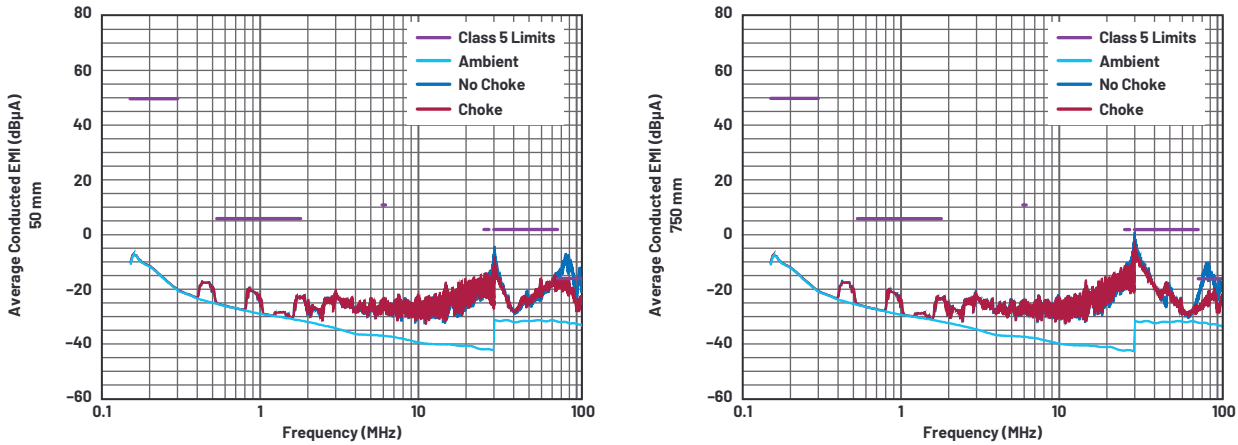

Figure 4. Current probe CE shows that emissions are lower in the FM band when a common-mode choke is used.

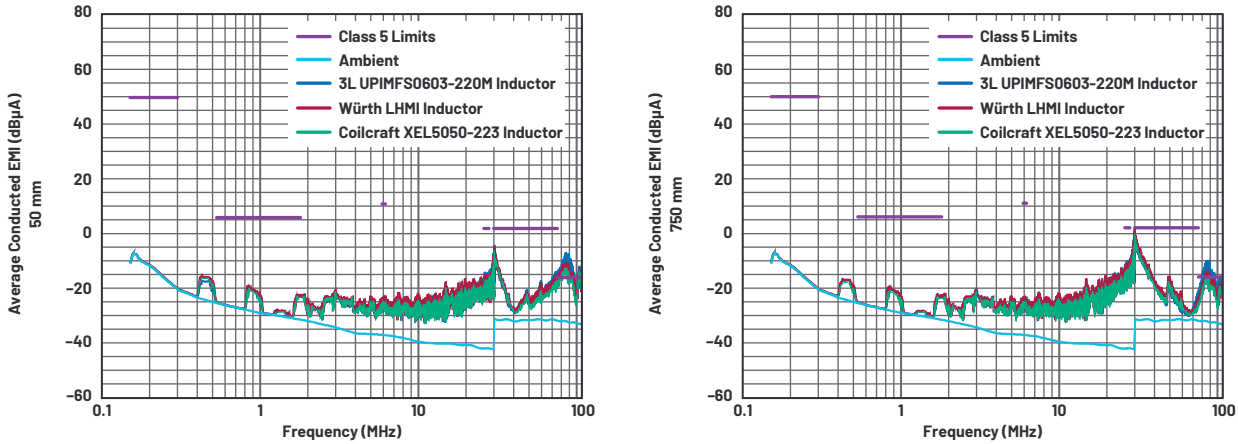

Figure 5. Current probe CE inductor comparison.

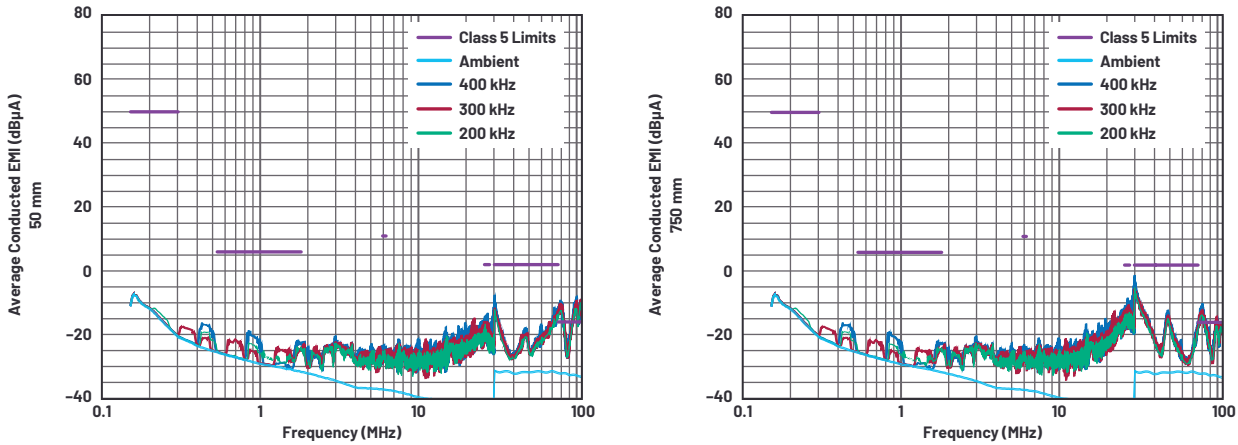

Figure 6. Current probe CE comparison of switching frequencies.

Three 22 µH shielded inductors were tested, as listed in Table 1. EMI was evaluated in the same circuit without a CM choke, and each inductor was assembled in its best performing orientation. The results are compared in Figure 5. In this study, the Coilcraft XEL inductor yields the best FM band performance, reducing FM band EMI by 5.1 dB compared to a 3L inductor.

Lower Switching Frequency (f_{SW}) Results in a Quieter FM Band

Reducing the switching frequency lowers the emissions energy at a given high frequency. In Figure 6, current probe CE is tested without a CM choke and compared at 200 kHz, 300 kHz, and 400 kHz switching frequencies. All the components other than RT were kept the same. The 200 kHz test shows the lowest EMI in the FM band, with emissions 3.2 dB lower than the 400 kHz case.

Shrink Your Noise Antenna by Reducing Switch Node Area

The high dV/dt switching node is a noise source, which generates capacitive coupling and increases CM EMI noise in CE. It also works as an antenna, which radiates electromagnetic noise into the space, affecting radiated EMI as well. Therefore, a minimized switching node area on the PCB layout improves EMI performance.

To test this on a PCB board, the switching node area was reduced by cutting off some copper and moving the inductor closer to the IC, as shown in Figure 7. EMI was tested before and after the copper removal, and the result is shown in Figure 8.

The 50 mm current probe CE test decreases 1 dB at 105 MHz, while the 750 mm test does not show obvious improvement. This result indicates the copper area is not the main contributing factor to FM band EMI for this application. Still, it is worth trying to reduce switch node area as much as possible to achieve a low EMI PCB layout, or during EMI mitigation.

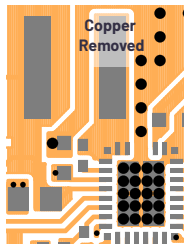

Figure 7. Switch node cutoff area.

Conclusion

A power supply's EMI performance depends foremost on the performance of the power supply IC, but even a high performance IC can only deliver low EMI with proper selection of components and effective PCB layout. In this article, we explored several methods of mitigating conducted emissions (CE) in the FM band using a board built around the LT3922-1 automotive HUD LED driver.

Applying a CM choke on positive and negative input lines increases impedance in the common-mode noise current loop. Different inductors with different core materials, core constructions, and coil constructions yield a range of EMI performance results. It is difficult to estimate which inductor is best by looking exclusively at specs, but comparisons can be made in the EMI lab.

The assembly orientation of inductors on the PCB is also important. Reducing switching frequency and reducing switching node copper area can both help reduce FM band CE. If the DUT is a switching regulator circuit using a controller part (external MOSFETs), FM band EMI can be further reduced by reducing switching slew rates and minimizing hot loop areas.

References

[1] Ling Jiang, Frank Wang, Keith Szolusha, and Kurk Mathews. "A Practical Method for Separating Common-Mode and Differential-Mode Emissions in Conducted Emissions Testing." *Analog Dialogue*, Vol. 55, No. 1, January 2021.

[2] Keith Szolusha and Gengyao Li. "Does the Assembly Orientation of an SMPS Inductor Affect Emissions?" *emiTime*, August 2020.

[3] Ranjith Bramanpalli. "ANP047: The Behavior of Electro-Magnetic Radiation of Power Inductors in Power Management." Würth Elektronik, March 2018.

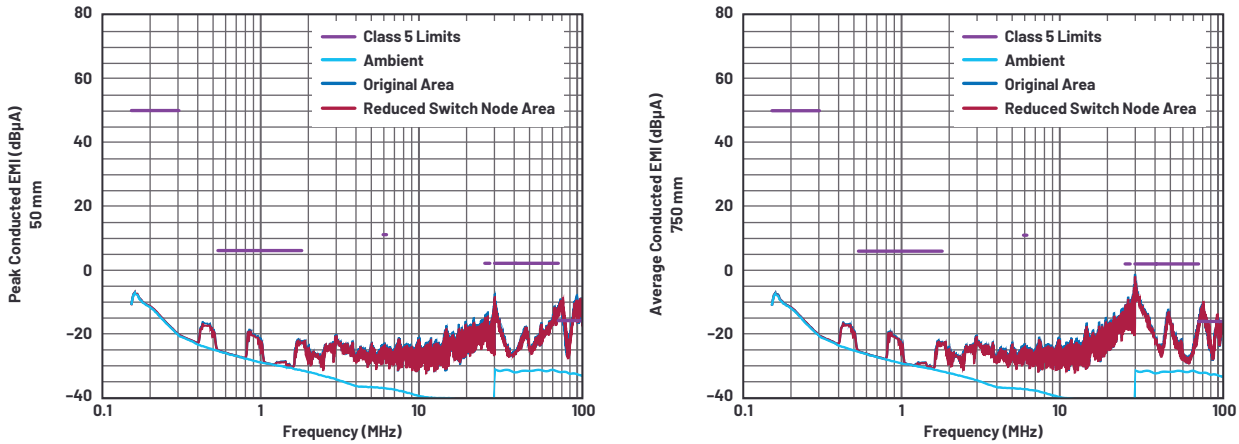

Figure 8. Current probe CE comparing switch node areas.

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How A²B Technology and Digital Microphones Enable Superior Performance in Emerging Automotive Applications

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Dietmar Ruwisch, Senior Audio Technologist at Analog Devices, Inc. and
Yu Du, Senior Principal Acoustic Engineer at Harman International Industries

Introduction

This article about Automotive Audio Bus® (A²B®) technology explains recent advances in digital microphone and connectivity technologies. These innovations are enabling swift adoption of game-changing applications for future generations of vehicle infotainment systems.

Markets and Application Landscape

Within the automotive in-cabin electronics segment, it's becoming increasingly clear that the universe of audio-, voice-, and acoustics-related applications is rapidly expanding as car manufacturers attempt to differentiate their vehicles from the competition. Additionally, as average consumers become more tech savvy, their expectations related to both the driving experience and level of personal interaction with the vehicle are expanding significantly. Home theater quality sound systems are commonplace across all vehicle price points and are now being augmented by sophisticated hands-free (HF) and in-car communications (ICC) systems. Additionally, active and road noise cancellation (ANC/RNC) systems, historically deployed in only the top-level premium vehicles, are now making their way into more mainstream, affordable segments. Looking to the future, audible or acoustics-based techniques will become a critical component in Level 4/Level 5 autonomous vehicle engine control units (ECUs) as they attempt to detect the presence of emergency vehicles.

The common thread binding all these legacy and emerging applications is the dependency on high performance acoustic sensing technology such as microphones and accelerometers. And since nearly all emerging applications require multiple acoustic sensors like microphones (or mic arrays) to achieve the best system-level performance, a simple cost-effective interconnect technology is required to ensure that total system costs are minimized. Historically, the lack of a microphone-optimized interconnect technology has been a significant pain point for car manufacturers, as each microphone would need to be directly connected to the processing unit using expensive and heavy shielded analog cable. These added costs—primarily in terms of actual wiring, but secondarily in terms of added weight and reduced fuel efficiency—have in many cases prevented the widespread adoption of these applications, or at least limited them to only the super-premium segments. Recent advances in both digital microphone and connectivity technologies are proving to be enablers to the swift adoption of game-changing applications in future generations of vehicle infotainment systems. A²B technology will make a difference.

Traditional Analog Microphone Implementations and Limitations

Using a handheld cell phone while operating a vehicle is banned in most countries, while Bluetooth®-enabled hands-free devices have become standard equipment in almost all vehicles. A wide array of hands-free solutions is available, from simple standalone units containing a loudspeaker and microphone to advanced solutions that are completely integrated within the vehicle infotainment system. Until recently, most hands-free systems were implemented in a very similar fashion. They were comprised of only one (rarely two) microphone(s), and the associated microphone technology was the 50-year-old electret condenser microphone (ECM) type. The voice quality of the transmitted audio was often unsatisfactory, especially in simple standalone units where the distance between the microphone and the talker's mouth could be rather large. Communication quality could be improved if the microphone were mounted as close to the mouth as possible (for example, in the headliner of the vehicle). However, in this case, both front seats require individual microphones if the driver and passenger are to be equally supported.

A typical automotive ECM is a device that combines the ECM capsule with a small amplifier circuit in a single housing. The amplifier delivers an analog signal with a voltage level that allows transport over wires of several meters in length, as required in typical automotive installations. Without amplification, the original ECM signal would be too low for such a wire length, as the signal-to-noise ratio (SNR) would degrade too far due to electromagnetic interferences on the wire. Even the amplified signal requires shielded wiring, which is typically a 2-wire cable with a bias (8 V) that supplies the microphone device. Given such wiring requirements, it is obvious that the number of ECM devices used in mainstream vehicles is limited due to weight and system cost constraints.

One of the few advantages of ECMs is their built-in acoustic directionality, which is usually trimmed to a super- or hypercardioid polar pattern (a MEMS mic can also be made unidirectional but typically requires more complex acoustic designs). Typically, 10 dB or more backward attenuation can be achieved, where "backward" means the direction toward the windshield, from which only noise (that is, no desired signals, such as the talker's voice) originates. Having a higher sensitivity in the incoming direction of the desired signal is very beneficial to increase the SNR. However, directional ECM capsules introduce unwanted side effects such as the high-pass characteristic where sensitivity decreases at lower frequencies. The 3 dB cutoff frequency of such a high-pass response is typically in the range of 300 Hz to 350 Hz. In the early days of HF technology, this high-pass behavior was an advantage because engine noise was present primarily at lower frequencies, so the engine sound was already attenuated through the microphone. However, since wideband, or HD, telephony is available, this high-pass behavior starts to become a problem. In a wideband call, the effective bandwidth is increased from 300 Hz to 3400 Hz, to 100 Hz to 7000 Hz. The built-in high-pass filter of the microphone makes it necessary to amplify signals between 100 Hz and 300 Hz in the postprocessing unit, which would not be required if the microphone were to deliver better audio bandwidth in the first place. Another disadvantage of ECM technology is the significant part-to-part variation in terms of sensitivity and frequency response. The relatively large manufacturing tolerance of ECMs may not present a problem for single microphone applications. However, if more than one microphone signal is deployed in a small-spaced microphone array application, then tight matching between microphones is essential for optimal array performance. In such a case, ECMs can hardly be used. Furthermore, from the physical size perspective, traditional ECM capsules are not generally suitable for small form factor microphone arrays.

Microphone arrays have experienced widespread applicability including in vehicles because they can provide similar, often superior, directionality performance when compared to traditional ECMs. Spatial information regarding sound impact directions can be extracted from the microphone signals using two or more suitable microphones grouped in an array. This class of algorithms is often referred to as beamforming (BF). The name beamforming is borrowed from an analogy with phased array antenna technology, where a radio "beam" is formed from the emission of an antenna array focused in a certain direction using a simple, purely linear filter and sum algorithm. Although there is no such beam in a microphone array, the term beamforming has also become very common in the field of microphone signal processing, where it covers a much wider range of both linear and nonlinear algorithms that enable higher performance and greater flexibility than the simple linear beamforming process.

In addition to the BF processing, a raw microphone signal almost always requires postprocessing because every HF microphone captures both desired voice signals and disturbances in the environment such as a car cabin. Wind, road, and engine noise deteriorate the SNR, and signals being played by loudspeakers—usually referred to as loudspeaker echoes—are additional sources of unwanted signals. In order to reduce such disturbances and improve voice quality, elaborate digital signal processing techniques are required, often referred to as acoustic echo cancelling and noise reduction (AEC/NR). AEC removes the loudspeaker sound from the microphone, which otherwise would be transmitted as an echo of the voice of the person speaking at the other end of the line. NR reduces constant driving noise while increasing the SNR of the transmitted signal. Although elaborate specifications (for example, ITU-T P.1100 and P.1110) that define many performance details of an HF system have been published by the International Telecommunication Union (ITU), the subjective impression of the communication quality in a call from an operating vehicle can be unsatisfactory if the AEC/NR processing is of substandard quality. Together with the previously mentioned BF algorithm, the bundle of AEC/NR/BF enables a wide array of new applications, all related with some level of digital audio signal processing. To support these applications, a new generation of microphone technology overcoming disadvantages of traditional ECMs is demanded.

Digital MEMS Microphones—Technical and Performance Advantages

Microelectromechanical systems (MEMS) technology is swiftly becoming the new industry standard for microphones, as it offers many advantages over traditional ECMs. First and foremost, MEMS enable a much smaller form factor sound sensor than existing ECM capsules. Additionally, integrating a MEMS sensor with an analog-to-digital converter (ADC) in a single IC results in a digital microphone that delivers signals ready for AEC/NR/BF processing.

Analog-ported MEMS microphones without an integrated ADC are also available, but they share many of the same disadvantages as analog ECMs and even require more complex amplifier circuitry than ECMs if operated on the traditional 2-wire analog interface. It is only with an all-digital interface technology that the interference and SNR problems inherent to analog wires can be significantly alleviated. Also, from a production perspective, MEMS are preferred because MEMS mics can be produced with a much tighter specification variance than ECM capsules, which is important for BF algorithms. Lastly, with MEMS IC microphones, the manufacturing process is greatly simplified because automated mounting techniques can be utilized, which reduces overall production costs. From an application perspective, the smaller form factor is the largest advantage, and, due to very small sound-entry portholes, MEMS mic arrays can be made virtually invisible. The porthole and the sound channel to the sensor require great care in terms of design and production quality. If the acoustic seal is not tight, noise from the inner structure may reach the sensor and leakage between two sensors may degrade the performance of the BF algorithm. Different from typical ECM capsules that can be designed and manufactured to be either omnidirectional or directional, MEMS microphone elements are almost always manufactured to be omnidirectional (that is, they have no intrinsic directionality of sound reception). As such, MEMS microphones are phase-true omnidirectional sound pressure sensors that deliver ideal signals for advanced BF algorithms, where attenuation directions and beam widths can be user-configurable via software.

As a rule, it is very important that all signal processing modules are grouped in an integrated algorithm suite. Processing latencies would needlessly increase, and overall system performance would be degraded if functional blocks were implemented in isolation from one another. For example, a BF algorithm should always be implemented together with the AEC and, optimally, from the same provider. If the BF algorithm introduces any nonlinear effects on the signal, the AEC will most certainly produce unsatisfactory results. Ideal results of digital signal processing can best be achieved by an integrated algorithm bundle that receives uncorrupted microphone signals.

Standard linear BF and ADI-proprietary algorithms are compared below in detail in order to fully understand the performance potential of advanced BF algorithms. The plots in Figure 1 show three different BF algorithms regarding polar characteristics and frequency response in both in-beam and off-beam directions. A standard linear supercardioid algorithm based on a 2-mic array serves as the benchmark (black curves). The benchmark curve shows the maximum attenuation in the typical zero-angle directions (that is, maximum off-beam attenuation) and a "rear-lobe" at 180°, where off-beam attenuation is lower. The resultant rear-lobe is a trade-off with beam width in a linear algorithm. A cardioid beam (not shown) has its maximum attenuation exactly at 180°; however, its receptive area is broader than a hyper- or supercardioid configuration. Beams with less significant rear-lobes and higher off-beam attenuation can be achieved with nonlinear algorithmic approaches, with the red curve showing an ADI-proprietary 2-mic algorithm of this class (microphone spacing: 20 mm).

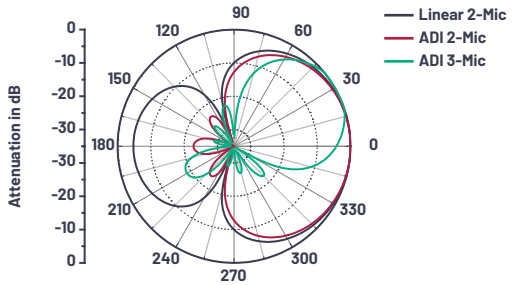

Figure 1. Polar attenuation characteristic of different BF algorithms.

With two omnidirectional microphones in an array, there is always a rotational symmetry of the beam shape. In other words, the attenuation at X° in the polar plot is the same as at 360° – X°. This assumes that the 0° to 180° line of the polar plot is equivalent to the imaginary line connecting the two microphones. The 3-dimensional beam shape can be imagined by rotating the 2D polar plot around this microphone axis. Asymmetric beam shapes without rotational symmetry or more narrow beams require at least three microphones arranged in a triangle. For example, in a typical overhead console installation, a 2-mic array can attenuate sound from the windshield. However, in such an orientation, a 2-mic array cannot distinguish driver from passenger. Rotating the array by 90° would make such driver/passenger distinction possible, but the noise from the windshield would not be distinguishable from sounds inside the cabin. Both windshield noise attenuation and driver/passenger differentiation are only possible using three or more omnidirectional microphones configured in an array. An exemplary polar characteristic of a respective ADI-proprietary 3-mic algorithm is given by the green curve in Figure 1 where the microphones are arranged in an equal-sided triangle with 20 mm spacing.

Polar plots are computed with band-limited white noise arriving at the microphone array from different angles. The audio bandwidth is limited to 100 Hz to 7000 Hz, which is the wideband (or HD-voice) bandwidth of state-of-the art cell phone networks. Figure 2 compares the frequency response curves of the different algorithm types. In the in-beam direction, the frequency response of all algorithms is, as expected, flat within the desired audio bandwidth. The off-beam frequency responses are computed for the off-beam half-space (90° through 270°), confirming high off-beam attenuation over a wide frequency range.

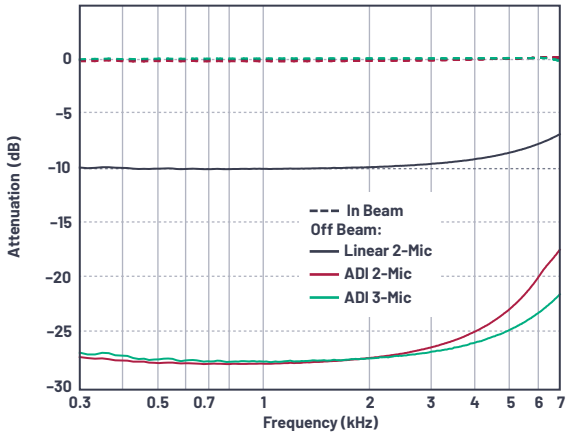

Figure 2. In-beam (dashed lines) and off-beam (bold lines) frequency responses of different BF algorithms.

The relationship between array microphone spacing and audio bandwidth vs. sample rate is worth further discussion. Wideband HD-voice uses a sample rate of 16 kHz, which is a good choice for speech transmission. There is a huge difference in voice quality and speech intelligibility between the current 16 kHz wideband sample rate and 8 kHz, which was used in earlier generations of narrow-band systems. Driven by speech recognition providers, there is growing demand for even higher sample rates, such as 24 kHz or 32 kHz. And specifications can be found where the sample rate of the voice-band application should be as high as 48 kHz, which is typically the primary system audio sample rate. The underlying motivation is to avoid any internal sample rate conversion. However, the additional computational resources required to support these high sample rates cannot be justified by a tangible audible benefit, so 16 kHz or 24 kHz are now widely accepted as the recommended sample rates for most voice-band applications.

High sample rates are problematic for BF applications because spatial aliasing occurs at frequencies equaling the speed of sound divided by twice the microphone spacing. Spatial aliasing is undesirable because BF is not possible at such aliasing frequencies. Spatial aliasing can be avoided in a wideband system (16 kHz sample rate) if the microphone spacing is limited to 21 mm or less. Higher sample rates require smaller spacing to avoid spatial aliasing. However, overly small mic spacing is also undesirable because microphone tolerances and especially intrinsic (non-acoustic) noise of the microphone sensors can become an issue. Signal differences between the microphones of an array get marginal if the spacing is small and disturbances such as intrinsic noise and sensitivity deviations between the microphones can overwhelm the signal difference between microphones. In practice, microphone spacing should not be less than 10 mm.

A²B Technology Overview

A²B technology has been specifically developed to simplify the connectivity challenge in emerging automotive microphone and sensor-intensive applications. From an implementation standpoint, A²B is a single-main, multiple subnode (up to 10), line topology. The third generation of A²B transceivers that is currently in full production consists of five family members—all offered in automotive, industrial, and consumer temperature ranges. The full-featured AD2428W, together with four feature-reduced, lower cost derivatives—AD2429W, AD2427W, AD2426W, and AD2420W—comprise ADI's latest family of pin-compatible, enhanced A²B transceivers.

The AD2427W and AD2426W offer reduced (subnode only) functionality and are primarily targeted for microphone connectivity applications such as hands-free, ANC/RNC, or ICC. The AD2429W and AD2420W are entry-level A²B derivatives that offer significant cost advantages relative to their full-featured counterparts and are particularly well-suited for cost-sensitive applications such as automotive eCall and multi-element microphone arrays. Table 1 shows a feature comparison among the third-generation A²B transceivers.

Table 1. A²B Transceiver Feature Comparison

Feature	AD2420/ AD2420W	AD2426/ AD2426W	AD2427/ AD2427W	AD2428/ AD2428W	AD2429/ AD2429W
Main Capable	No	No	No	Yes	Yes
Number of Discoverable Subnodes	—	—	—	Up to 10	Up to 2
Functional TRX Blocks	A only	A only	A + B	A + B	B only
I²S/TDM Support	No	No	No	Yes	Yes
PDM Microphone Inputs	2 mics	4 mics	4 mics	4 mics	4 mics
Max Node to Node Cable Length	5 m	15 m	15 m	15 m	5 m

The AD242x series supports daisy-chaining a single main plus up to 10 subnodes over a total bus distance of 40 m with up to 15 m supported between individual nodes. A²B's daisy-chain, line topology is an important advantage over existing ring topologies as it relates to overall system integrity and robustness. If one connection of the A²B daisy chain is compromised, the entire network does not collapse. Only those nodes downstream from the faulty connection are impacted by the failure. And A²B's embedded diagnostics can isolate the source of the failure, signaling an interrupt to initiate corrective action.

A²B's main/subnode line topology is inherently efficient when compared to existing digital bus architectures. After a simple bus discovery process, zero additional processor intervention is required to manage normal bus operation. As an added benefit of A²B's unique architecture, system latency is completely deterministic (a 2-bus cycle delay, which is less than 50 µs) irrespective of the audio node's position on the A²B bus. This feature is extremely important for speech and audio applications such as ANC/RNC and ICC, where audio samples from multiple remote sensors must be processed in a time-aligned fashion.

All A²B transceivers deliver audio, control, clock, and power over a single, 2-wire, UTP cable. This reduces overall system cost for a variety of reasons.

- The number of physical wires is reduced relative to traditional implementations.
- The actual wires themselves can be lower cost, lower weight UTP as opposed to more expensive shielded cables.
- Most importantly, for particular use cases, A²B technology offers a bus power capability that delivers up to 300 mA of current to audio nodes on the A²B daisy chain. This bus power capability eliminates the need for local power supplies at the audio ECU—further reducing total system costs.

The total 50 Mbps bus bandwidth delivered by A²B technology supports up to 32 upstream and up to 32 downstream audio channels using standard audio sample rates (44.1 kHz, 48 kHz, etc.) and channel widths (16-, 24-bit). This provides significant flexibility and connectivity to a wide range of audio I/O devices. Maintaining a completely digital audio signal chain between audio ECUs ensures that the highest quality audio is preserved without introducing the potential for audio degradation via ADC/DAC conversion.

System-level diagnostics are an essential component of A²B technology. All A²B nodes have the capability to identify a variety of fault conditions including opens, wires shorted together, reversed wires, or wires shorted to power or ground. This capability is important from a system integrity standpoint because, in the case of opens, wire shorts, or reversed wire faults, A²B nodes are still fully functional upstream of the fault. The diagnostic capability also provides for the efficient isolation of system-level failures, which is critically important from the dealer/installer standpoint.

The recently announced, fourth generation of A²B transceivers, AD243x, builds upon the existing technology foundation by increasing key functional parameters (node count increased to 17, bus power increased to 50 W) while adding an additional SPI-based control channel (10 Mbps) that provides an efficient software over-the-air (SOTA) capability for remote programming of intelligent A²B-connected nodes. The new features provided by the AD243x family make it well-suited for LED-fitted microphone nodes in super-premium microphone architectures.

Applications of A²B Microphones and Sensors in the Automotive Industry

From a single voice microphone to a multi-element BF mic array for HF communication, from ANC to RNC, from ICC to siren sound detection, microphones have found more and more applications in the automotive industry. In accordance with the technology and market trend, almost every single new vehicle that hits the road today is equipped with at least one microphone module for HF communication. Premium and luxury cars may come with six or more microphone modules that are necessary for realizing the full potential of BF, AEC, ANC, RNC, ICC, and so on, where digital MEMS microphones present clear advantages.

The growing microphone count presents one significant challenge to vehicle infotainment engineers—how to simplify the connecting harnesses and minimize their weight. This is not a trivial task for traditional analog systems. At a minimum, an analog microphone requires a pair of two shielded wires (ground and signal/power), pins, and connector cavities for interconnection. The amount of wires is always twice the number of microphone modules in the system. Meanwhile, the total weight of the harness could increase even more rapidly depending on the wire length that is needed for connecting each microphone module. One simple way to mitigate this problem is to reduce the number of microphones used in the system by sharing a microphone signal among multiple applications. For example, the same microphone signal could be used in HF communications and as an error signal in the ANC system. However, different applications may require different microphone characteristics. In the previously mentioned example, an HF microphone signal often prefers to have a rising frequency response shape (that is, sensitivity decreases with decreasing frequency) to remove the low frequency noise content inside the cabin. This is a helpful and very effective technique to improve the speech intelligibility delivered by a voice microphone. On the contrary, an ANC microphone requires sufficient sensitivity level at low frequencies as the main purpose of the ANC algorithm is to reduce the low frequency noise. Thus, to share the same microphone in two applications in an analog system, the signal coming from the microphone needs to be fed into different circuits for proper frequency filtering. In this case, one or multiple ground loops may form, which can cause significant noise issues.

As a digital bus with daisy-chaining capability, A²B technology together with the digital MEMS microphone provide a well-suited solution for interconnecting and/or sharing multiple microphone signals demanded by audio, voice, noise cancelling, and other acoustic applications that are rapidly expanding in vehicles. Consider an imaginary while exemplary case where a car application calls for an HF microphone module, an ANC microphone module, and a simple array microphone module consisting of two microphone elements for BF, and all three modules are integrated around the overhead console area. Figures 3a and 3b show how

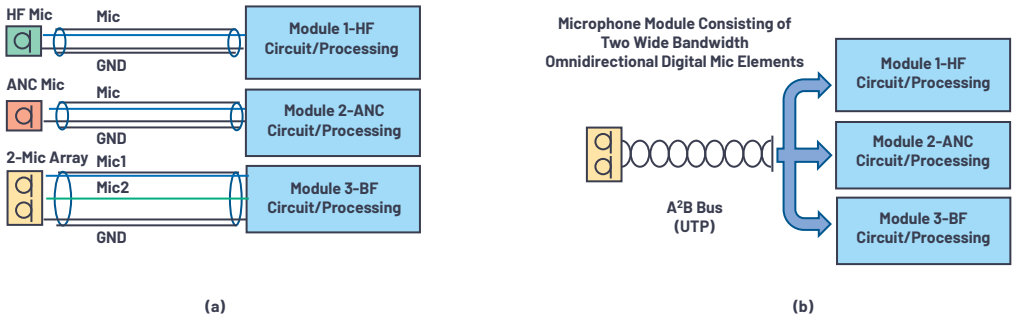

Figure 3. (a) Analog system design with analog mic elements (shielded wires). (b) Digital system design with digital mic elements (A²B technology and UTP wires).

such a design may be realized with the traditional analog and the digital A²B systems, respectively.

Since the analog system cannot easily accommodate microphone sharing, each application block (HF, ANC, and BF) requires dedicated microphone(s) and separate harnesses for connecting to the corresponding functional circuit(s). This leads to four separate microphone elements and three sets of harnesses (a total of seven wires plus shielding). In contrast, because sharing signals is easily supported by the digital A²B system, the number of microphone elements can be potentially reduced from four to two. In this specific example, a single microphone module consisting of two wide bandwidth omnidirectional microphone elements can be used to provide two channels of acoustic signals that cover the needs of all application blocks. Once these two channels of signals reach the center processing unit (for example, the head unit or amplifier) through a simple UTP wire, they can then be shared and digitally processed to support HF, ANC, and BF applications.

Although the example illustrated in Figure 3 may not represent a real situation, it clearly demonstrates the benefits of the A²B technology over the traditional analog technology. A digital audio bus system like the A²B technology addresses the challenge of automobile manufacturers to offer new audio and acoustic-related concepts that enhance user experience and allows these concepts to be brought to the market for faster implementation.

Indeed, many applications that are either new to the automotive market or previously difficult to implement have been made possible by the commercialization of A²B technology. For example, as a leading automotive audio solution provider, Harman International has developed a family of digital microphone and sensor modules that takes advantage of the A²B system to enable various automotive applications. Figure 4 shows some common automotive A²B microphones and sensors and how they can be used on a vehicle. These sensors include single A²B microphones and multi-element microphone arrays for ANC and voice communication, A²B accelerometers for RNC, externally mounted bumper A²B microphones, and rooftop A²B microphone arrays for emergency siren detection and acoustic environment monitoring. Enabled by these A²B microphones and accelerometers, more and more application solutions requiring multiple sensor inputs are currently under development to further enhance the user experience in the automotive industry.

Summary

Vehicle architectures of the future will become increasingly more dependent on high performance acoustic sensing technology such as microphones and accelerometers. A completely digital approach including sensor, interconnect, and processor provides significant performance and system cost benefits. Analog Devices and Harman International are partnering to deliver cost-effective solutions that create value and differentiation for their end customers.

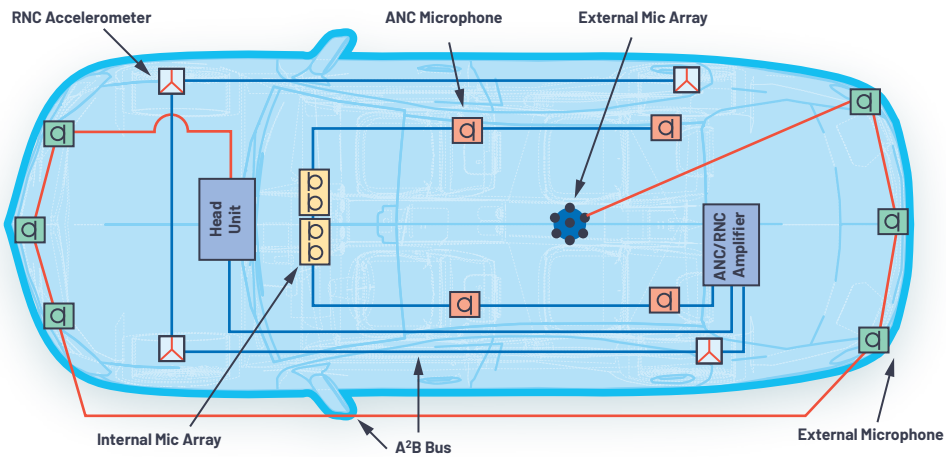

Figure 4. Common A²B microphones and sensors.

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CTSD Precision ADCs—Part 4: Ease of ADC Input and Reference Drive Simplify Signal Chain Design

Abhilasha Kawle, Analog Design Manager and
Roberto Maurino, Design Engineer

In this article, we highlight one of the most important architectural traits of new continuous-time sigma-delta (CTSD) precision ADCs: the easy to drive resistive input and reference. The key to achieving optimal signal chain performance is ensuring that the input source or the reference itself is not corrupted when interfaced with an ADC. With traditional ADCs, complex signal condition circuitry design, termed as front-end design, is required for the seamless interface of input and reference to the ADC. The unique architectural properties of CTSD ADCs enable simplified and innovative ways of interfacing this ADC to the input and reference. To begin, let's have a quick recap of traditional ADC front-end designs.

Front-End Design for Traditional ADCs

In this article, we will use the terms "sensor" or "input signal" interchangeably to represent any kind of voltage input to the ADC signal chain. The input signal for the ADC signal chain could be a sensor, a signal from some source, or the feedback of a control loop. It is well known that in traditional discrete-time sigma-delta (DTSD) ADCs and successive approximation register (SAR) ADCs, the sampling network at the input and reference is a switched capacitor load. When the switch turns ON, the capacitor is charged to the input, and when it turns OFF, the capacitor holds the sampled value. At every sampling clock edge when the switch reconnects the capacitor to the input, a finite current termed kickback current is required to charge or discharge the capacitor to the new sampled value. The profile of the current is shown in Figure 1a. Most sensors and reference ICs fall short of driving such magnitudes of kickback currents and if directly interfaced to the ADC, there is a high probability of the input signal or reference getting corrupted. One of the known solutions to avoid this corruption is to use a driving buffer amplifier to isolate the input sensor and the reference from the ADC. The driver amplifier should have the capability to absorb these kickback currents as shown in Figure 1b. This leads to the requirement of a high slew rate and a high bandwidth amplifier to support the required input charging/discharging currents and settle the kickbacks within one sampling time period. These stringent requirements limit the choice of buffer amplifiers that can be used on input and reference paths for the traditional ADCs.

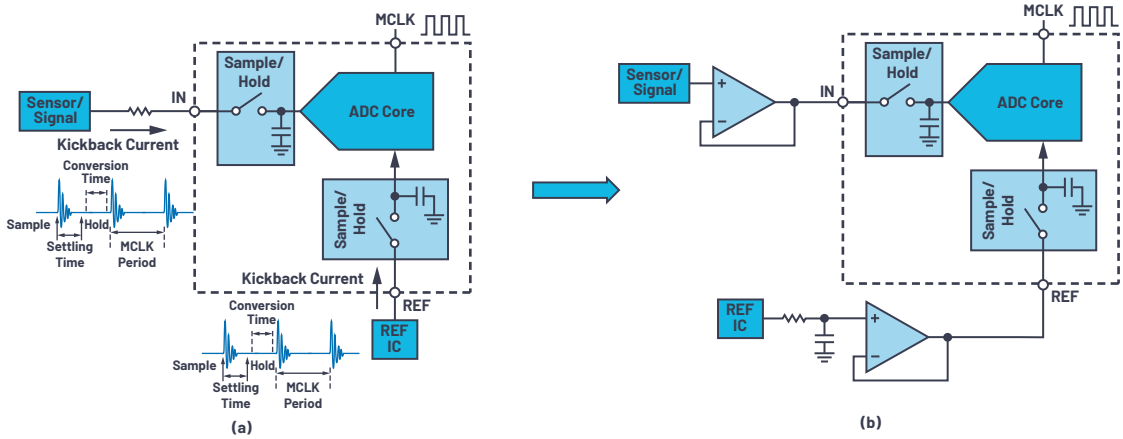

Figure 1. (a) Kickback current on the input and reference of a traditional ADC, and (b) the isolation of the kickback currents by the buffers on an input and reference.

On the other hand, a low-pass antialiasing filter is required on the input to ensure high frequency noise and interferers are heavily attenuated so that when they fold back due to sampling into the frequency band of interest, the performance is not degraded. The challenge for incumbent ADC signal chain designers is to fine-tune the opposing requirements of alias rejection and output settling. The front-end design with driver and antialiasing filter for a DTSD ADC is shown in Figure 2.

The input path consists of an instrumentation amplifier (in-amp) that interfaces the sensor to a fully differential amplifier (FDA), which finally drives the ADC. The in-amp isolates the input sensor environment from the ADC circuit. For example, the common-mode (CM) signal of the sensor can be very high, up to 10s of volts. But most FDAs and ADCs don't support this high input common-mode voltage. A general in-amp has the capability to support wide input common mode while providing an output common mode suitable for the FDA and ADC. Another advantage of an in-amp is that it has high input impedance. This means that if the sensor cannot drive the input resistor of the FDA directly, then the sensor can be interfaced with an FDA using an in-amp. The FDA itself would require a high bandwidth and slew rate for faster output settling. An active antialiasing filter (AAF) required for the interferer's immunity is built around the FDA.

The drivers of the input or the reference have conflicting requirements: on the one hand, high bandwidth is desired for settling, but on the other, low bandwidth is required to filter noise and interferers. On the reference path, the front-end design for the DTSD ADC signal chain is shown in Figure 2, which has a reference IC connected to a buffer that drives the reference load of the ADC. It also includes a noise filter that cuts off the noise of the reference IC and buffer beyond a certain frequency. The design requirements of this filter are discussed in a later section. The reference buffer has high bandwidth and slew rate requirements for faster settling of the sampling event disturbances.

Part 1 of this series demonstrated that a new signal chain using a precision CTSD ADC could be 68% smaller than the complex signal chains of traditional ADCs. This size reduction decreases the BOM, and the simplicity helps signal chain designers achieve faster time to market.

CTSD ADC Advantage: Resistive Input and Reference

In Part 2, the CTSD ADC architecture was explained to signal chain designers with an unconventional approach to inverting closed-loop amplifiers. As noted in Part 2, a CTSD ADC can be envisioned as a sigma-delta ADC with a resistive input and reference load. The input and reference structure are a simple resistive load, which means there are no high bandwidth or high slew rate drive requirements. Part 3 demonstrated the unique advantages of a CTSD that offers interference immunity due to its inherent alias rejection. In a traditional signal chain design, the external alias rejection filter needed to attenuate the interferers is an added challenge, while CTSD ADCs have no need for an external AAF. Due to the inherent alias rejection property of CTSD ADCs, the signal transfer function of the modulator loop equates to an antialiasing filter that attenuates the high frequency interferers. Because of the resistive input and inherent AAF, the input network is simplified, and the sensor can be directly connected to the ADC. In cases where sensors may not have the capability to drive such a resistive load, an in-amp could be used to interface the sensor to the ADC. Similarly, on the reference side, due to the resistive load, the reference buffer is eliminated in the CTSD ADC signal chain. A simplified schematic with an in-amp is shown in Figure 3b.

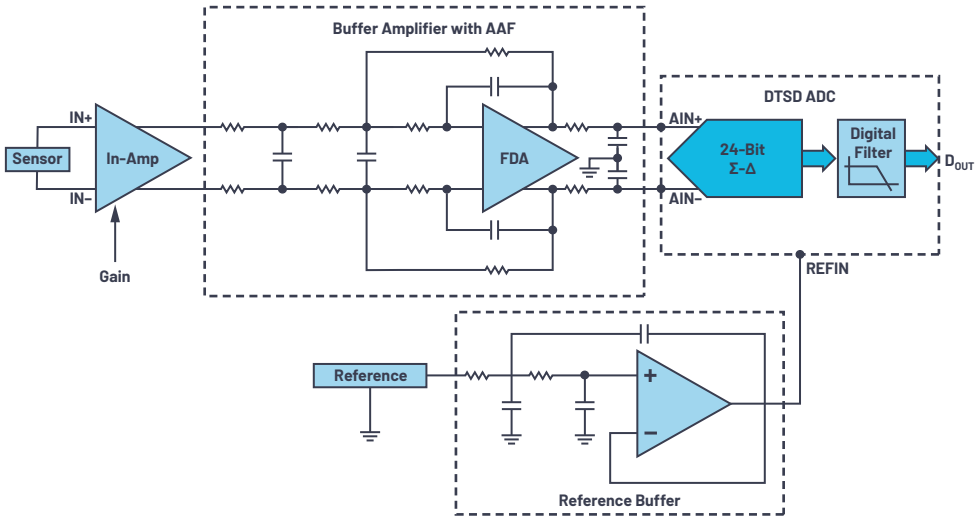

Figure 2. The front-end design of a discrete-time sigma-delta ADC.

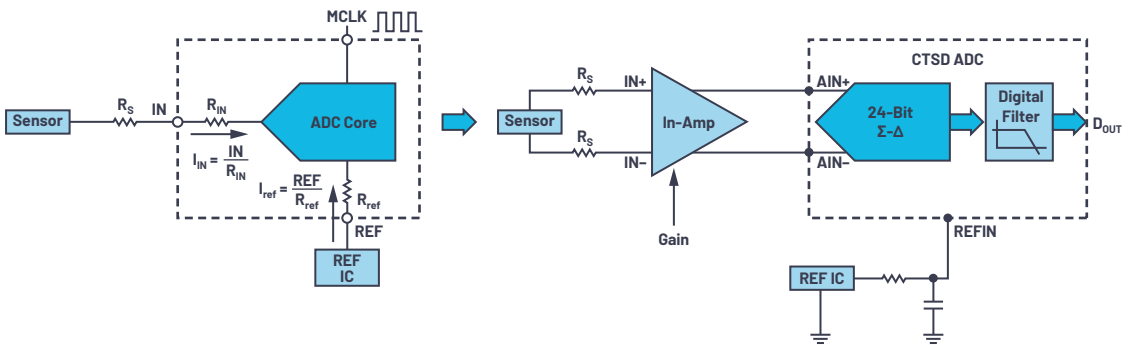

Figure 3. (a) A CTSD architecture offers resistive input and reference load, and (b) a direct in-amp with the reference driving a CTSD ADC.

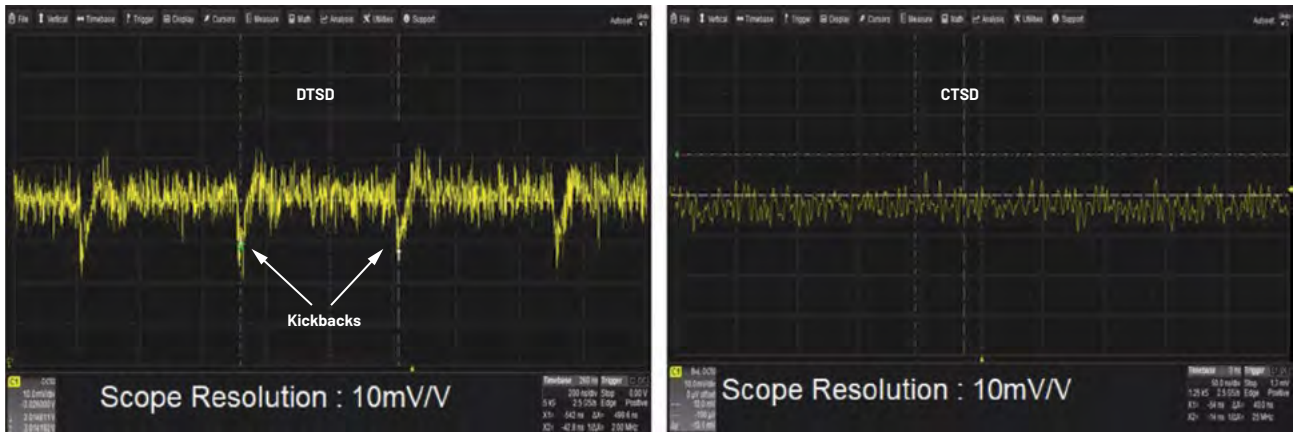

Figure 4. (a) Kickbacks in input current for a DTSD ADC, and (b) a continuous input current profile for a CTSD ADC.

Figure 4 shows further support for how CTSD ADCs help simplify input front-end design. For the DTSD ADC, the discontinuities in input current because of kickbacks when the input sampling switch changes state are noticeably seen. With the CTSD ADC, the input current is observed to be continuous, which maintains signal continuity.

The Simplified Input Drive Design

We have established that the input drive of the CTSD ADC is resistive. This section will address the value of the input impedance R_{IN} in planning for the input drive of the ADC. R_{IN} is a function of the noise performance specified for the ADC. For example, in the AD4134, which is a precision CTSD ADC with a dynamic range of 108 dB with 4 V reference, the input impedance is 6 kΩ differential. This indicates that when a full-scale 8 V p-p differential input signal is applied to the ADC, the peak current requirement is 1.3 mA p-p. If the sensor can support the input current V_{IN}/R_{IN}, then it can be directly interfaced to the ADC. The scenarios where a simple amplifier would be required to drive this resistive load are:

1) When the sensor doesn't have the drive capability to provide the peak current of V_{IN}/R_{IN}.
2) Signal chain design dictates that gain or attenuation is required for the sensor output.
3) Isolating input sensor environment from the ADC circuit.
4) The sensor has a large output impedance.
5) The sensor is far from the ADC and the track routing could add significant resistance to the input.

In scenario 4 and 5, there would be a voltage drop across the extra external resistor R_s, which indicates a signal loss at the ADC input. This leads to gain errors for the signal chain and drift of errors with temperature, which can lead to performance degradation. The temperature gain drift is caused by the different temperature coefficients of the external resistance and internal resistance. This problem can be solved with a simple amplifier to isolate the extra external resistance. Because the driving load for this amplifier is resistive, the selection criteria of this amplifier are:

- Input impedance: To avoid signal attenuation or loss, the impedance of the sensor should be matched with the amplifier input impedance.
- Output impedance: The output impedance should be sufficient to drive the resistive input load of the ADC.
- Output type: As a general signal chain design guideline, a differential signaling strategy is recommended for best signal chain performance. A differential output type amplifier or a design technique for single-ended to differential output is best suited for this task. Also, for the best performance, it is preferable to set the common mode of this differential signal to $V_{REF}/2$.
- Programmable gain: The input signal is generally gained or attenuated to map it to the full-scale range of the ADC. This is because the maximum performance can be obtained from an ADC signal chain when the full input range of its ADC is used.

Based on the application, this amplifier could be an in-amp or an FDA or combination of two single-ended op amps forming a differential output amplifier. With no rigid requirements of high slew rate or high bandwidth, a wide range of selection from ADI's amplifier portfolio is available to drive this CTSD ADC based on application requirements. Also, amplifier performance parameters are generally specified with a resistive load, which makes the selection more straightforward.

As an example, for the AD4134, one option for a performance-compatible in-amp with programmable gain options and fully differential outputs is the LTC6373. This in-amp provides high impedance to the input source and can easily drive the differential 6 kΩ impedance with noise and linearity performance on par with the ADC. With its wide range of input common-mode support and programmable gain options, any sensors or input signals with a wide range of signal magnitude can be interfaced with the ADC. An example of input front-end design with this direct in-amp drive is shown in Figure 4.

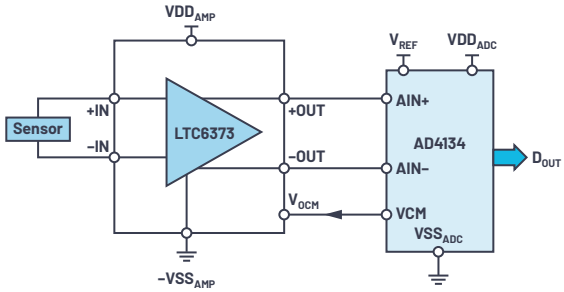

Figure 5. Input front-end design with CTSD ADC directly interfacing to in-amp.

Another example is a low voltage simple front-end design using a fully differential driver amplifier like the LTC6363-0.5/LTC6363-1/LTC6363-2, based on the gain or attenuation required, as shown in Figure 6. The scenario when FDAs could be used is when the sensor has the capability to drive the resistive load of the FDA but is single-ended type or has a common-mode that is not supported by the ADC or requires small gain/attenuation in the signal chain.

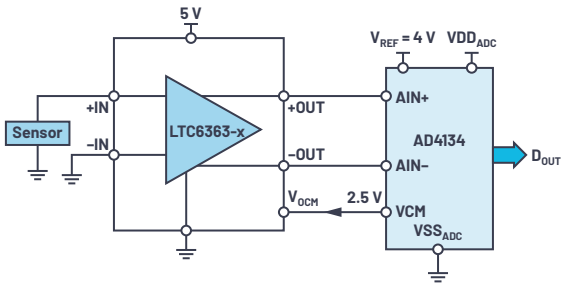

Figure 6. An input front-end design with a CTSD ADC directly interfacing to fully differential amplifier.

Another example includes a low BOM option for single-ended input conversion to a fully differential signal at the ADC using two single-ended op amps, as shown in Figure 7.

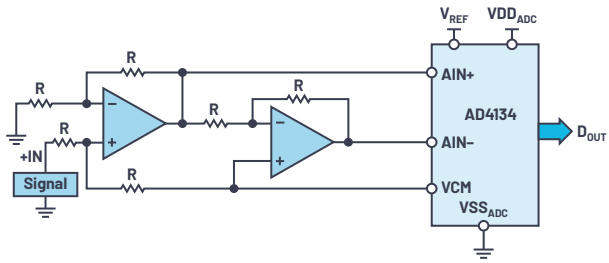

Figure 7. An input front-end design with a CTSD ADC with two single-ended amplifiers.

There are many other examples, like using a combination of a single-ended in-amp and single-ended op amp to build a differential output front end for a very high input CM or low drive strength single-ended type sensor. Any such combination can be selected based on performance, area, and BOM requirements to better suit the application.

A list of other amplifiers that are compatible with AD4134 are:

- Operational amplifiers: ADA4625-2, ADA4610-2, AD8605, and ADA4075-2.
- Fully differential amplifiers: ADA4940-2, LTC6363, and ADA4945-1.
- Instrumentation amplifier: AD8421.

ADI's amplifier selection guide can be used to select the best amplifier suited for an application. For example, for high linearity applications like audio test equipment, the ADA4945-1 is recommended. For photodiode applications where the most important consideration is very high input impedance, a transimpedance amplifier (TIA) like ADA4610-2 can be used.

With the input front end dramatically simplified with a CTSD ADC, let's have a look at the similar simplification of the reference drive.

The Simplified Reference Design

The ADC output is a representation of its input and reference, as given by Equation 1.

$$D_{OUT} = V_{IN} \times \frac{2^N}{VREF_{ADC}} \quad (1)$$

Where V_{IN} = input voltage level, $VREF_{ADC}$ = reference of the ADC, N = number of bits, D_{OUT} = ADC digital output.

Equation 1 indicates that, for the best ADC performance, a clean, uncorrupted reference is important. The three major performance metrics of the ADC signal chain that are affected by an error in the reference are:

- **Signal-to-noise ratio (SNR):** The major noise contributors to SNR are the input path, the ADC itself, and the reference. For a target total noise at the output of the ADC, accounting for the other noise contributors, the budget for the reference noise is generally ⅓ or ¼ of standalone ADC output noise. The reference or reference buffers typically have higher noise than the ADC. If we look at any data sheet for a reference or reference buffer IC, spectral noise density, or $Noise_{density}$, is one of the specifications. If we revisit noise calculations basics, the total noise at the output of the reference or reference buffer is then given by

  $$Total\ Reference\ Noise = Noise_{density} \times \sqrt{(Noise\ Bandwidth)} \quad (2)$$

  We cannot control the $Noise_{density}$ as it is fixed for the chosen reference or buffer. The only controllable parameter is the noise bandwidth (NBW). To target low reference noise, we reduce the noise bandwidth of reference or reference buffer. This is generally done by connecting a first-order low-pass RC filter to the ADC, as shown in Figure 8. For a first-order RC filter, the NBW is given by

  $$NBW = \frac{1}{2\pi RC} \times \frac{\pi}{2} = \frac{1}{4 \times RC} \quad (3)$$

  The ADC reference current, I_{ADC}, flowing through the filter resistor R causes a voltage drop, which changes the actual reference value at the ADC. Therefore, it is recommended to choose a small value of R and a large value of C to meet the NBW requirements for low reference noise.

- **Gain error:** As evident from Equation 1, $VREF_{ADC}$ determines the slope of the output to input transfer function just like in a straight equation such as y = mx. This slope is also termed as the gain of the ADC. Thus, if the reference changes, the gain of the ADC also changes.
- **Linearity:** For traditional DTSD ADCs and SAR ADCs, the reference current and the accompanying kickbacks are dependent on the input signal. Therefore, if the reference does not settle completely before the next sampling clock edge, the error seen on the reference will be input dependent and cause nonlinearity. Mathematically, the $VREF_{ADC}$ is then represented as

  $$VREF_{ADC} = (VREF - I_{ADC} \times R) = VREF + aV_{IN} + bV_{IN}^2 + cV_{IN}^3 \quad (4)$$

  Referring to Equation 1, the ADC output D_{OUT} will have various higher order dependencies based on the input of the ADC, and this dependency causes harmonics and integral nonlinearity. Hence, for traditional ADCs there is a hard requirement on the high slew rate and bandwidth of the reference buffer to settle the reference output within the sampling time period.

If we carefully analyze the SNR and linearity, we see that the reference or reference buffer has quite conflicting requirements to satisfy. There is a low bandwidth requirement for noise and a high bandwidth requirement for faster settling. Tuning the fine balance between the two requirements has been an age-old challenge for signal chain designers. Some of the latest DTSD ADCs and SAR ADCs have the reference buffer incorporated on-chip to ease one step in signal chain design, but these solutions require additional power or come with certain performance penalties. Because CTSD ADCs don't need a fast settling buffer and have a resistive input to remove the need for a fast settling driver, they're able to avoid these performance problems.

The CTSD ADC addresses reference driver challenges with the following properties and design improvements:

- With the resistive load on reference, there is no settling requirement at every sampling clock edge. This allows designers to directly connect the reference IC to the ADC without requiring a dedicated reference buffer.
- Patented design techniques make the reference current independent of the input and force the reference current of the ADC, I_{ADC} to be substantially constant. This is beneficial when an RC filter may be required to reduce the reference noise, as shown in Figure 8. The result is a constant voltage drop across the resistor with no input dependent terms added to $VREF_{ADC}$. A provision is designed to digitally correct for the gain error at the system level depending on the value of R and the voltage measured at the reference pin. Hence, this simple reference interface will not have gain or linearity errors.

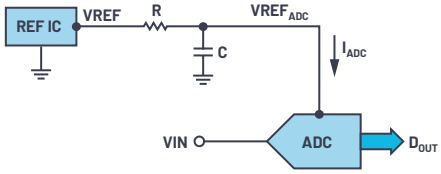

Figure 8. A resistive reference load enabling a direct connection to a reference IC with a passive filter.

Even though a provision has been implemented to digitally correct for the error caused by the voltage drop across R, one might wonder if this would limit the full-scale range of the CTSD ADC, as the actual reference ($VREF_{ADC}$) of the ADC would be lesser than the applied VREF.

For example, if the VREF of the reference IC is trimmed and set to 4.096 V and the ADC reference current (I_{ADC}) = 6 mA, then, for a filter resistance of R = 20 Ω, the actual reference of the ADC ($VREF_{ADC}$) is 3.967 V. This is shown in Equation 5. In such a case, when the specified full-scale differential input of 2 × VREF = 8.192 V p-p (which is greater than 2 × $VREF_{ADC}$) is applied at the input of the ADC, is there a possibility of saturating the output of the ADC? The answer is "no." CTSD ADCs are designed to support input magnitudes that are a few mV beyond the reference at the ADC pin, REFIN. In our example case of AD4134, this extended range limits the resistor value to a maximum of 25 Ω. The value of C for the noise filter is then chosen to satisfy the noise bandwidth calculated.

Reference Drive Design Simplified

CTSD ADCs have eased the design of the reference drive, but there are still additional factors to consider when selecting the correct R for the filter followed by digital gain error correction of the voltage drop across the resistor. Digital gain error correction, also known as calibration, is a common feature in many ADCs, and it offers signal chain designers the freedom to compensate for errors in the signal chain at the digital output of an ADC. As such, it may not require an added design step but rather reuse of the same algorithm, which is common for many signal chains. At the face of it then, the selection of resistor doesn't seem to be a particularly involved design step, but there is one caveat: the temperature dependence of the voltage drop. The external filter resistor and I_{ADC} drift differently with temperature, which in turn causes $VREF_{ADC}$ and the gain of the ADC to drift with temperature. For applications with stringent gain drift requirements, a crude solution consists of calibrating the signal chain periodically. But a much better and innovative solution is made possible because of CTSD technology. Since the ADC reference load current is a constant and function of resistive material used on-chip, it was possible to provide the filter resistor, R, with 20 Ω on-chip, as shown in Figure 9.

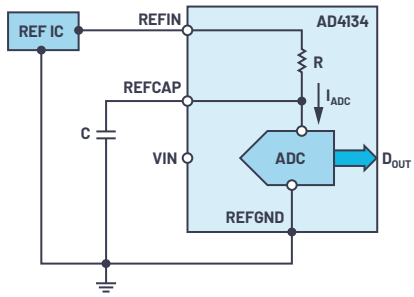

Figure 9. An on-chip reference noise filter resistor simplifying the reference front-end design for a CTSD ADC.

In the new front-end design, the reference IC is connected at the REFIN pin and the filter capacitor is connected at the REFCAP pin to form the noise filter for the reference IC noise. Since the resistance of the on-chip resistor R and the I_{ADC} are both functions of the same resistor material, there is no temperature drift on REFCAP ($VREF_{ADC}$). AD4134 also uses a patented on-chip reference correction algorithm to digitally self-calibrate for the voltage drop across the on-chip resistor. Thus, the reference drive design is now simplified to the selection of the reference IC and capacitor value based on the performance requirements.

ADR444 is one of the low noise reference ICs that can be used as a companion for a CTSD ADC. The AD4134's data sheet has further details on the capacitor value selection and the internal and external digital gain calibration.

Conclusion

CTSD ADCs eliminate many of the barriers to achieving optimal precision performance and simplified front-end design. In upcoming articles, we will cover how a CTSD ADC modulator core's output is processed into its final digital output format for use by an external digital controller for optimum processing. From the sigma-delta basics explained throughout this series, we know the modulator output cannot be processed directly, as it is sampled at a much higher rate. There is a need to reduce the sample rate to the required output data rate (ODR) of the application. Next, we will introduce a novel asynchronous sample rate conversion (ASRC) technique that enables signal chain designers to tune the final ADC output at any desired ODR and go beyond the age-old restriction of limiting ODR to a multiple of sampling frequency. Stay put for these interesting insights!

References

"Driving Precision Converters: Selecting Voltage References and Amplifiers." Analog Devices, Inc.

Mahaffey, Anna. "Driving SAR ADCs Part 1: Analog Input Model." Analog Devices, Inc.

Shah, Anshul. "Why Does Voltage Reference Noise Matter?" *Analog Dialogue*, Vol. 54, No. 1, March 2020.

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Optimizing Power Systems for the Signal Chain—Part 3: RF Transceivers

Pablo Perez, Jr., Senior Applications Engineer and
John Martin Dela Cruz, Applications Engineer

Introduction

Part 1 of this signal chain power optimization series discusses how power supply noise can be quantified to identify which parameters of signal chain devices it affects. An optimized power distribution network (PDN) can be created by determining the actual noise limits the signal processing devices can accept without affecting the integrity of the signals they produce. In Part 2, this methodology is applied to high speed analog-to-digital and digital-to-analog converters, where it demonstrates that lowering noise to a necessary level does not always equate to higher cost, increased sized, and lower efficiency. These design parameters can actually be met in one optimized power solution.

This article focuses on another part of the signal chain—the RF transceivers. Here, we check the sensitivity of the device to the noise coming from each power rail to identify which ones need additional noise filtering. An optimized power solution is provided, which is further validated by comparing its SFDR and phase noise performance to the current PDN when attached to the RF transceiver.

Optimizing the Power System for the ADRV9009 6 GHz Dual RF Transceiver

The ADRV9009 is a highly integrated, radio frequency (RF), agile transceiver offering dual transmitters and receivers, integrated synthesizers, and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption demanded by 3G, 4G, and 5G macrocell time division duplex (TDD) base station applications.

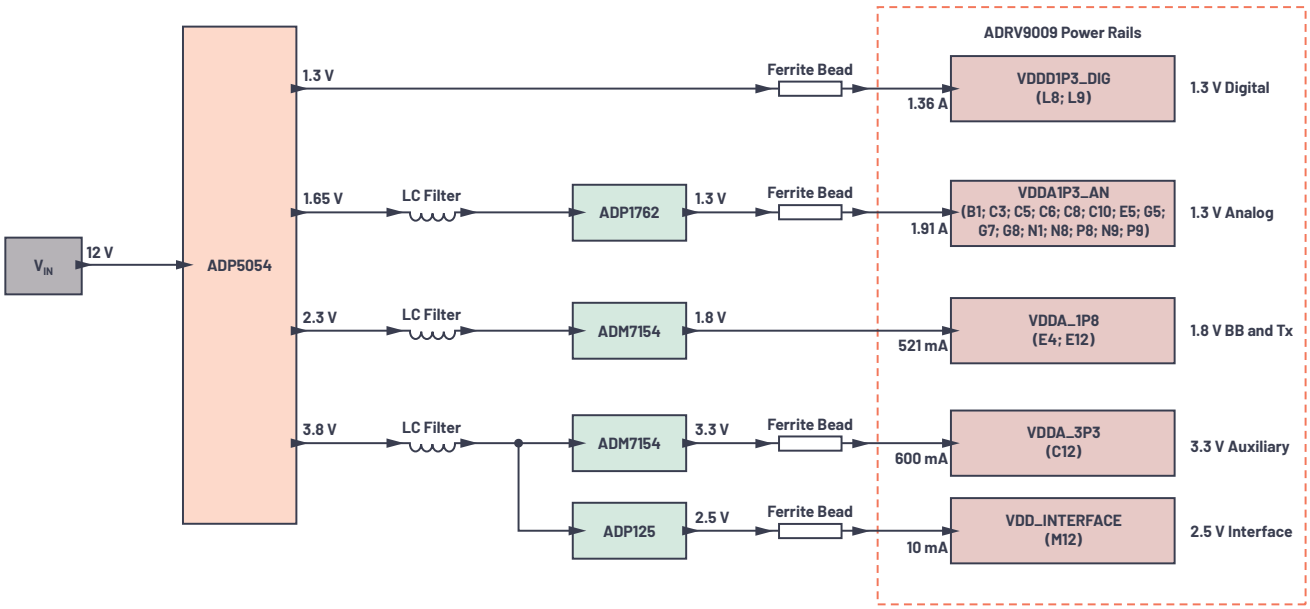


Figure 1. A standard evaluation board power distribution network for the ADRV9009 dual transceiver. This setup uses an ADP5054 quad regulator with four LDO postregulators to meet noise specifications and maximize the performance of the transceiver. The goal is to improve on this solution.

Figure 1 shows the standard PDN for the ADRV9009 dual transceiver. The PDN consists of an ADP5054 quad switcher with four linear regulators. The goal here is to see what performance parameters of the power distribution network can be improved, while producing noise that does not degrade the performance of the transceiver.

As shown throughout this series,[1,2] quantifying the sensitivity of ADRV9009 to power supply noise is necessary to optimize the PDN. The ADRV9009 6 GHz dual RF transceiver requires five different power rails, namely:

- 1.3 V analog (VDDA1P3_AN)
- 1.3 V digital (VDDD1P3_DIG)
- 1.8 V transmitter and BB (VDDA_1P8)
- 2.5 V interface (VDD_INTERFACE)
- 3.3 V auxiliary (VDDA_3P3)

Analysis

Figure 2 shows the Receiver 1 port PSMR results for the analog rails (VDDA1P3_AN, VDDA_1P8, and VDDA_3P3). For the digital rails—VDDD1P3_DIG and VDD_INTERFACE—the maximum injected ripple we could produce with a signal generator did not produce spurs in the output spectrum, so we don't need to worry about minimizing ripple on those rails. Modulated spur amplitude is expressed in dBFS where the maximum output power (0 dBFS) is equivalent to 7 dBm or 1415.89 mV p-p in a 50 Ω system.

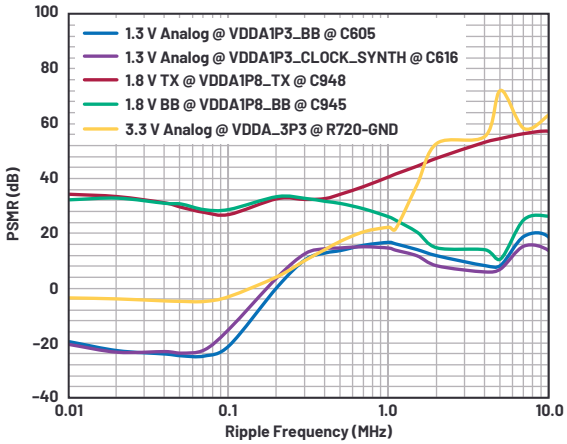


Figure 2. The PSMR performance of the analog supply rails of the ADRV9009 transceiver at Receiver 1.

For the VDDA1P3_AN rail, the measurement was taken at two different branches of the transceiver board. Notice that in Figure 2, PSMR falls below 0 dB at <200 kHz ripple frequency, indicating that ripple at these frequencies produces even higher modulation spurs in the same magnitude. This means that below 200 kHz, Receiver 1 is very sensitive to even the smallest ripple that the VDDA1P3_AN rail produces.

The VDDA_1P8 rail is divided into two branches in the transceiver board: VDDA1P8_TX and VDDA1P8_BB. The VDDA1P8_TX rail reaches a minimum PSMR at 100 kHz at around ~27 dB, corresponding to 63.25 mV p-p of 100 kHz ripple, resulting in modulated spurs of 2.77 mV p-p. VDDA1P8_BB measures a minimum of ~11 dB at a 5 MHz ripple frequency, equivalent to 0.038 mV p-p spurs produced by 0.136 mV p-p of injected ripple.

VDDA_3P3 data shows that at around 130 kHz and below, PSMR falls below 0 dB, which indicates that the RF signal at Receiver 1 is very sensitive to noise coming from VDDA_3P3. The PSMR for this rail rises as the frequency increases, reaching up to 72.5 dB at 5 MHz.

In sum, the PSMR results show that among the power supply rails, VDDA1P3_AN and VDDA_3P3 rail noise are the most worrisome, contributing the most significant ripple content coupled to Receiver 1 of the ADRV9009 transceiver.

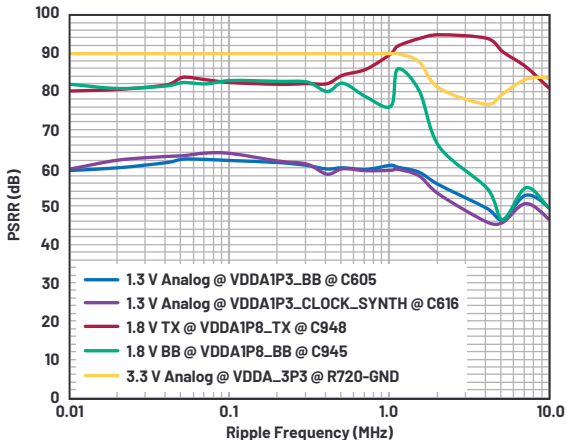


Figure 3. The PSRR performance of the analog supply rails of the ADRV9009 transceiver at Receiver 1.

Figure 3 shows the PSRR performance of ADRV9009 for the analog supply rails. VDDA1P3_AN's PSRR is flat at ~60 dB up to 1 MHz, and it slightly falls to a minimum of ~46 dB at 5 MHz. This can be viewed as a 0.127 mV p-p of 5 MHz ripple that produces a 0.001 mV p-p spur riding the LO frequency together with the modulated RF signal.

The PSRR for the VDDA1P8_BB rail of the ADRV9009 bottoms out at ~47 dB at 5 MHz, while the VDDA1P8_TX rail's PSRR doesn't fall below ~80 dB. In the spectrum below 1 MHz, the PSRR of VDDA_3P3 is higher than the shown 90 dB. The measurement is clipped at 90 dB as the maximum injected ripple up to 1 MHz is 20 mV p-p—not high enough to produce spurs above the noise floor of the local oscillator. The PSRR for that rail is higher than what's shown below 1 MHz, and as the frequency increases, it drops to 76.8 dB at 4 MHz, its lowest value in the 10 kHz to 10 MHz range.

Similar to the PSMR results, PSRR data shows that the majority of the noise coupled to the local oscillator frequency, particularly above 1 MHz, comes from the VDDA1P3_AN and VDDA_3P3 rails.

To determine if a power supply can meet noise requirements, the ripple output of the DC power supply is measured, resulting in a waveform plotted across 100 Hz to 100 MHz frequency range, like that shown in Figure 4. To this spectrum, an overlay is added: the threshold at which sideband spurs will appear at the modulated signal. The overlaid data is obtained by injecting sinusoidal ripple into the specified power supply rail at several reference points, to see what ripple levels produce sideband spurs, as discussed in Part 1 of this series.

The threshold data shown in Figure 4 to Figure 6 are for the three supply rails to which the transceiver is most sensitive. The power rail spectra are shown for various DC-to-DC converter configurations, with and without spread spectrum frequency modulation (SSFM) enabled or additional filtering via LDO regulator or low-pass (LC) filter. These waveforms are measured at the power supply board to give room for additional margin that is greater than or equal to 6 dB below the noise limit.

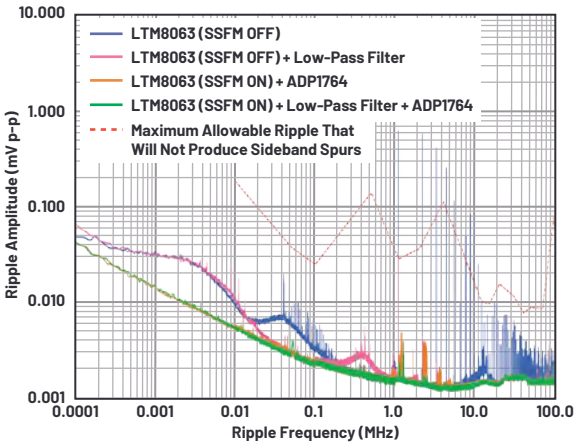


Figure 4. The output noise spectrum of the LTM8063 (various configurations) powering the VDDA1P3_AN rail, along with the maximum allowable ripple for that rail.

Testing

Figure 4 shows the spur threshold for the VDDA1P3_AN rail along with the measured noise spectrum for various configurations of an LTM8063 µModule® regulator. As shown in Figure 4, using the LTM8063 directly powering the rail with spread spectrum frequency modulation (SSFM) disabled produces ripple at the LTM8063's fundamental operating frequency and harmonics that exceed the threshold. In particular, the ripple exceeds the limit by 0.57 mV at 1.1 MHz, indicating that some combination of postregulator and filter is needed to suppress the noise coming from the switching regulator.

If only an LC filter is added (no LDO regulator), the ripple at the switching frequency just reaches the maximum allowable ripple—there's probably not enough design margin to ensure top performance of the transceiver. Adding an ADP1764 LDO postregulator and turning on the LTM8063's spread spectrum mode lowers the fundamental switching ripple amplitude and its harmonics over the entire spectrum, and the noise peaks due to SSFM in the 1/f region. The optimum result is achieved by turning on SSFM, and adding both an LDO regulator and LC filter, which reduces the remaining noise caused by the switching action—leaving an ~18 dB margin from the maximum allowable ripple.

Spread spectrum frequency modulation spreads noise over a wider band, thereby reducing the peak and average noise at the switching frequency and its harmonics. This is done by modulating the switching frequency up and down by a 3 kHz triangle wave. This introduces new ripple at 3 kHz, which is taken care of by the LDO regulator.

When SSFM is enabled, the resulting low frequency ripple and its harmonics are apparent in the VDDA_1P8 and VDDA_3P3 output spectrums shown in Figure 5 and Figure 6, respectively. As shown in Figure 5, the noise spectrum of the LTM8074 with SSFM enabled provides a minimum ~8 dB margin to the maximum allowable ripple for the VDDA_1P8 rail. So no postregulator filtering is necessary to meet the noise requirements on this rail.

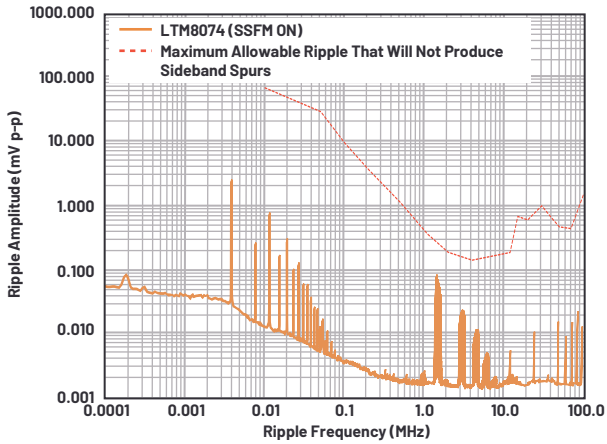


Figure 5. The output noise spectrum of the LTM8074 (with SSFM on) powering the VDDA_1P8 rail, along with the maximum allowable ripple for that rail.

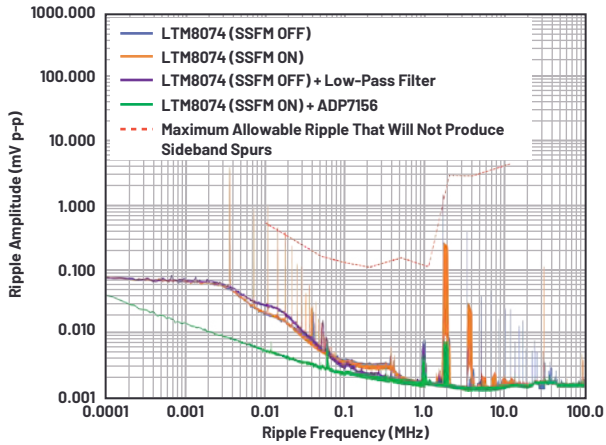


Figure 6. The output noise spectrum of the LTM8074 (in various configurations) powering the VDDA_3P3 rail, along with the maximum allowable ripple for that rail. Note the rail's sensitivity to low frequency ripple due to the possibility of this noise inducing phase jitter in the 3.3 V supplied clock.

Figure 6 shows the noise spectrum for various configurations of the LTM8074 µModule regulator, along with the maximum noise requirements for the 3.3 V VDDA_3P3 rail. For this rail, we're examining the results using the LTM8074 Silent Switcher® µModule regulator. The LTM8074-only configuration (no filter or LDO postregulator) produces noise that exceeds the limit regardless of whether spread spectrum mode is enabled or disabled.

The results of two alternate configurations meet the noise specification with >6 dB margin: the LTM8074 without SSFM enabled plus an LC filter, and the LTM8074 with SSFM enabled with an LDO postregulator. Although both meet the requirement with sufficient margin, the LDO postregulator solution gets the edge here. This is because the VDDA_3P3 rail also provides the 3P3V_CLK1 clock supply, so a reduction of 1/f noise is relatively more important, as noise here could translate to phase jitter in the local oscillator if not addressed.

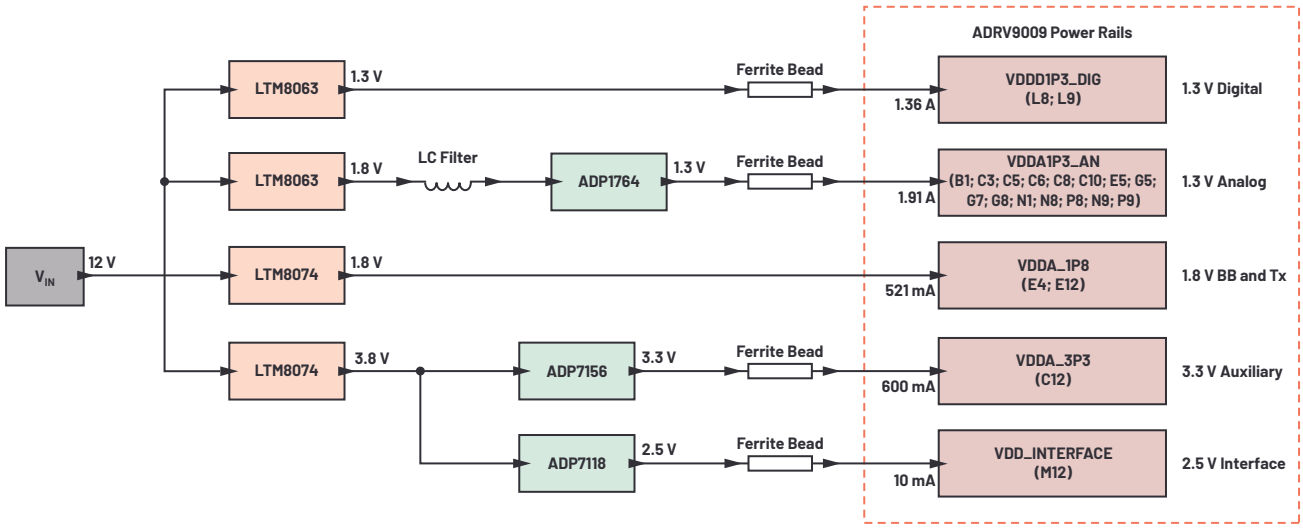


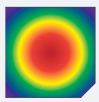
Figure 7. An optimized PDN for an ADRV9009 transceiver using LTM8063 and LTM8074 µModule regulators.

Optimized Solution

Based on the outcome of tests above, Figure 7 shows an optimized solution that would give >6 dB noise margin when used on an ADRV9009 transceiver board.

Table 1 shows the comparison of the optimized PDN to the standard PDN. The component area reduction is 29.8%, and the efficiency has increased to 69.9% (from 65.7%) with an overall power saving of 0.6 W.

Table 1. Comparison of ADRV9009 Optimized PDN to the Current PDN

	Current PDN as Shown in Figure 1	Optimized PDN as Shown in Figure 7	Improvement of the Optimized PDN from the Current PDN
Component Area	148.2 mm² 	104.0 mm² 	29.8%
Overall Efficiency	65.7% 	69.9% 	4.2%
Power Loss	3.8 W 	3.2 W 	0.6 W

To validate the efficacy of this optimized power solution—in terms of systematic noise performance—a phase noise measurement is performed. The optimized solution in Figure 7 is compared to the control case—an engineering release version of the ADRV9009 evaluation board, namely the AD9378 evaluation board using the PDN shown in Figure 1. The same board is used, but with the PDN as shown in Figure 7, and the phase noise results were compared. Ideally, the optimized solution meets or exceeds the data sheet reference graphs.

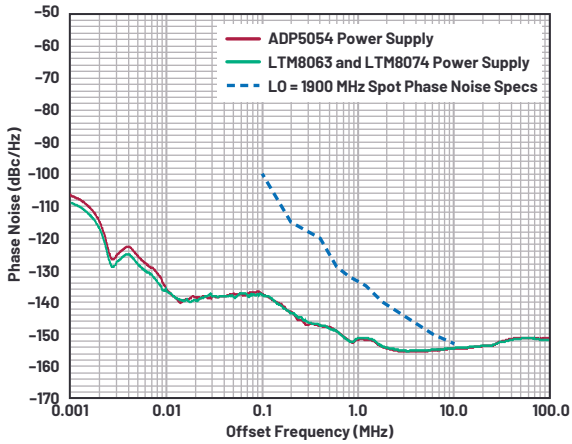


Figure 8. An AD9378 phase noise performance comparison between an ADP5054 and a µModule device's PSU taken at LO = 1900 MHz, PLL BW = 425 kHz, and stability = 8.

Figure 8 shows the phase noise results of the AD9378 evaluation board with the standard ADP5054-based power supply compared to the results from the same board using a power supply based on the LTM8063 and LTM8074. The µModule power solution has slightly better performance of around 2 dB vs. the ADP5054 power solution. As seen in Figure 8 and Table 2, measurement results for both power solutions are significantly lower than the data sheet specs due to the use of a low phase noise signal generator for the external local oscillator.

Table 2. Phase Noise Measurement Result at LO = 1900 MHz

Offset Frequency (MHz)	Phase Noise (dBc/Hz)		
	Data Sheet Specifications	Evaluation Results	
		ADP5054	LTM8063 and LTM8074
0.1	–100	–137.74	–137.77
0.2	–115	–143.16	–143.32
0.4	–120	–147.37	–147.20
0.6	–129	–149.02	–149.04
0.8	–132	–151.81	–151.96
1.2	–135	–151.73	–151.22
1.8	–140	–153.97	–153.76
6	–150	–155.10	–154.80
10	–153	–154.51	–154.36

The transceiver's SFDR measurement using both power solutions, as shown in Table 3, shows comparable performance for both power solutions, except for LO = 3800 MHz where ADP5054's switching ripple starts to produce modulation spurs on the carrier signal output spectrum, as seen in Figure 9.

Table 3. ADRV9009 Transceiver SFDR Performance

LO Frequency (MHz)	SFDR (dBc)				
	Data Sheet Specifications	Tx1		Tx2	
		ADP5054	LTM8063 and LTM8074	ADP5054	LTM8063 and LTM8074
800	70.00	86.03	86.95	86.62	86.63
1800	70.00	85.94	87.30	86.01	85.90
2600	70.00	85.98	86.01	85.50	85.78
3800	70.00	73.87	77.42	73.93	77.31
4800	70.00	71.44	71.98	71.10	71.82

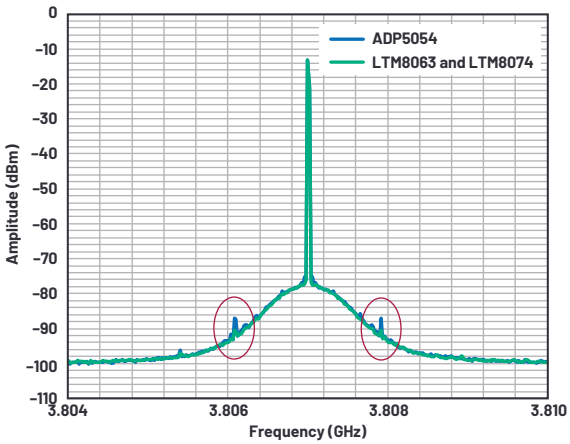


Figure 9. Transmitter 1 carrier signal and spurious frequency due to power supply switching frequency. The measurements were taken at LO = 3800 MHz, Fbb = 7 MHz, –10 dBm.

Conclusion

Different requirements for various applications could demand further improvement or changes in the power distribution networks of the evaluation boards. Being able to quantify the noise requirements of signal processing ICs provides a more effective way of designing its power supply or even just optimizing the existing power solution. For high performance RF transceivers such as the ADRV9009, setting up noise injection in the PDN to identify how much power supply noise is tolerable helped us make improvements in space requirements, efficiency, and, critically, thermal performance over the current PDN. Keep following this power system optimization series for succeeding entries.

References

[1] Pablo Perez, Jr. and Patrick Errgy Pasaquian. "Optimizing Power Systems for the Signal Chain—Part 1: How Much Power Supply Noise Is Tolerable?" *Analog Dialogue*, Vol. 55, No. 1, March 2021.

[2] John Martin Dela Cruz and Patrick Errgy Pasaquian. "Optimizing Power Systems for the Signal Chain—Part 2: High Speed Data Converters." *Analog Dialogue*, Vol. 55, No. 2, April 2021.

Delos, Peter. "Power Supply Modulation Ratio Demystified: How Does PSMR Differ from PSRR?" Analog Devices, Inc., December 2018.

Delos, Peter. "Transceiver Phase Noise Teardown Informs Performance Capability with an External LO." Analog Devices, Inc., October 2019.

Naeem, Naveed and Samantha Fontaine. "Characterizing the PSRR of Data Acquisition µModule Devices with Internal Bypass Capacitors." *Analog Dialogue*, Vol. 54, No. 3, July 2020.

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RAQ Issue 189: Isolation for SAR ADCs

Wilfried Platzer, Applications Engineer

Question:

How do I add isolation to my ADC without harming its performance?

Answer:

For isolated high performance ADCs, keep one eye on isolated clocks and a second on isolated power.

SAR ADCs have traditionally been used for lower sample rates and lower resolution. Nowadays, fast, high precision, 20-bit SAR ADCs sampling at 1 MSPS like the LTC2378-20 and oversampled SAR ADCs with 32-bit resolution like the LTC2500-32 are available. When designing for high performance to utilize the ADC performance, very low noise is required across the complete signal chain. When additional isolation is required for a signal chain, performance will be impacted.

There are three isolation topics to consider:

- Isolated power to ensure the hot side is powered
- Data isolation to ensure the datapath is isolated
- Clock isolation for the ADC (sample clock or conversion signal), in case the clock is not generated at the hot side

Isolated Power (Comparison Between Flyback and Push-Pull Topology)

For sensor applications, isolated power is usually in a less than 10 W range.

Flyback converters are widely chosen to isolate power. Figure 1 shows the simplicity of a flyback converter. The topology's advantage is that only a few external components are required. Flyback converters have only one integrated switch. This switch can be the main noise source impacting signal chain performance. For high performance analog design, the flyback converter comes with many high discontinuities in the form of electromagnetic radiation called EMI, which can limit the performance of your circuit.

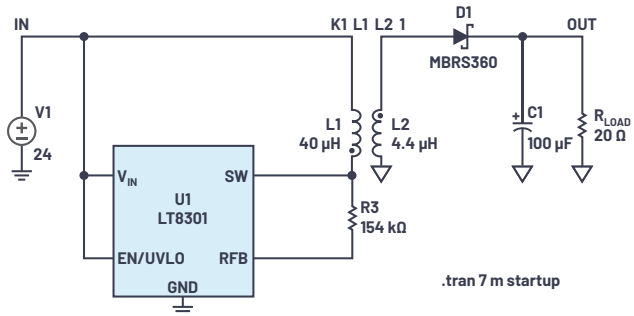

Figure 1. A typical flyback converter topology.

Figure 2 shows the current in transformers L1 and L2. The currents jump from high values to zero in a short period of time in the primary (L1) and secondary (L2) windings. The current spikes can be seen in the I(L1)/I(L2) traces in Figure 3. Current and energy are built up in the primary inductance and they are transferred while the switch is off to the secondary inductance, which creates transients. Those transients of the switching noise effects need to be reduced, and, consequently, snubbers and filters must be inserted in the design. Aside from the additional filters, an additional disadvantage of the flyback topology is that the utilization of the magnetic material is low, leading to larger transformers due to the required high inductances. Furthermore, the hot loops of the flyback converter are large and not easy to manage. For background information on hot loops, please read Application Note AN139.

Another challenge of the flyback converter involves the switching frequency change. Figure 3 shows a frequency change due to load change. As seen in Figure 3a, t1 < t2. This means that f_{SWITCH} is when the load current decreases from the higher load current I1 to the lower load current I2. The variations in frequency create internal noise at unpredictable times. In addition, the frequencies also will differ from part to part, which will make it more difficult to filter them as adjusted filtering would be required for each individual PCB. Taking a 20-bit SAR ADC, with a 5 V input span, one LSB corresponds to ~5 µV. The errors introduced through EMI noise should be below 5 µV, which means that a flyback topology should not be selected when isolating power for a precision system.

There are other isolated power architectures with lower radiating emissions. Push-pull converters are much better suited in respect to radiation compared to flyback converters. A push-pull regulator like the LT3999 offers the possibility of clock synchronization to the ADC and helps to achieve high performance. Figure 4 shows the LT3999 in an isolated power circuit with synchronization to an ADC sampling clock. Remember that the primary to secondary capacitor provide switching noise a return path to avoid common-mode noise effects. This capacitor may be realized in a PCB design with overlapping primary and secondary planes and/or with a real capacitor.

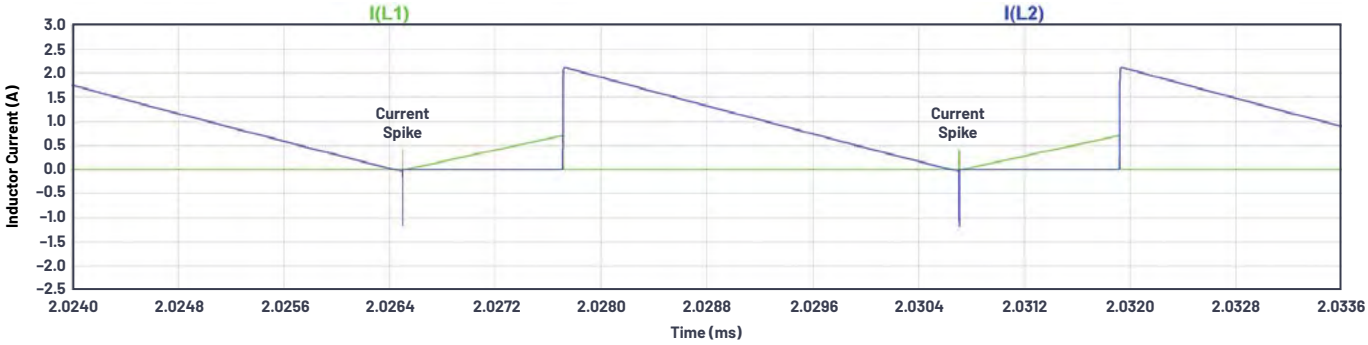

Figure 2. LT8301 switching currents in the transformer windings.

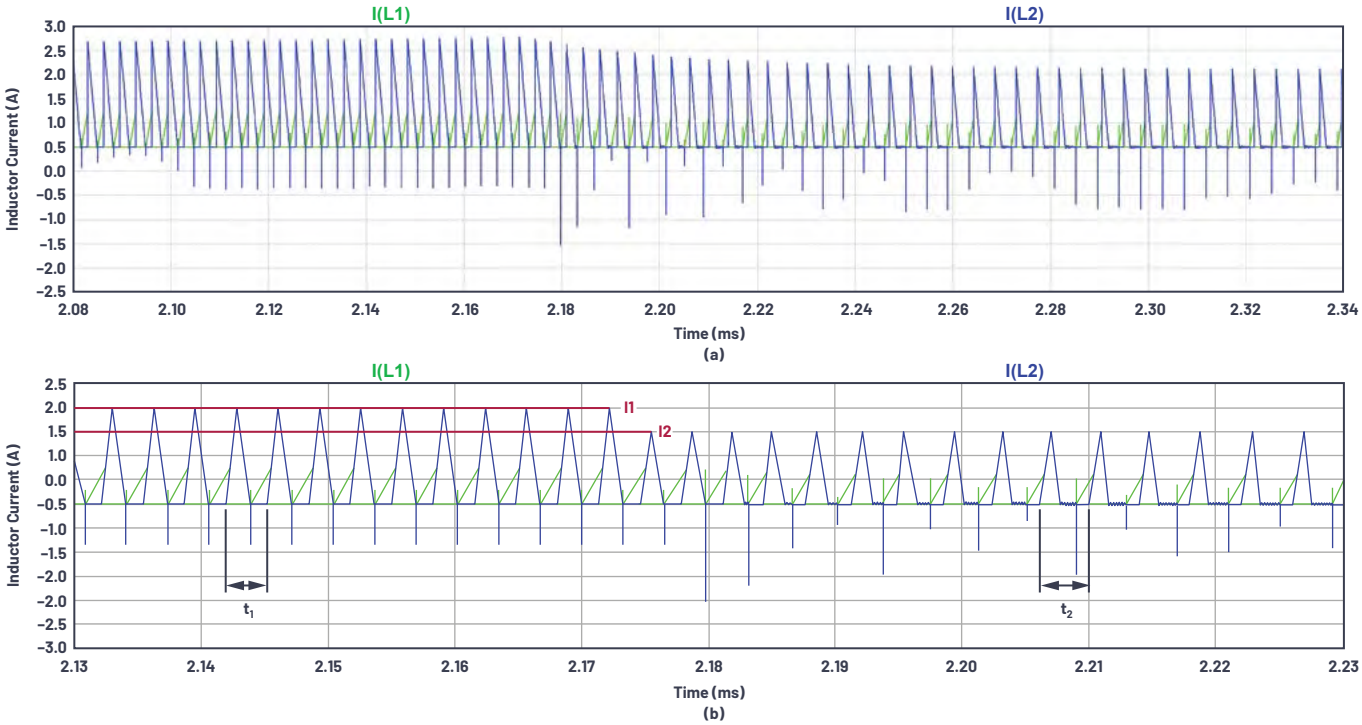

Figure 3. (a) LT8301 frequency change with (b) a close-up of the frequency change from 2.13 ms to 2.23 ms.

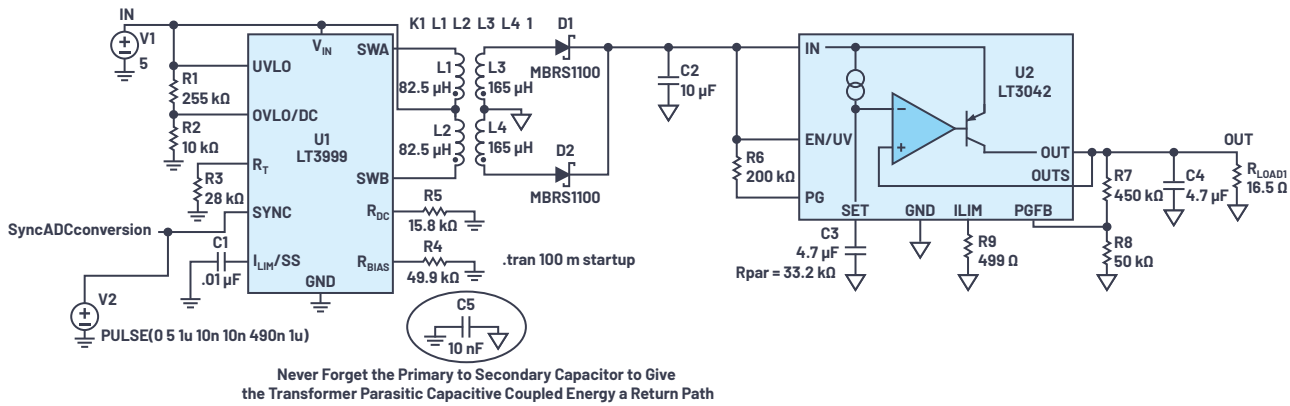

Figure 4. An LT3999 with an ultralow noise postregulator.

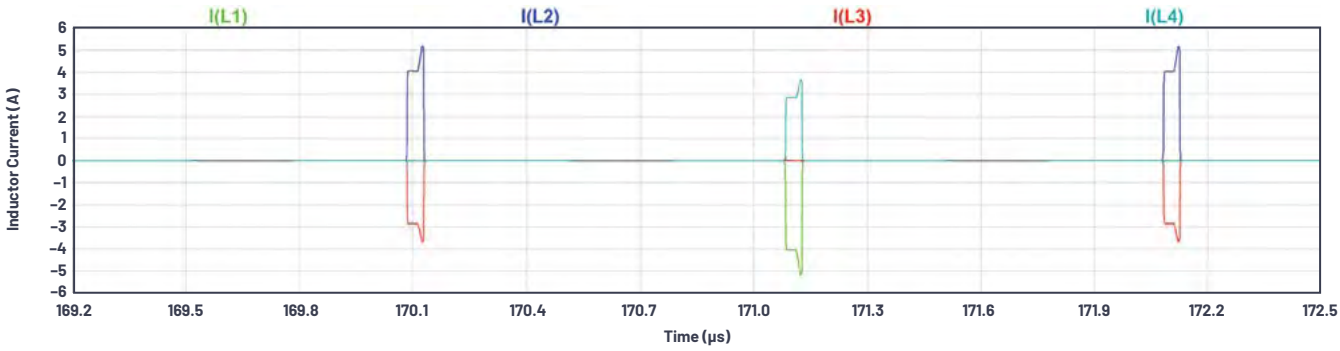

Figure 5. LT3999 current waveforms.

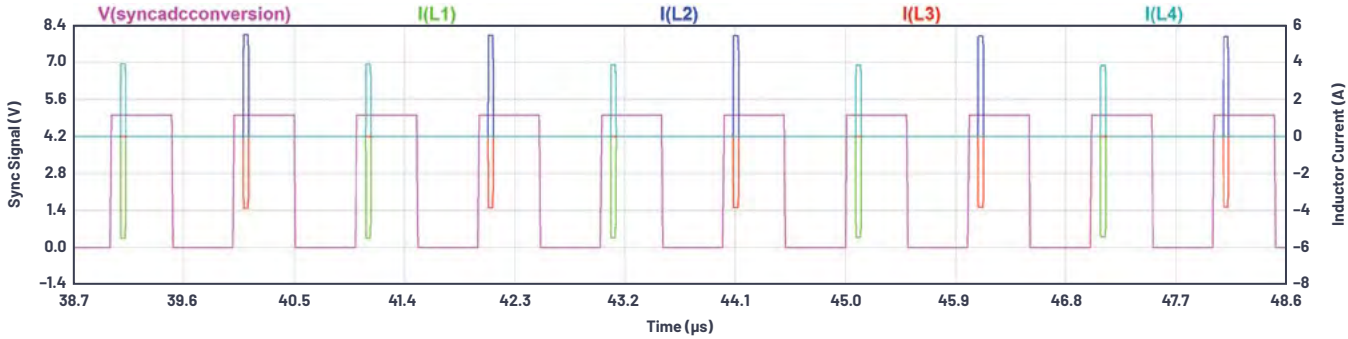

Figure 6. LT3999 and the switching relation to the sync pin.

Figure 5 shows the current waveforms at the transformer (both the primary side and secondary side current), which gives a better utilization of the transformer and provides better EMI behavior.

Figure 6 shows synchronization to an external clock signal. The end of the acquisition phase aligns to the positive edge of the sync pin. As a result, there will be a long quiet time of ~4 µs. This enables the converter to sample an input signal during that timeframe and eliminate the transient effects in the isolated power to a minimum. The LTC2378-20 has an acquisition time of 312 ns, which is ideal for the <1 µs quiet window.

Data Isolation

Data isolation can be done with digital isolators, such as those in the ADuMx family. Those digital isolators are available for many standard interfaces like SPI, I²C, CAN, etc.—for example, the ADuM140 can be used for SPI isolation. To achieve data isolation, the SPI signal SPI clock, SDO, SCK, and Busy just need to be connected to the data isolator. In data isolation, electrical energy is transferred from the primary side to the secondary side through the inductive isolation barrier. A current return path needs to be added, which is done by a capacitor. This capacitor can be built at the PCB with overlapping planes.

Clock Isolation

Clock isolation is another important task. In case you want to have a high performance ADC with 20 bits at a 1 MHz sample rate, such as the LTC2378-20, a signal-to-noise ratio (SNR) of 104 dB SNR is possible. To achieve high performance, a jitter free clock is required. Why shouldn't you use a standard isolator like the ADuM14x series? The standard isolator will limit the performance of the ADC as it adds jitter to the clock. More details can be found in Design Note DN1013.

Figure 7 displays the theoretical limit of the SNR over frequency for various types of clock jitter. High performance ADCs like the LTC2378 have an aperture clock jitter of 4 ps, which gives a theoretical 106 dB limit at 200 kHz input.

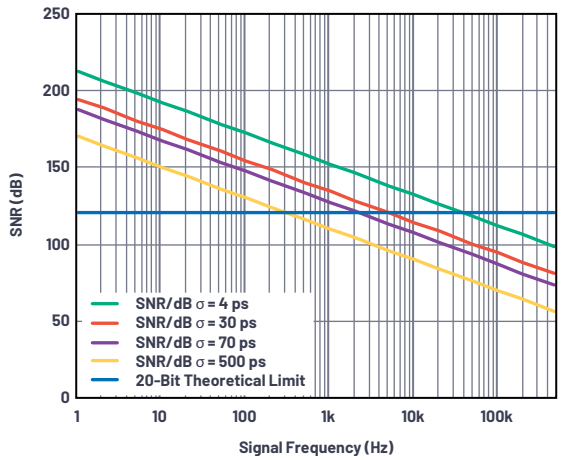

Figure 7. Clock jitter vs. ADC performance.

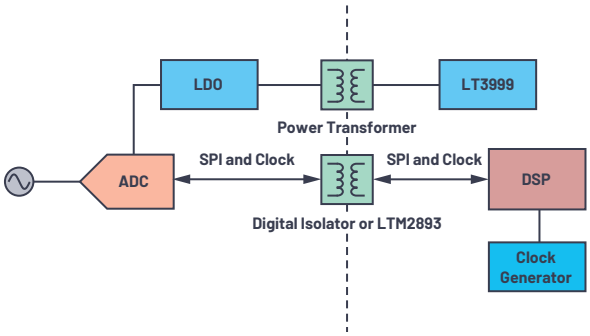

Figure 8. Clock isolation using a standard isolator.

The standard clock isolator concepts depicted in Figure 8 include:

- A good standard digital isolator like the ADuM250N has a jitter of 70 ps rms. For a 100 dB SNR goal, the signal sample rates are limited to 20 kHz due to the clock jitter.
- An optimized clock isolator like LTM2893 provides a reduced jitter of 30 ps rms. For a 100 dB SNR goal, the signal sample rate is now 50 kHz, which gives you more bandwidth at full SNR performance.

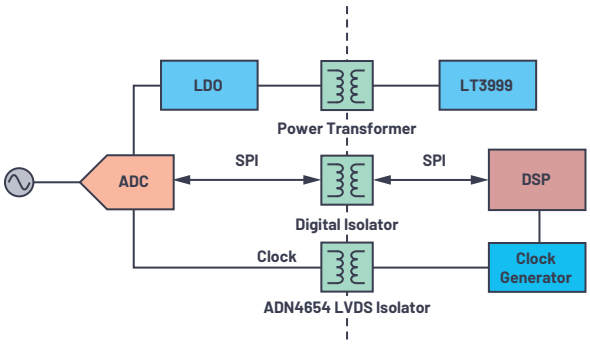

Figure 9. Clock isolation using an LVDS clock isolator.

- Figure 9: For higher input frequencies, LVDS isolators should be used. ADN4654 provides a 2.6 ps jitter, which brings you close to the best performance for an ADC. The SNR limit through clock jitter at 100 kHz input would be 110 dB.

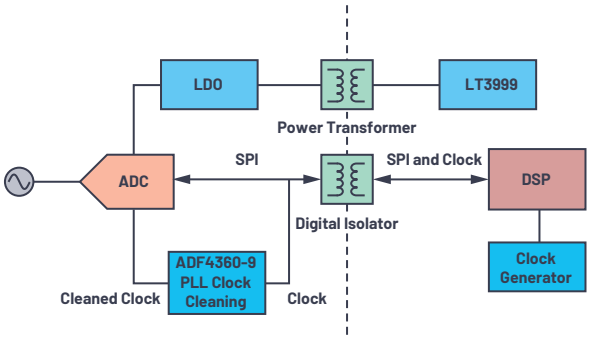

Figure 10. Clock isolation using an additional PLL for clock jitter cleaning.

- Figure 10: This shows the use of a PLL for clock cleaning. An ADF4360-9 can help to reduce the clock jitter.

A more detailed block diagram for a clock cleaning with a PLL is shown in Figure 11. You can use the ADF4360-9 as a clock cleaner and add a divider by 2 to the output. The AD7760 is characterized to 1.1 MHz.

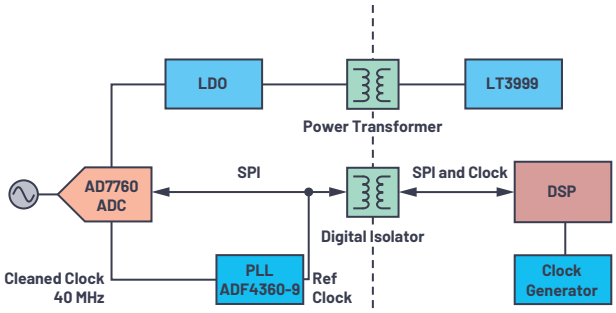

Figure 11. An ADF4360-9 used as a clock cleaner.

So a 1 MSPS SAR ADC like the LTC2378 will not directly be supported. A low jitter flip-flop helps in this case. It divides the clock by 2.

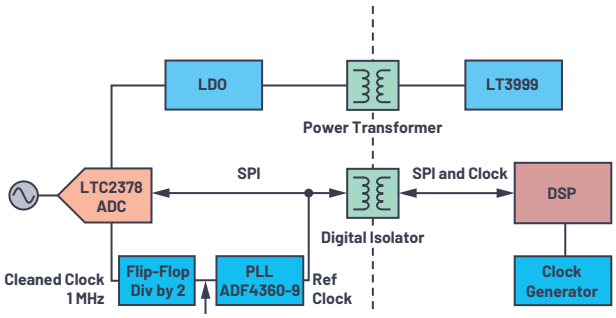

Figure 12. A flip-flop used to get the clock down for the LTC2378.

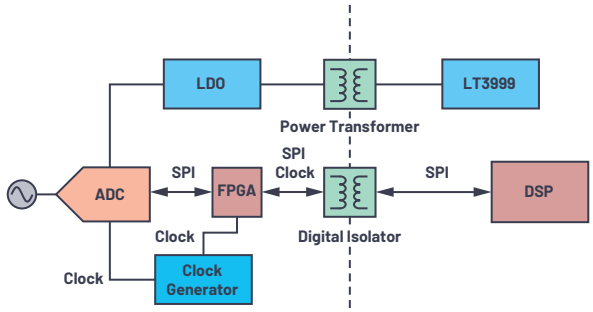

Figure 13. Clock generation at the isolated (hot) side.

- Figure 13: Local clock generation is another option to get a clock with the required jitter performance. Local clock generation makes the clocking architecture more complicated as it introduces asynchronous clock domains to the system. For example, if you want to use two separate isolated ADCs, the clocks will differ in absolute frequency and a sample rate conversion must be added to match the clocks again. Some details on sample rate conversion can be found in the Engineer-to-Engineer Note, EE-268.

Clocking for High Performance Sigma-Delta ADCs

Similar problems with the clocks apply also for high performance sigma-delta ADCs like the AD7760. Here the important clock signal is the jitter free oversampling clock at, for example, 40 MHz. In this case, no additional dividers are required.

Conclusion

Isolated high performance ADCs require a careful isolated design and a selection of various isolation techniques to achieve a high performance SNR above 100 dB. Specific care should be taken on the isolated clock, as the influence of the clock jitter could destroy the performance. Secondly, care should be given to isolated power. Simple isolation topologies like a flyback introduce high EMI transients. For better performance, a push-pull converter should be used. Data isolation is another, albeit less important, concern as standard available devices offer good performance and have less impact to the overall system performance. Addressing these three isolation topics enables the designer to come up with a high performance isolated system solution.

About the Author

Wilfried Platzer studied information technology with an emphasis on RF in Karlsruhe, Germany. He started at ITT in 1997 and later worked at TDK-Micronas. Wilfried has held several positions starting as a field applications engineer and then focusing on IC concept and IC system architecture engineering for mixed-signal ICs. After 11 years, he moved to an electronic predevelopment position at Auma and in 2015, he joined Linear Technology (now part of Analog Devices). Currently, Wilfried is a senior field applications engineer at Analog Devices, providing regional support for Switzerland. He can be reached at wilfried.platzer@analog.com.

Low Noise and Low Power DAQ Solution for Seismology and Energy Exploration Applications

David Guo, Product Application Engineer and
Steven Xie, Product Application Engineer

Precision data acquisition (DAQ) systems are popular in industrial applications. In some DAQ applications, low power and ultralow noise are required. One example is seismic sensor-related applications, where a lot of information can be extracted from seismic data that is useful for a wide range of applications such as structural health monitoring, geophysical research, oil exploration, and even industrial and household safety.[1]

DAQ Signal Chain Requirements

Seismic geophones are electromechanical conversion devices that convert ground vibration signals into electrical signals. They are suitable for high resolution seismic exploration. They are implanted in the ground along arrays to measure the time of returns of seismic waves as they are reflected off discontinuity surfaces such as bedding planes, as shown in Figure 1.

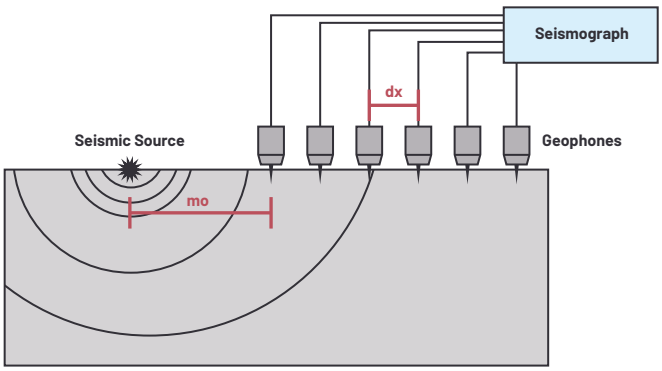

Figure 1. Seismic source and geophone array.

To capture the small output signal from the geophones, a high sensitivity DAQ signal chain must be built for data analysis. The total rms noise should be = 1.0 µV rms with a limited flat low-pass bandwidth range of 300 Hz to ~400 Hz, while the signal chain should achieve a THD of around –120 dB. Since the seismic instrument is battery-supplied, the power dissipation should be balanced around 30 mW.

This article introduces two signal chain solutions to achieve the following targeted requirements:

- Gain of PGIA: 1, 2, 4, 8, 16
- ADC with integrated programmable wideband filter
- RTI noise at gain = 1 (300 Hz to ~400 Hz with –3 dB bandwidth) with 1.0 µV rms
- THD: –120 dB at gain = 1
- CMRR at gain = 1 with >100 dB
- Power consumption (PGIA plus ADC): 33 mW
- Secondary channel for self-test

DAQ Signal Chain Solution

There is no single precision ADC that has all the features and that can achieve such low noise and THD on the ADI website, nor is there a PGIA that can provide such low noise and low power. However, ADI provides great precision amplifiers and precision ADCs to build signal chains to achieve the target.

To build a low noise, low distortion, and low power consumption PGIA, the ultralow noise ADA4084-2 or zero-drift amplifier ADA4522-2 are good candidates.

For very high precision ADCs, the 24-bit sigma-delta ADC AD7768-1 or 32-bit SAR ADC LTC2500-32 can be the best options. They provide configurable ODR with an integrated flat low-pass FIR filter for different DAQ applications.

Seismic Signal Chain Solution: ADA4084-2 PGIA and AD7768-1

The total signal chain is shown in Figure 2. The ADA4084-2, the ADG658, and 0.1% resistors can build a low noise and low THD PGIA for up to eight different selectable gain options. The AD7768-1 is a single-channel low power, –120 dB THD platform. It has a low ripple programmable FIR, DC to 110.8 kHz digital filter, and it uses the LT6657 as its reference device.

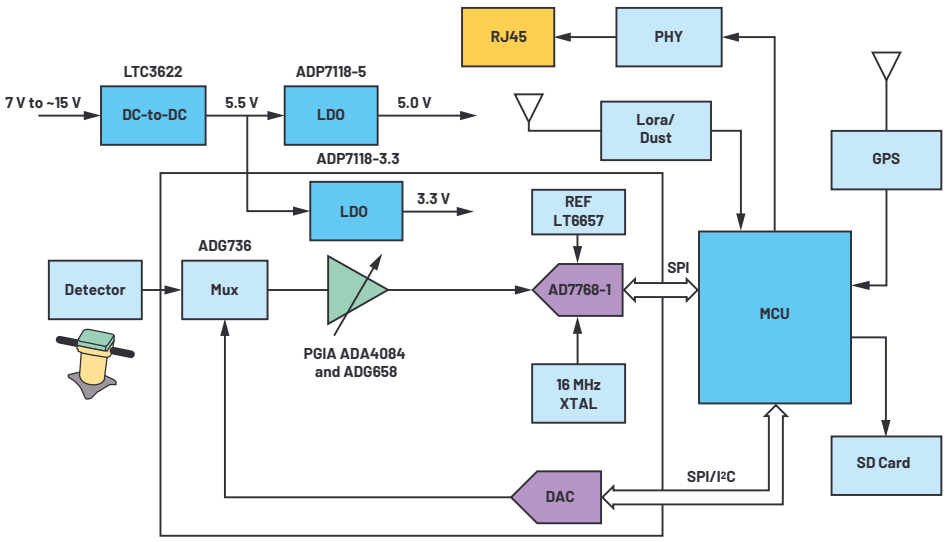

Figure 2. ADA4084-2 PGIA and AD7768-1 plus MCU filtering signal chain solution.

AD7768-1 can get 1.76 µV rms noise running at an ODR of 1 kSPS with power consumption of 10 mW in low power mode. To achieve a final 1.0 µV rms noise, it can run at higher ODR, such as 16 kSPS in median mode. When AD7768-1 runs at higher modulator frequency, it has a lower noise floor, as shown in Figure 3, with higher power consumption. A flat low-pass FIR filter algorithm can be implemented in the MCU software to remove the higher bandwidth noise and decimate the final ODR to 1 kSPS. The final rms noise will be around one fourth of 3.55 µV, which is 0.9 µV.

Table 10. Low Ripple FIR Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V)

ODR (kSPS)	Decimation Rate	−3 dB Bandwidth (kHz)	Shorted Input Dynamic Range (dB)	RMS Noise (µV)
Fast Mode				
256	32	110.8	108.43	10.98
128	64	55.4	111.96	7.31
64	128	27.7	115.15	5.06
32	256	13.9	118.23	3.55
16	512	6.9	121.20	2.52
8	1024	3.5	124.16	1.79
Median Mode				
128	32	55.4	108.45	10.94
64	64	27.7	111.89	7.37
32	128	13.9	115.22	5.02
16	256	6.9	118.22	3.55
8	512	3.5	121.23	2.51
4	1024	1.7	124.17	1.79
Low Power Mode				
32	32	13.9	108.54	10.84
16	64	6.9	112.12	7.17
8	128	3.5	115.30	4.97
4	256	1.7	118.31	3.52
2	512	0.87	121.22	2.52
1	1024	0.43	124.33	1.76

Figure 3. Balancing the AD7768-1's ODR for targeted noise with MCU postfiltering.

As one example, the MCU software FIR filter can be made as shown in Figure 4 to balance performance and group delay.

Seismic Signal Chain Solution: ADA4084-2 PGIA and LTC2500-32

The LTC2500-32 is a low noise, low power, high performance 32-bit SAR ADC with an integrated configurable digital filter. With 32-bit digitally filtered low noise and low INL output, it is targeted for seismology and energy exploration.

A high impedance source should be buffered to minimize settling time during acquisition and to optimize the switch cap input SAR ADC linearity. For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2500-32. A discrete PGIA circuit must be designed to drive LTC2500-32 for both low noise and low THD, which is introduced in the PGIA section.

PGIA Implementation

The key specifications of a PGIA circuit include:

- Power supply: 5 V minimum
- Since the AD7768-1 has 19.7 mW, the PGIA circuit should be <13.3 mW to meet the 33 mW power consumption target
- Noise: the noise at gain = 1 is 0.178 µV rms, about 1/10 of AD7768-1's 1.78 µV rms

There are three types of PGIA topologies:

- An integrated PGIA
- A discrete PGIA with an integrated instrumentation amplifier
- A discrete PGIA with an operational amplifier

Table 1 lists ADI's digital PGIAs. The LTC6915 has the lowest I_0. With 50 nV/√Hz noise density, the integrated noise within the 430 Hz BW is 1.036 µV rms, which exceeds the 0.178 µV rms target. Because of this, an integrated PGIA is not a good choice.

Table 2 lists several instrumentation amplifiers, including the 300 µA I_0 AD8422. The integrated noise within 430 Hz BW is 1.645 µV rms, so it is not a good choice, either.

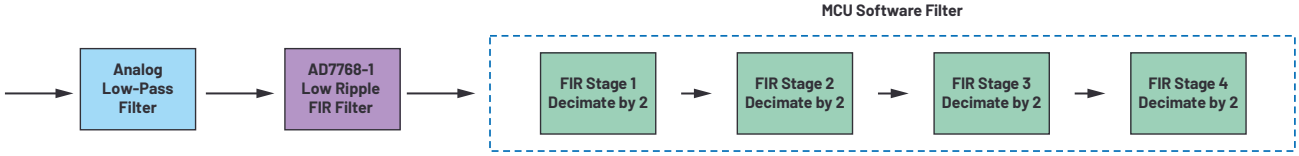

Figure 4. MCU post-FIR filter stages.

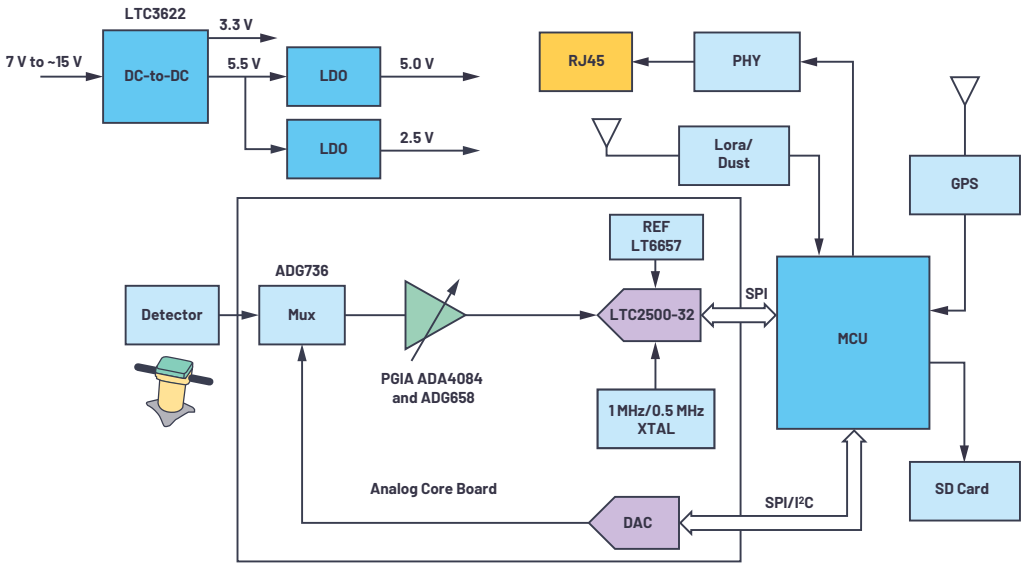

Figure 5. ADA4084-2 PGIA and LTC2500-32 signal chain solution.

Table 2. Digital Filter Parameters for Different Filter Types and Down-Sampling Factors

FILTER TYPE	DOWN-SAMPLING FACTOR (DF)	OUTPUT DATA RATE		–3dB BANDWIDTH		FILTER LENGTH	GROUP DELAY (f_{SMPL} = 1Msps)	DYNAMIC RANGE (dB)	NOISE (µV RMS)
		f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps	f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps				
Flat Passband	4	250ksps	256ksps	85.74kHz	87.80kHz	140	70µs	110.7	10.69
	8	125ksps	128ksps	42.92kHz	43.95kHz	280	140µs	114	7.34
	16	62.5ksps	64ksps	21.47kHz	21.98kHz	560	280µs	116.8	5.33
	32	31.25ksps	32ksps	10.73kHz	10.99kHz	1120	560µs	120	3.68
	64	15.6ksps	16ksps	5.37kHz	5.50kHz	2240	1120µs	122.8	2.66
	128	7.8ksps	8ksps	2.68kHz	2.75kHz	4480	2240µs	126.1	1.83
	256	3.9ksps	4ksps	1.34kHz	1.37kHz	8960	4480µs	129	1.31
	512	1.95ksps	2ksps	670.85Hz	686.95Hz	17920	8960µs	131.4	0.98
	1024	977sps	1ksps	335.42Hz	343.47Hz	35840	17920µs	134	0.73
	2048	488sps	500sps	167.71Hz	171.74Hz	71680	35840µs	136.8	0.53
	4096	244sps	250sps	83.85Hz	85.87Hz	143360	71680µs	138.1	0.45
	8192	122sps	125sps	41.93Hz	42.93Hz	286720	143360µs	139.8	0.37
	16384	61sps	62.5sps	20.96Hz	21.47Hz	573440	286720µs	140.6	0.34

Figure 6. LTC2500-32 flat pass-band filter noise for different downsampling factors.

Table 1. Digital PGIAs

Part Number	Gain (min) (V/V)	Gain (max) (V/V)	I_0/Amp (max) (mA)	V_S Span (min) (V)	V_S Span (max) (V)	Input Voltage Noise (typ) (nV/√Hz)
LTC6915	1	4096	1.6	2.7	11	50
AD8557	28	1300	1.8	2.7	5.5	32
AD8556	70	1280	2.7	5	5.5	32
AD8250	1	10	4.5	10	30	18
AD8251	1	8	4.5	10	34	18

Table 2. Instrumentation Amplifiers

Part Number	Gain (min) (V/V)	Gain (max) (V/V)	I_0/Amp (max)	V_S Span (min) (V)	V_S Span (max) (V)	Input Voltage Noise (typ) (nV/√Hz)
AD8422	1	1000	300 µA	4.6	36	8
LT1168	1	10,000	530 µA	4.6	40	10
AD8220	1	1000	750 µA	4.5	36	14
AD8224	1	1000	800 µA	4.5	36	14
AD8221	1	1000	1 mA	4.6	36	8

Table 3. Low Noise, Low Power Operational Amplifiers

Device	V_{OS} (max) (µV)	I_{BIAS} (max)	GBP (typ) (MHz)	0.1 Hz to 10 Hz V_{NOISE} (typ) (nV p-p)	V_{NOISE} Density (typ) (nV/√Hz)	Current Noise Density (typ) (fA/√Hz)	I_Q/Amp (typ) (µA)	V_S Span (min) (V)	V_S Span (max) (V)
ADA4522-2	5	150 pA	2.7	117	5.8	800	830	4.5	55
ADA4084-2	100	250 nA	15.9	100	3.9	550	625	3	30

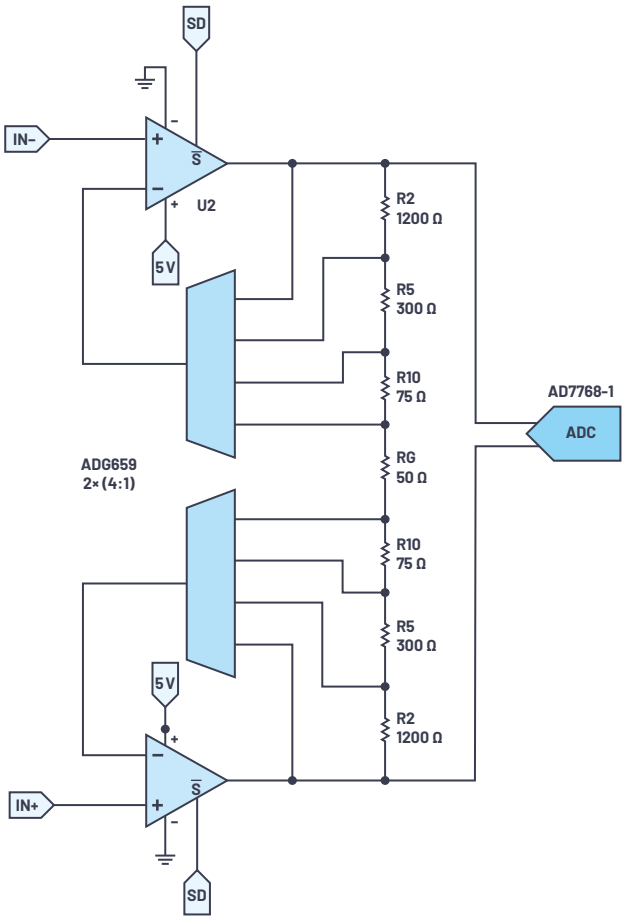

Figure 7. Block diagram of a discrete PGIA.

Discrete PGIA by Operational Amplifiers

The article "Programmable Gain Instrumentation Amplifiers: Finding One that Works for You" discusses the various integrated PGIAs and supplies good guidelines for building a discrete PGIA when trying to meet a specific requirement.[2] Figure 7 shows the block diagram of a discrete PGIA circuit.

ADG659/ADG658 can be chosen with low capacitance and 5 V power supply.

For op amps, I_Q (<1 mA per channel) and noise (<6 nV/√Hz voltage noise density) are key specifications. The precision op amps ADA4522-2 and ADA4084-2 are good choices, with their features listed in Table 3.

For gain resistors, 1.2 kΩ/300 Ω/75 Ω/25 Ω resistors are chosen to achieve 1/4/16/64 gain. With greater resistance, noise may increase, and with lesser resistance, more power consumption is needed. If another gain configuration is needed, resistors must be carefully chosen to ensure the gain accuracy.

A differential input ADC plays the role of subtractor. The CMRR of the ADC is >100 dB, which can meet the system requirement.

Noise Simulation

LTspice® can be used to simulate the noise performance of a discrete PGIA. The integral noise BW is 430 Hz. Table 4 shows the noise simulation result of two different PGIAs and the AD7768-1. The ADA4084 solution has better noise performance, especially at high gain.

Table 4. Noise Simulation Result

	ADA4084 PGIA and AD7768-1	ADA4522 PGIA and AD7768-1
RTI Integrated Noise Within 430 Hz BW and Gain = 1 (µV rms)	1.765	1.774
RTI Integrated Noise Within 430 Hz BW and Gain = 4 (µV rms)	0.744	0.767
RTI Integrated Noise Within 430 Hz BW and Gain = 16 (µV rms)	0.259	0.311
RTI Integrated Noise Within 430 Hz BW and Gain = 64 (µV rms)	0.148	0.225

In-Loop Compensation Circuit to Drive LTC2500-32

The AD7768-1 has an integrated precharge amplifier to ease the driving requirement. For SAR ADCs, such as the LTC2500-32, high speed amplifiers are normally suggested for use as the driver. In this DAQ application, the bandwidth requirement is low. For driving LTC2500-32, an in-loop compensation circuit using the precision amplifier (ADA4084-2) is suggested. Figure 8 shows the in-loop compensation PGIA used to drive the LTC2500-32. The PGIA has the following features:

- R22/C14/R30/C5 and R27/C6/R31/C3 are key components to better stability for in-loop compensation circuitry.
- With ADG659, A1/A0 = 00, gain = 1, and the feedback path of the upper amplifier is amplifier out ⟶ R22 ⟶ R30 ⟶ S1A ⟶ DA ⟶ R6 ⟶ AMP –IN.
- With ADG659, A1/A0 = 11, gain = 64, and the feedback path of the upper amplifier is amplifier out ⟶ R22 ⟶ R8 ⟶ R10 ⟶ R12 ⟶ S4A ⟶ DA ⟶ R6 ⟶ AMP –IN.

The PGIA is connected to LTC2500-32EVB to verify the performance. Different passive component (R22/C14/R30/C5 and R27/C6/R31/C3) values are tried to reach better THD and noise performance at different gain (1/4/16/64). The final components values are: R22/R27 = 100 Ω, C14/C6 = 1 nF, R30/R31 = 1.2 kΩ, C3/C5 = 0.22 µF. The measured 3 dB BW at gain = 1 below PGIA is about 16 kHz.

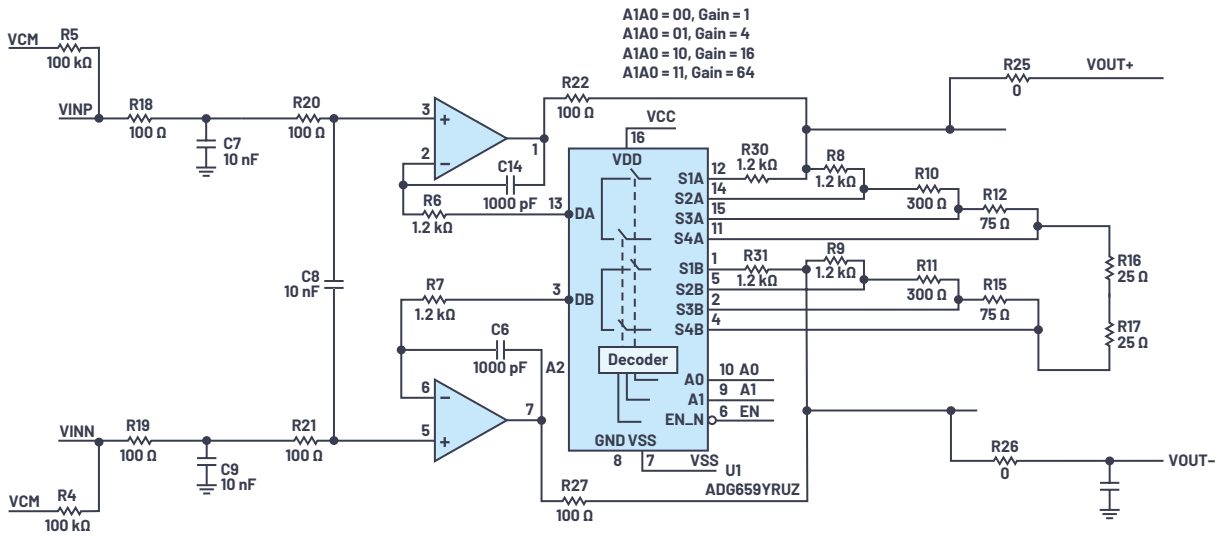

Figure 8. A PGIA to drive the LTC2500-32.

Bench Evaluation Setup

To test the noise, THD, and CMRR performance, a discrete ADA4084-2 PGIA and AD7768-1 board were made as a total solution. This solution is compatible with the EVAL-AD7768-1 evaluation board, so it can interface with the control board SDP-H1. Thus, the EVAL-AD7768FMCZ software GUI can be used to gather and analyze data.

The ADA4084-2 PGIA and LTC2500-32 board is designed as an alternative total solution. The board interfaces to the SDP-H1 controller board, which is controlled by the LTC2500-32FMCZ software GUI.

In both boards, the PGIA's gain is designed as 1/2/4/8/16, which is different from what's shown in Figure 8. Table 5 shows the evaluation results for these two boards.

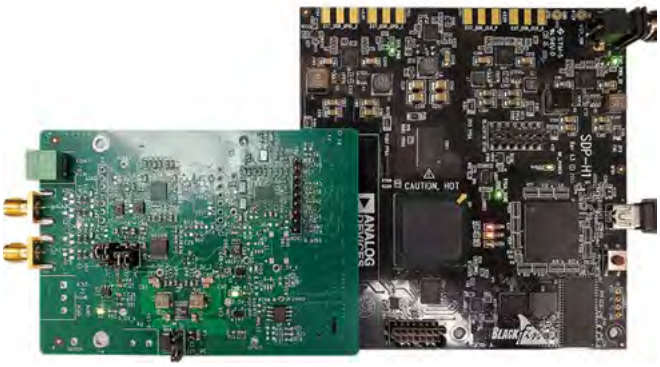

Figure 9. ADA4084-2 PGIA and AD7768-1 evaluation board solution.

Table 5. Signal Chain Solution Test Results

	ADA4084-2 and AD7768-1 (Median Mode, FMOD = 4 MHz, ODR = 16 kSPS)+	ADA4084-2 and AD7768-1 (Median Mode, FMOD = 4 MHz, ODR = 16 kSPS)+ MCU FIR and DEC to ODR = 16 k/16 = 1 kSPS	ADA4084-2 and LTC2500-32 ADC MCLK = 1 MHz
RTI Noise at Gain = 1 (μV rms)	3.718	0.868	0.82
RTI Noise at Gain = 2 (μV rms)	1.996	0.464	0.42
RTI Noise at Gain = 4 (μV rms)	1.217	0.286	0.3
RTI Noise at Gain = 8 (μV rms)	0.909	0.208	0.24
RTI Noise at Gain = 16 (μV rms)	0.808	0.186	0.19
THD at Gain = 1 (dB)	–125	–125	–122
THD at Gain = 2 (dB)	–125	–125	–119
THD at Gain = 4 (dB)	–124	–124	–118
THD at Gain = 8 (dB)	–120	–120	–117
THD at Gain = 16 (dB)	–115	–115	–115
CMRR at Gain = 1 (dB)	131	131	114
CMRR at Gain = 4 (dB)	117	117	121
CMRR at Gain = 16 (dB)	120	120	126
Pd Typical (mW)	31.3	31.3	33.2

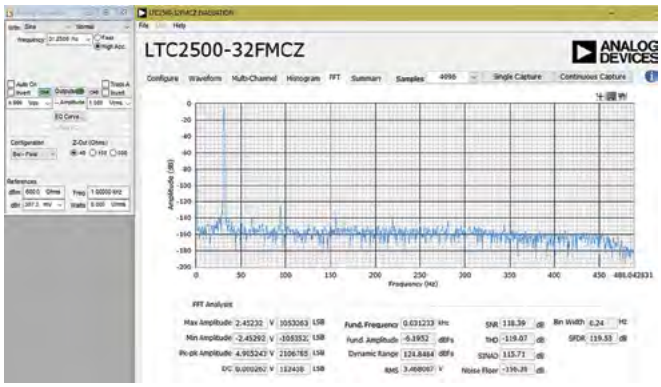

Figure 10. ADA4084-2 PGIA and LTC2500-32 board FFT for gain 1.

Conclusion

To design a very low noise and low power DAQ solution for seismology and energy exploration, a discrete PGIA can be designed with low noise and THD precision amplifiers to drive a high resolution precision ADC. This solution is flexible to balance the noise, THD, and ODR against its power consumption requirements.

- Benefits from LTC2500-32's low noise performance, as well as the ADA4084-2 and LTC2500-32, show the best noise performance without an MCU's further filtering processing.
- Both the ADA4522-2 and ADA4084-2 have good noise performance at PGIA gain = 1. The noise performance is about 0.8 µV rms.
- ADA4084-2 has better noise performance at high gain. At gain = 16, ADA4084-2 and LTC2500-32's noise is 0.19 µV rms, which is better than the 0.25 µV rms of the ADA4522-2.
- For the AD7768-1, with MCU's filtering, the ADA4084-2 and AD7768-1 solution shows noise performance similar to the ADA4084-2 and LTC2500-32 solution.

This article gives a solution to data acquisition that requires both low noise and low power with limited bandwidth. There are other DAQ applications that require different performance. If low power consumption is not a must, then the following operational amplifiers can be used to build the PGIA:

- Lowest noise: the LT1124 and LT1128 can be considered to have the best noise performance.
- Lowest drift: the ADA4523, a new zero-drift amplifier, has better noise specifications than the ADA4522-2 and LTC2500-32.
- Lowest bias current: the ADA4625-1 is recommended if the sensor's output resistance is high.
- Higher BW: The ADA4807, LTC6226, and LTC6228 are good solutions when building high BW, low noise PGIAs in high BW DAQ applications.

In DAQ applications where noise and power are not important but a small PCB area and high integrity are required, ADI's new integrated PGIAs, ADA4254 and LTC6373, are also good choices. ADA4254 is a zero-drift, high voltage, 1/16 to ~176 gain robust PGIA, and LTC6373 is a 25 pA I_{BIAS}, 36 V, 0.25 to ~16 gain, low THD PGIA.

Table 6. Precision Op Amp Selection Table

Part Number	V_{OS} (max) (µV)	I_{BIAS} (max)	GBP (typ) (MHz)	0.1 Hz to 10 Hz V_{NOISE} (typ) (nV p-p)	V_{NOISE} Density (typ)	Current Noise Density (typ)	I_Q/Amp (typ)	V_S Span (min) (V)	V_S Span (max) (V)
ADA4522-2	5	150 pA	2.7	117	5.8 nV/√Hz	800 fA/√Hz	830 µA	4.5	55
ADA4084-2	100	250 nA	15.9	100	3.9 nV/√Hz	550 fA/√Hz	625 µA	3	30
ADA4625-1	80	75 pA	18	150	3.3 nV/√Hz	4.5 fA/√Hz	4 mA	5	36
LT1124	70	20 nA	12.5	70	2.7 nV/√Hz	300 fA/√Hz	2.3 mA	8	44
LT6233	500	3 µA	60	220	1.9 nV/√Hz	430 fA/√Hz	1.15 mA	3	12.6
ADA4084-1	100	250 nA	15.9	100	3.9 nV/√Hz	550 fA/√Hz	565 µA	3	30
ADA4807-1	125	1.6 µA	200	160	3.3 nV/√Hz	700 fA/√Hz	1 mA	2.7	11
ADA4523-1	5	300 pA	5	88	4.2 nV/√Hz	1 pA/√Hz	4.5 mA	4.5	36
LT1128	40	90 nA	20	35	850 pV/√Hz	1 pA/√Hz	7.4 mA	8	44
LTC6228	95	25 µA	890	940	880 pV/√Hz	3 pA/√Hz	16 mA	2.8	11.75
LTC6226	95	20 µA	420	770	1 nV/√Hz	2.4 pA/√Hz	5.5 mA	2.8	11.75

References

[1] Geophones. ScienceDirect.

[2] Jesse Santos, Angelo Nikko Catapang, and Erbe D. Reyta. "Understanding the Fundamentals of Earthquake Signal Sensing Networks." *Analog Dialogue*, Vol. 53, No. 4, December 2019.

[3] Kristina Fortunado. "Programmable Gain Instrumentation Amplifiers: Finding One that Works for You." *Analog Dialogue*, Vol. 52, No. 4, December 2018.

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How to Select and Design the Best RTD Temperature Sensing System

Jellenie Rodriguez, Applications Engineer and
Mary McCarthy, Applications Engineer

Introduction

This article discusses the history and design challenges for designing a resistance temperature detector (RTD)-based temperature measurement system. It also covers RTD selection and configuration trade-offs. Finally, it details RTD system optimization and evaluation.

Why Is RTD Temperature Measurement Important?

Temperature measurement plays an important role in many different end applications such as industrial automation, instrumentation, CbM, and medical equipment. Whether monitoring environmental conditions or correcting system drift performance, high accuracy and precision are very important. There are several types of temperature sensors that can be used such as thermocouples, resistance temperature detectors (RTDs), electronic band gap sensors, and thermistors. The temperature sensor selected along with the design depends on the temperature range being measured and the accuracy required. For temperatures in the range of -200°C to +850°C, RTDs provide an excellent combination of high accuracy and good stability.

What Are the Main Temperature Measurement Challenges?

Challenges include

- Current and voltage selection. An RTD sensor is a passive device and does not produce an electrical output on its own. Excitation current or voltage is used to measure the resistance of the sensor by passing a small electrical current through the sensor to generate a voltage. How do I select the current/voltage?
- Is a 2-wire, 3-wire, or 4-wire the best choice for my design?
- How should the RTD signal be conditioned?
- How do I adjust the above variables so that the converter or other building blocks are used within their specification?
- Connecting multiple RTDs in a system—how are the sensors connected? Can some blocks be shared among the different sensors? And what is the impact to the overall system performance?
- What is the expected error for my design?

RTD Selection Guide

RTD Overview

For an RTD, the resistance of the sensor varies as a function of temperature in a precisely defined manner. The most widely used RTDs are platinum Pt100 and Pt1000, which are available in 2-wire, 3-wire, and 4-wire configurations. Other RTD types are made from nickel and copper.

Table 1. Common RTD Types

RTD Type	Materials	Range
Pt100, Pt1000	Platinum (numeric is resistance at 0°C)	-200°C to +850°C
Pt200, Pt500	Platinum (numeric is resistance at 0°C)	-200°C to +850°C
Cu10, Cu100	Copper (numeric is resistance at 0°C)	-100°C to +260°C
Ni120	Nickel (numeric is resistance at 0°C)	-80°C to +260°C

The most common Pt100 RTDs can take two different shapes: wire wound and thin film. Each type is built to several standardized curves and tolerances. The most common standardized curve is the DIN curve. DIN stands for "Deutsches Institut für Normung," which means "German institute for standardization." The curve defines the resistance vs. temperature characteristics of a platinum 100 Ω sensor, the standardized tolerances, and the operating temperature range. This defines the accuracy of the RTD starting with a base resistance of 100 Ω at a temperature of 0°C. There are different standard tolerance classes for DIN RTDs. These tolerances are shown in Table 2, and they also apply to Pt1000 RTDs that are useful in low power applications.

Table 2. RTD Accuracy—Class A, Class B, 1/3 DIN

Sensor Type	DIN Class	Tolerance @ 0°C	Tolerance @ 50°C	Tolerance @ 100°C
Pt100 RTD Thin Film	Class B	±0.30°C	±0.55°C	±0.80°C
Pt100 RTD Thin Film	Class A	±0.15°C	±0.25°C	±0.35°C
Pt100 RTD Wire Wound/ Thin Film	1/3 Class B	±0.1°C	±0.18°C	±0.27°C

Both the RTD itself and its accuracy must be considered when selecting the RTD sensor. The temperature range varies with element type, and the accuracy denoted at calibration temperature (usually at 0°C) varies with temperature. Thus, it is important to define the temperature range being measured and take into consideration that any temperature below or above the calibration temperature will have a wider tolerance and lower accuracy.

RTDs are categorized by their nominal resistance at 0°C. A Pt100 sensor has a temperature coefficient of approximately 0.385 Ω/°C and a Pt1000 has a temperature coefficient that is a factor of 10 greater than the Pt100. Many system designers use these coefficients to get an approximate resistance to temperature translation, but the Callendar-Van Dusen equations provide a more accurate translation.

The equation for temperature t ≤ 0°C is

$$R_{RTD}(t) = R_0[1 + At + Bt^2 + C(t - 100°C)t^3] \quad (1)$$

The equation for temperature t ≥ 0°C is

$$R_{RTD}(t) = R_0(1 + At + Bt^2) \quad (2)$$

where:

t is the RTD temperature (°C)
$R_{RTD}(t)$ is the RTD resistance at temperature (t)
R_0 is the RTD resistance at 0°C (in this case, R_0 = 100 Ω)
$A = 3.9083 \times 10^{-3}$
$B = -5.775 \times 10^{-7}$
$C = -4.183 \times 10^{-12}$

RTD Wiring Configurations

Another sensor parameter that needs to be considered when selecting an RTD is its wiring configuration, which will affect system accuracy. There are three different RTD wiring configurations available in the market wherein each configuration has advantages and disadvantages over one another and may require different techniques to reduce the measurement error.

A 2-wire configuration is the simplest but the least accurate configuration due to errors in lead-wire resistance and its variation with temperature contributing a significant measurement error. Thus, this configuration is only useful in applications where lead wires are short or when using a high resistance sensor (for example, Pt1000), both of which minimize lead resistance effects on the accuracy.

3-wire is the most used configuration because of the advantage of using three pins, which are useful in designs where the connector size is minimized (three connection terminals required vs. the 4-wire terminal for a 4-wire RTD). 3-wire also has significant accuracy improvement over the 2-wire configuration. The lead-wire resistance error in 3-wire can be compensated using different calibration techniques that will be later covered in this article.

4-wire is the most expensive but the most accurate configuration. In this configuration, the errors due to lead-wire resistance, along with temperature variation effects, are removed. Therefore, a 4-wire configuration results in the best performance.

RTD Configuration Circuit

A high precision and accurate RTD sensor measurement requires precise signal conditioning, analog-to-digital conversion, linearization, and calibration. The typical design of an RTD measurement system consists of the different stages as shown in Figure 2. Although the signal chain looks simple and straightforward, there are several complex factors involved and designers must consider complex component selection, connection diagram, error analysis, and other analog signal conditioning challenges that impact overall system board size and the cost of the bill of materials (BOM) due to the higher number of contributing blocks. On the brighter side, there are plenty of integrated solutions available in ADI's portfolio. This complete system solution helps designers to simplify their designs while reducing the board size, time to market, and the cost of the overall RTD measurement system.

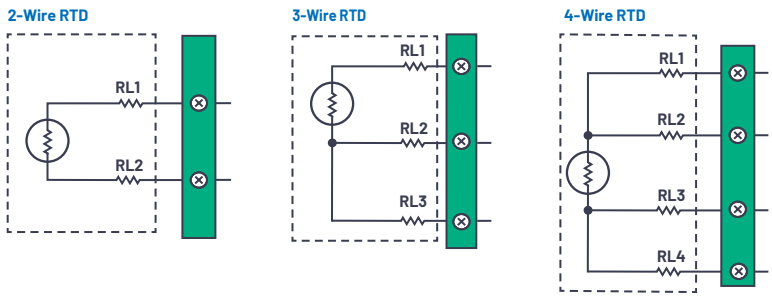

Figure 1. RTD wiring configurations.

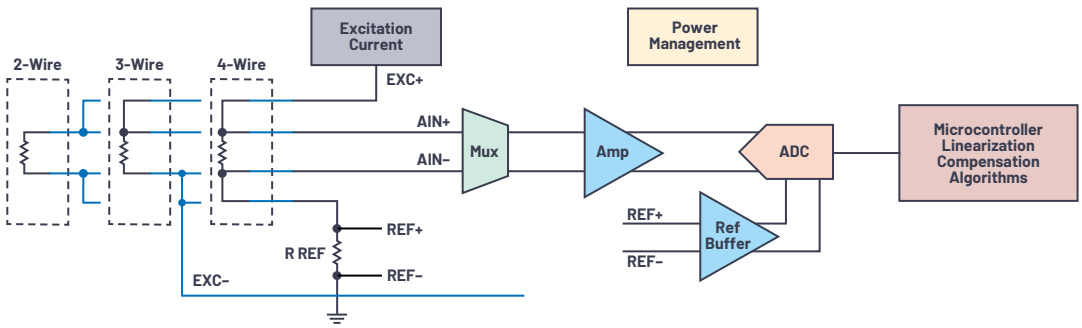

Figure 2. Typical RTD measurement signal chain block.

The three RTD wiring configurations have different wiring techniques needed to interface or connect an RTD to an ADC, along with the other external components, and requirements from the ADC, such as excitation current and a flexible mux. This section covers a deeper understanding and focus on each RTD configuration circuit design and considerations.

Sigma-Delta ADCs

Sigma-delta (Σ-Δ) ADCs offer multiple benefits when designing RTD systems. Firstly, as sigma-delta ADCs oversample the analog input, external filtering is minimized, with a simple RC filter being the only requirement. They offer flexibility in terms of choice of filter type and choice of output data rate. The inbuilt digital filtering can be used to reject any interference from the mains power supply in mains operated designs. 24-bit, high resolution ADCs such as the AD7124-4/AD7124-8 have a peak-to-peak resolution of 21.7 bits maximum. Other benefits are

- Wide common-mode range for the analog inputs
- Wide common-mode range for the reference inputs
- Ability to support ratiometric configurations
- Buffered reference and analog inputs

Some sigma-delta ADCs are highly integrated and include

- A programmable gain amplifier (PGA)
- Excitation currents
- Reference/analog input buffers
- Calibration functions

They simplify the RTD design significantly along with reducing the BOM, system cost, board space, and time to market.

For this article, the AD7124-4/AD7124-8 are used as the ADC. These are low noise, low current precision ADCs with an integrated PGA, excitation currents, analog input, and reference buffers.

Ratiometric Measurement

A ratiometric configuration is a suitable and cost-effective solution for systems that use resistive sensors such as RTDs or thermistors. With a ratiometric approach, the reference and sensor voltages are derived from the same excitation source. Therefore, the excitation source does not need to be accurate. Figure 3 shows an example of a ratiometric configuration in a 4-wire RTD application. A constant excitation current supplies the RTD and a precision resistor, R_{REF}, with the voltage generated across R_{REF} being the reference voltage for the RTD measurement. Any variation of the excitation current does not affect the accuracy of the measurement. Therefore, using a ratiometric approach allows a noisier, less stable excitation current to be used. An excitation current is preferred over voltage excitation due to its better noise immunity. The major factors to consider when selecting an excitation source value are discussed later in this article.

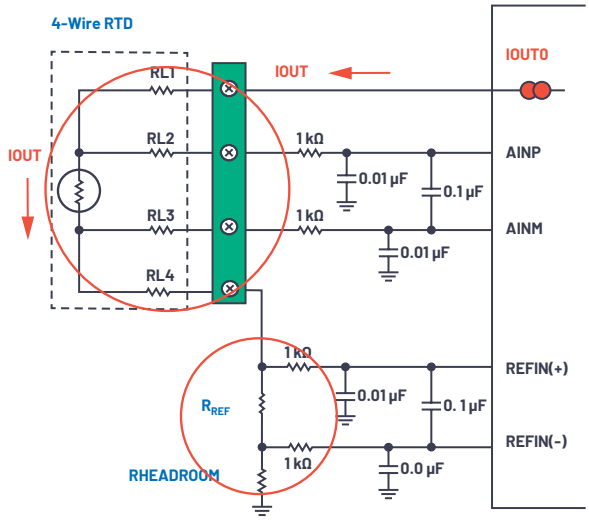

Figure 3. 4-wire RTD ratiometric measurement.

Shared IOUT/AIN Pin

Many RTD system designers use sigma-delta ADCs with integrated mux and excitation currents that allow multiple channel measurements and flexible routing of the excitation currents to each sensor. An ADC such as the AD7124 allows a single pin to operate simultaneously as an excitation current and an analog input pin (see Figure 4). Sharing pins between IOUT and AIN will only require two pins per 3-wire RTD sensor, which increases the channel count. However, in this configuration, a large value of the resistor R in the antialiasing or electromagnetic interference (EMI) filtering can add errors to the RTD resistance value as R is in series with the RTD—thus, limited R values can be used. That's why it is usually recommended to have a dedicated pin for each excitation current source to avoid possible errors across RTD measurements.

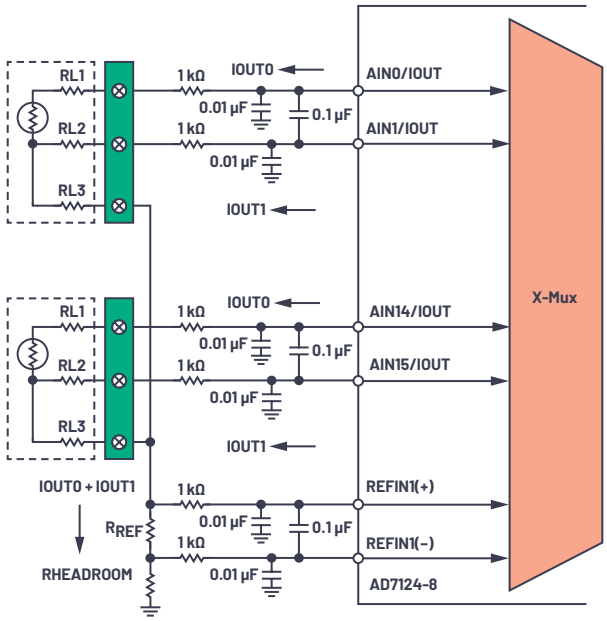

Figure 4. 3-wire RTD with a shared IOUT/AIN pin.

4-Wire RTD Connection Diagram

A 4-wire RTD configuration offers the best performance. The only issue that system designers face is the cost of the sensor itself and the size of the 4-pin connector compared to the other two configurations. In this configuration, the errors due to the lead wires are inherently removed by the return wires. A 4-wire configuration uses Kelvin sensing with two wires to carry the excitation current to and from the RTD, while the remaining two wires sense the current across the RTD element itself. Errors due to lead resistance are inherently removed. A 4-wire configuration only requires one excitation current IOUT, as shown in Figure 5. Three analog pins from the ADC are used to implement a single 4-wire RTD configuration: one pin for excitation current, IOUT, and two pins as a fully differential input channel (AINP and AINM) used for sensing the voltage across the RTD.

When the design uses multiple 4-wire RTDs, a single excitation current source can be used with the excitation current being directed to the different RTDs in the system. By placing the reference resistor on the low side of the RTD, a single reference resistor can support all the RTD measurements; that is, the reference resistor is shared by all RTDs. Note that the reference resistor can be placed on the high side or low side if the ADC's reference input has wide common-mode range. So, for a single 4-wire RTD, either the reference resistor on the high side or low side can be used. However, when using multiple 4-wire RTDs in a system, placing the reference resistor on the low side is advantageous as one reference resistor can be shared by all RTDs. Note that some ADCs include reference buffers. These buffers may require some headroom, so a headroom resistor is then required if the buffer is enabled. Enabling the buffer means that more robust filtering can be connected to the reference pins without causing errors such as gain errors within the ADC.

2-Wire RTD Connection Diagram

The 2-wire RTD configuration is the simplest configuration and is shown in Figure 6. For the 2-wire configuration, only one excitation current source is required. Thus, three analog pins from the ADC are used to implement a single 2-wire RTD configuration: one pin for excitation current, IOUT, and two pins as a fully differential input channel (AINP and AINM) used for sensing the voltage across the RTD. When the design uses multiple 2-wire RTDs, a single excitation current source can be used with the excitation current being directed to the different RTDs in the system. By placing the reference resistor in the low side of the RTD as per the 4-wire configuration, a single reference resistor can support all the RTD measurements; that is, the reference resistor is shared by all RTDs.

The 2-wire configuration is the least accurate of the three different wiring configurations since the actual resistance at the point of measurement includes both the resistances of the sensor and the lead wires RL1 and RL2, thus increasing the voltage measurement across the ADC. If the sensor is remote and the system uses a very long wire, then the errors will be significant. For example, a 25-foot length of a 24 AWG copper wire will have an equivalent resistance of 0.026 Ω/foot (0.08 Ω/meter) × 2 × 25 foot is to 1.3 Ω. Therefore, 1.3 Ω wire resistance produces an error of (1.3/0.385) = 3.38°C (approximately) due to wire resistance. The wire resistance also changes with temperature, which adds additional error.

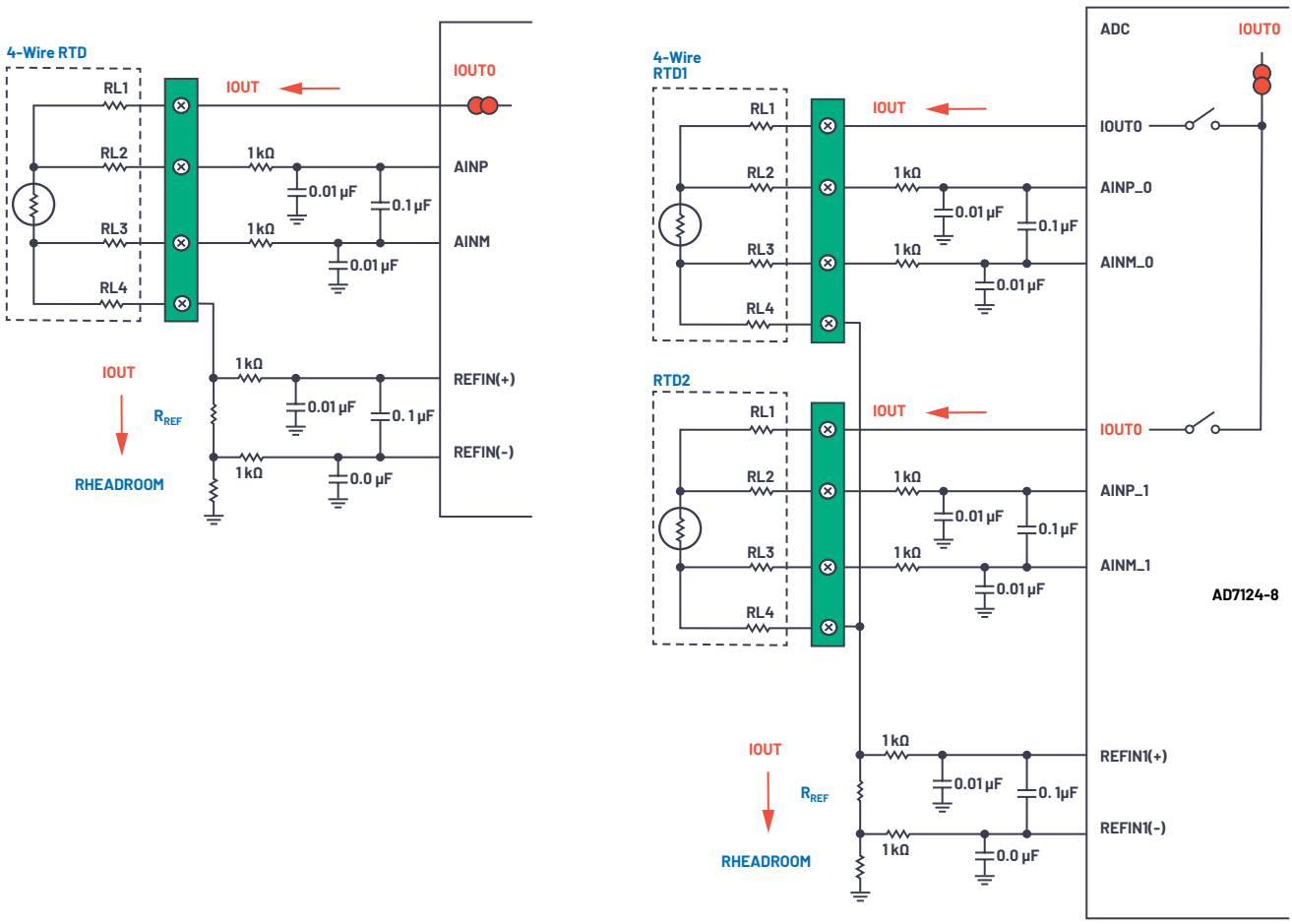

Figure 5. Single and multiple 4-wire RTD analog input configuration measurements.

3-Wire RTD Connection Diagram

The significant error due to lead-wire resistances of the 2-wire RTD configuration can be significantly improved by using a 3-wire RTD configuration. In this article, we use a second excitation current (shown in Figure 7) to cancel the lead-wire resistance errors produced by RL1 and RL2. Thus, four analog pins from the ADC are used to implement a single 3-wire RTD configuration: two pins for excitation currents (IOUT0 and IOUT1) and two pins as a fully differential input channel (AINP and AINM) used for sensing the voltage across the RTD.

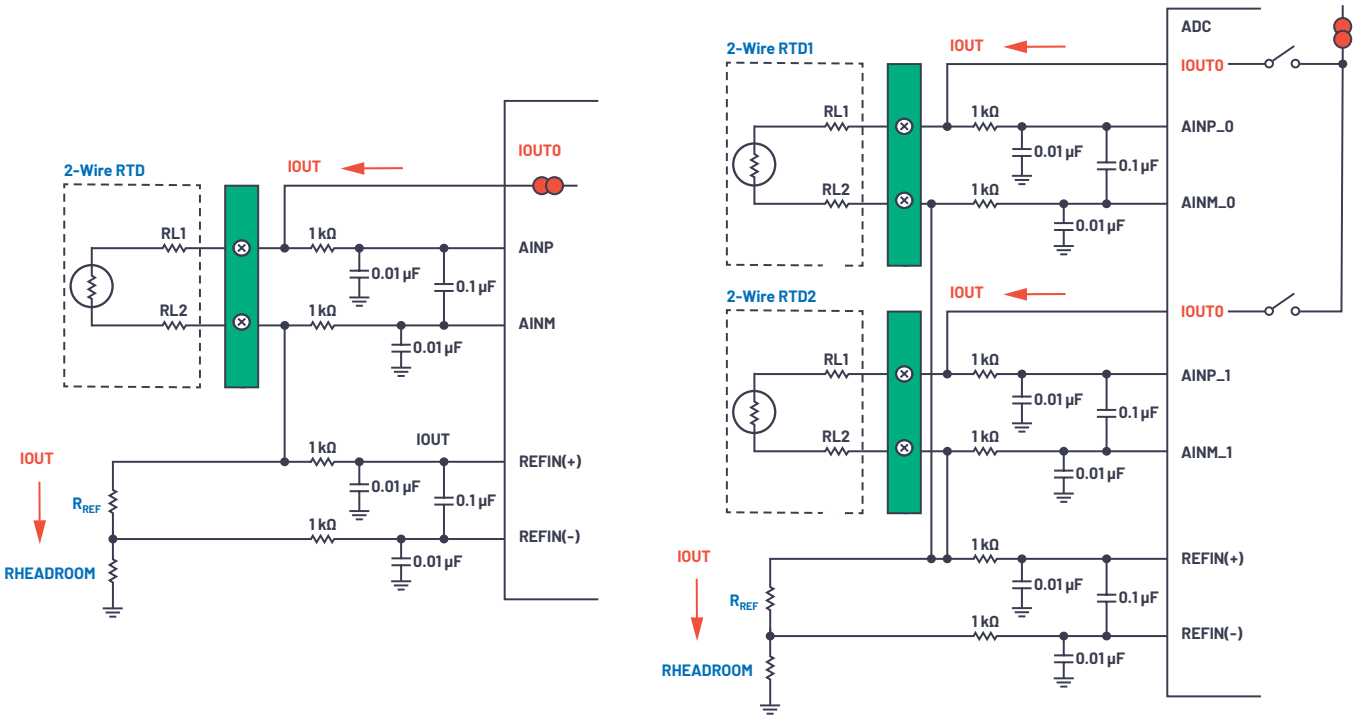

Figure 6. Single and multiple 2-wire RTD analog input configuration measurement.

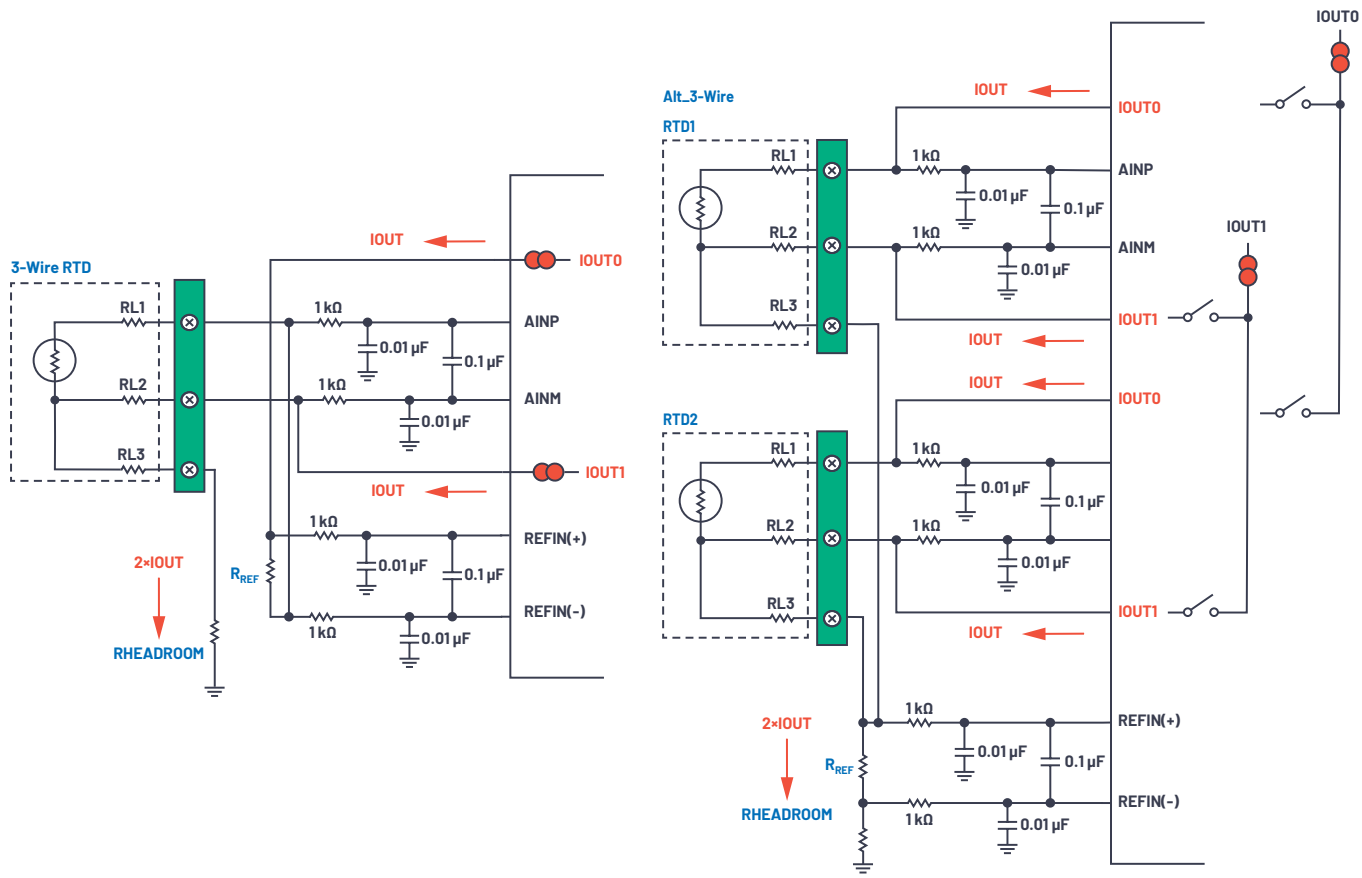

Figure 7. Single and multiple 3-wire RTD analog input configuration measurement.

There are two ways to configure a 3-wire RTD circuit. Method 1 places the reference resistor on the top side so the first excitation current IOUT0 flows to R_{REF}, RL1 then to RTD, and the second current flows through the RL2 lead resistance and develops a voltage that cancels the voltage dropped across the RL1 lead resistance. So, well matched excitation currents null the error due to the lead resistance completely. If the excitation currents have some mismatch, the impact of the mismatch is minimized using this configuration. The same current flows to the RTD and R_{REF}; thus, any mismatch between the two IOUTs affects the lead resistance calculation only. This configuration is useful when measuring a single RTD.

When measuring multiple 3-wire RTDs, a reference resistor on the bottom side is recommended (Method 2) so only a single reference resistor can be used, which minimizes the overall cost. However, in this configuration, one current flows through the RTD while both currents flow through the reference resistor. So, any mismatch in IOUT can affect the value of the reference voltage along with the lead resistance cancellation. When excitation current mismatch is present, this configuration will have greater error than Method 1. There are two possible ways to calibrate the mismatch and mismatch drift between IOUT, hence improving the accuracy of the second configuration. First is calibrating by chopping (swapping) the excitation currents, performing a measurement on each phase, and then averaging the two measurements. Another solution is to measure the actual excitation currents themselves and then use the calculated mismatch to compensate for the mismatch in the microcontroller. More details regarding these calibrations are discussed in CN-0383.

RTD System Optimization

Looking at system designer issues, there are different challenges involved in designing and optimizing RTD application solutions. Challenge one is the sensor selection and connection diagram that were discussed in the previous sections. Challenge two is the measurement configuration, which includes the ADC configuration, setting the excitation current, setting the gain, and selecting the external components while ensuring system optimization and operating within the ADC specification. And lastly, the most critical issue is how to achieve the target performance and what are the error sources that contribute to the overall system error.

Luckily, there is a new RTD_Configurator_and_Error_Budget_Calculator that offers a hands-on solution in designing and optimizing RTD measurement systems from concept to prototyping.

The tool

- Enables the understanding of the correct configuration, wiring, and circuit diagram
- Assists in the understanding of the different error sources and allows design optimization

The tool is designed around the AD7124-4/AD7124-8. It allows the customer to adjust settings such as excitation current, gain, and external components. It indicates out-of-bound conditions to ensure that the final solution is within the specifications of the ADC.

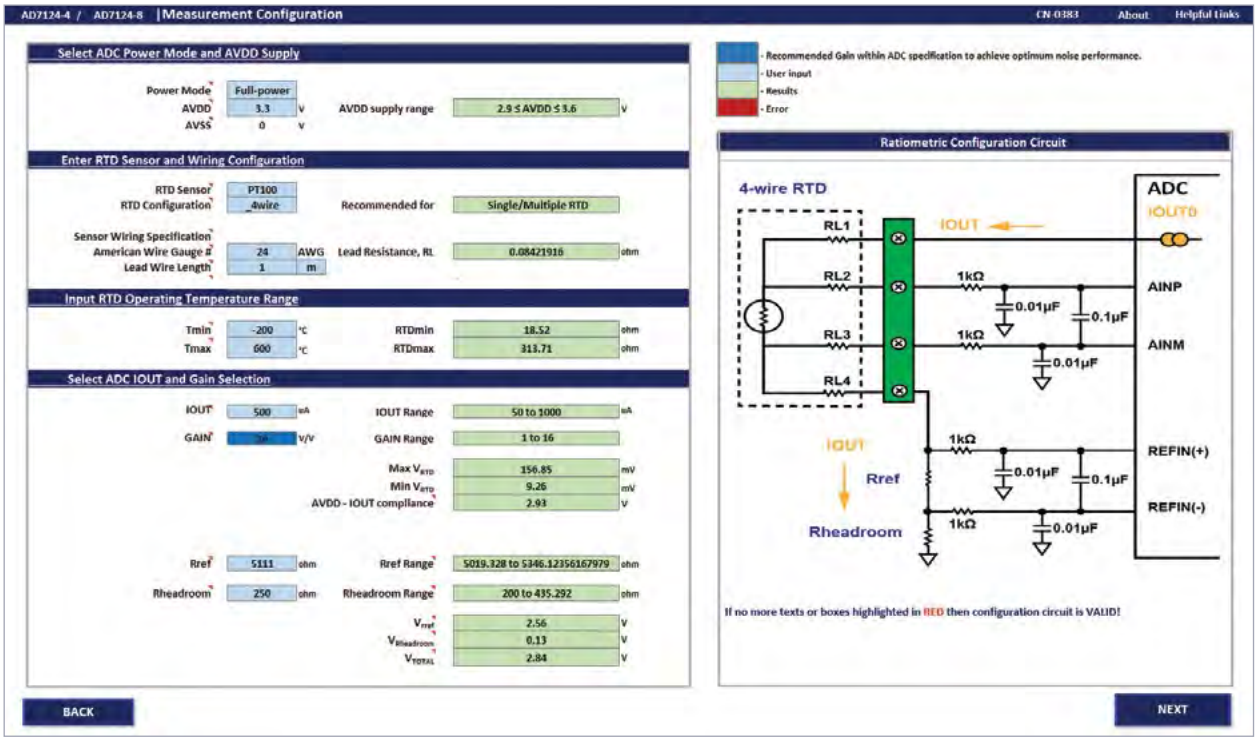

Figure 8. RTD configurator.

Selection of Excitation Current, Gain, and External Components

Ideally, we tend to select higher magnitudes of excitation current to generate a much higher output voltage and maximize the ADC input range. However, since the sensor is resistive, the designer must also ensure the power dissipation or self-heating effects of a large value of excitation current will not affect the measurement results. A system designer may select a high excitation current. However, to minimize self-heating, the excitation current needs to be turned off between measurements. The designer needs to consider the timing implications for the system. An alternative approach is to select a lower excitation current that minimizes self-heating. Timing is now minimized, but the designer needs to determine if system performance is affected. All scenarios can be tested via the RTD_Configurator_and_Error_Budget_Calculator. The tool allows the user to balance the selection of excitation current, gain, and external components to ensure that the analog input voltage is being optimized along with tuning the ADC gain and speed to give better resolution and better system performance, which means lower noise and lower offset error.

To understand the resulting filter profile or to get a deeper understanding of the timing of the conversions, the VirtualEval online tool provides this detail.

The ADC input and reference inputs of a sigma-delta ADC are both continuously sampled by a switched capacitor front end. For the RTD systems being discussed, the reference input is also driven by an external reference resistor. An external RC filter is recommended on the analog input of a sigma-delta ADC for antialiasing purposes. For EMC purposes, a system designer may use large R and C values both on the analog input and the reference input. Large RC values can cause gain errors in measurements as the front-end circuitry does not have sufficient time to settle between sampling instants. Buffering the analog and reference inputs prevents these gain errors and allows unlimited R and C values to be used.

For the AD7124-4/AD7124-8, when using an internal gain greater than 1, the analog input buffers are automatically enabled and since the PGA is placed in front of the input buffers, as the PGA is rail to rail, the analog input is also rail to rail. However, in the case of the reference buffers or when using the ADC at a gain of 1 with analog input buffers enabled, it is necessary to ensure that the headroom required for correct operation is met.

Signals from Pt100s are low level. They are in the order of hundreds of mV. For optimum performance, an ADC with wide dynamic range can be used. Alternatively, a gain stage can be used to amplify the signal before it is applied to the ADC. The AD7124-4/AD7124-8 support gains from 1 to 128, thus allowing an optimized design for a wide range of excitation currents. The multiple allowed options of PGA gain allow the designer to trade off excitation current value vs. gain, external components, and performance. The RTD configurator tool indicates whether the new excitation current values can be used with the selected RTD sensor. Suitable values for the precision reference resistor and the reference headroom resistor are also suggested. Note that the tool ensures the ADC is used within specification—it displays possible gains that will support the configuration. The AD7124 excitation currents have an output compliance; that is, the voltage on the pin providing the excitation current needs some headroom from AVDD. The tool will also ensure that this compliance specification is met.

The RTD tool allows the system designer to guarantee a system that is within the operating limits of the ADC and the RTD sensor. The accuracy of the external components such as the reference resistor and its contribution to the system error will be discussed later.

Filtering Options (Analog and Digital 50 Hz/60 Hz Rejection)

As discussed earlier, an antialiasing filter is recommended with sigma-delta converters. As the embedded filter is digital, the frequency response is reflected around the sampling frequency. Antialiasing filtering is required to adequately attenuate any interference at the modulator frequency and at any multiples of this frequency. Since sigma-delta converters oversample the analog input, the design of the antialiasing filter is greatly simplified and a simple single-pole RC filter is all that is required.

When the final system is used in the field, dealing with noise or interference from the environment in which the system is operating can be quite challenging, especially in application spaces such as industrial automation, instrumentation, process control, or power control, wherein being tolerant to noise and at the same time not being noisy to your neighboring components is required. Noise, transients, or other interference sources can impact the system accuracy and resolution. Interferences can also occur when systems are powered from the mains supply. Main power supply frequencies are generated at 50 Hz and its multiples in Europe, and 60 Hz and its multiples in the U.S. Thus, when designing an RTD system, a filtering circuit with 50 Hz/60 Hz rejection must be considered. Many system designers want to design a universal system that rejects both 50 Hz and 60 Hz simultaneously.

Most of the lower bandwidth ADCs, including AD7124-4/AD7124-8, offer a variety of digital filtering options that can be programmed to set notches at 50 Hz/60 Hz. The filter option selected has an effect on the output data rate, settling time, and the 50 Hz and 60 Hz rejection. When multiple channels are enabled, a settling time is required to generate a conversion every time the channel is switched; thus, selecting a filter type with longer settling time (that is, sinc4 or sinc3) will lower the overall throughput rate. In this case, a postfilter or FIR filter is useful to provide reasonable simultaneous 50 Hz/60 Hz rejection at lower settling times and thus increasing the throughput rate.

Power Consideration

The current consumption or power budget allocation of the system is highly dependent on the end application. The AD7124-4/AD7124-8 contain three power modes that allow trade-off between performance, speed, and power. For any portable or remote application, low power components and configurations must be used, and for some industrial automation applications, the complete system is powered from the 4 mA to 20 mA loop so that a current budget of only 4 mA maximum is allowed. For this type of application, the devices can be programmed in mid or low power mode. The speed is much lower, but the ADC still gives high performance. If the application is process control, which is powered from the mains supply, a much higher current consumption is allowed, so the device can be programmed in full power mode and this system can achieve a much higher output data rate and increased performance.

Error Sources and Calibration Options

After knowing the required system configuration, the next step is to estimate the errors associated with the ADC and the system errors. These help system designers to understand if the front end and ADC configuration will meet the overall target accuracy and performance. The RTD_Configurator_and_Error_Budget_Calculator allows the user to modify the system configuration for optimum performance. For example, Figure 9 shows a summary of all the errors. The system error pie chart indicates that the external reference resistor's initial accuracy and its temperature coefficient are the main error contributors to the overall system error. Thus, it is important to consider using an external reference resistor with higher accuracy and a better temperature coefficient.

The error due to the ADC is not the most significant error contributor to the overall system error. However, the error contribution from the ADC can be reduced further using the AD7124-4/AD7124-8's internal calibration modes. An internal calibration is recommended upon power-up or software initialization to remove the ADC gain and offset errors. Please note that these calibrations will not remove errors created by the external circuitry. However, the ADC can also support system calibrations so that the system offset and gain error can be minimized, but this may add additional cost and may not be required for most applications.

Fault Detection

For any harsh environment or for applications where safety is a priority, diagnostics are becoming part of the industry requirements. The embedded diagnostics in the AD7124-4/AD7124-8 reduce the need for external components to implement diagnostics, resulting in a smaller, simplified time and cost savings solution. Diagnostics include

- Checks of the voltage level on the analog pins to ensure it is within the specified operating range
- A cyclic redundancy check (CRC) on the serial peripheral interface (SPI) bus
- A CRC on the memory map
- Signal chain checks

These diagnostics lead to a more robust solution. The failure modes, effects, and diagnostic analysis (FMEDA) of a typical 3-wire RTD application have shown a safe failure fraction (SFF) greater than 90% according to IEC 61508.

RTD System Evaluation

Figure 10 shows some measured data from note CN-0383. This measured data was captured with the AD7124-4/AD7124-8 evaluation board, which includes demo modes for 2-, 3-, and 4-wire RTDs, and calculated the corresponding degree Celsius value. The results show that a 2-wire RTD implementation gives an error closer to the lower limit of the error boundary, while the 3-wire or 4-wire RTD implementation has an overall error that is well within the allowed limit. The higher error in the 2-wire measurement is due to the lead resistance errors described earlier.

Figure 9. RTD error sources calculator.

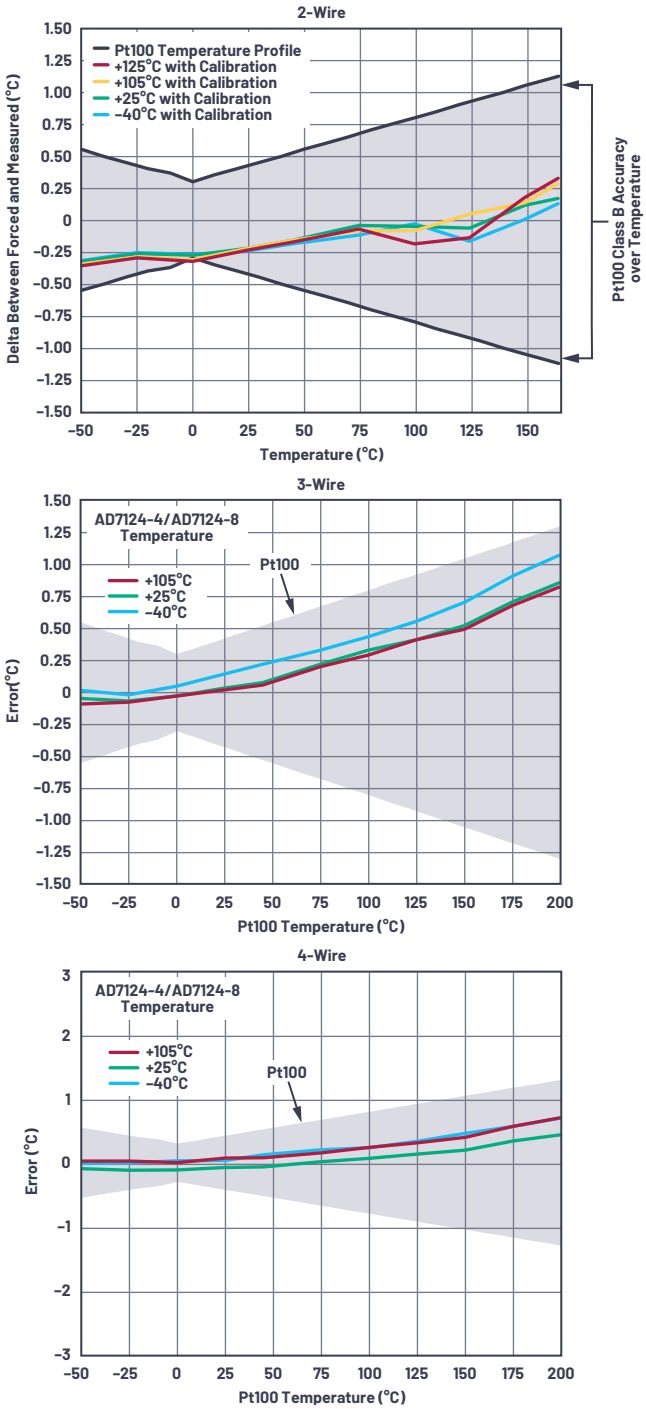

Figure 10. A 2-/3-/4-wire RTD temperature accuracy measurement postfilter in low power mode at 25 SPS.

What these examples show is that following the above RTD guidelines will lead to a high accuracy, high performance design when used in conjunction with ADI's lower bandwidth sigma-delta ADCs such as the AD7124-4/AD7124-8. The circuit note (CN-0383) will also serve as a reference design that helps the system designer get to prototyping quickly. The evaluation board allows the user to evaluate the system performance wherein each of the sample configuration demo modes can be used. Going forward, firmware for the different RTD configurations can be easily developed using ADI generated sample code available from the AD7124-4/AD7124-8 product pages.

ADCs, which use a sigma-delta architecture such as from the AD7124-4/AD7124-8, are suitable for RTD measurement applications since they address concerns such as 50 Hz/60 Hz rejection, as well as wide common-mode range on the analog and possibly the reference inputs. They are also highly integrated, containing all the functions needed for an RTD system design. In addition, they provide enhanced features such as calibration capability and embedded diagnostics. This level of integration, along with the complete system collateral or ecosystem will simplify the overall system design, cost, and design cycle from concept to prototyping.

To ease the system designers' journey, the RTD_Configurator_and_Error_Budget_Calculator tool along with the online tool VirtualEval, the evaluation board hardware and software, and CN-0383 can be used to address the different challenges, such as connectivity concerns and the overall error budget, and bring the users to the next level of their design.

Conclusion

This article has demonstrated designing an RTD temperature measurement system is a challenging, multistep process. It requires making choices in terms of the different sensor configurations, ADC selection, and optimizations and how those decisions impact overall system performance. The ADI RTD_Configurator_and_Error_Budget_Calculator tool, along with the online tool VirtualEval, the evaluation board hardware and software, and CN-0383 streamline the process by addressing connectivity and overall error budget concerns.

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Does the Assembly Orientation of an SMPS Inductor Affect Emissions?

Keith Szolusha, Applications Director,
Gengyao Li, Applications Engineer, and
Frank Wang, EMI Engineer

The spectrum of EMI emissions produced by switch-mode power supplies (SMPS) are a function of a number of parameters, including the size of the hot loop, switching speed (slew rate) and frequency, input and output filtering, shielding, layout, and grounding. One potential source of emissions is the switching node, referred to as SW on many schematics. The SW node copper can act as an antenna, transmitting the noise generated by fast and efficient high power switching events. This is the main source of emissions for most switching regulators.

The amount of top layer SW node copper certainly should be minimized to limit the antenna size. With a monolithic switching regulator (power switch within the IC), the SW node runs from the IC to the inductor with a short trace on the top layer. With a controller (power switch external to the switch controller IC) the SW node can be self-contained at the switches, away from the IC. SW node copper connects to one side of the inductor in buck and boost switcher topologies. Because of a number of performance parameters involved, layout of the Layer 1 SW node in the XY plane of the PCB, or on internal layers, is a bit of a black art (see Figure 1).

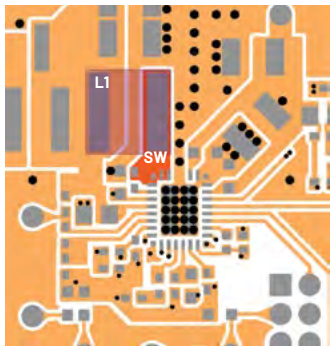

Figure 1. SW node highlight in XY plane of Layer 1 on DC3008A LT8386 low EMI LED driver.

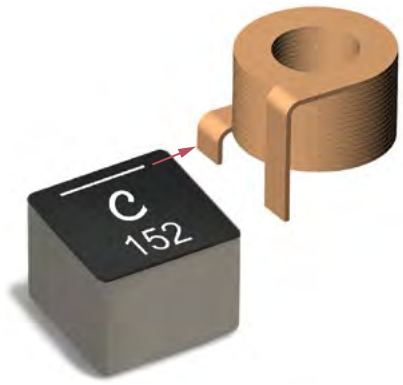

Figure 2. White stripe on the Coilcraft XAL inductor marks the short coil lead because coil leads are not visible. It indicates the direction of terminals and short lead. Connect high dv/dt here for lowest EMI.

Inductor Geometry

Of course, the SW node also extends vertically (in the Z plane) when the inductor terminals are considered. The vertical orientation of the inductor terminals can increase the antenna effect of the SW node and increase emissions. Furthermore, internal inductor windings may not be symmetrical. Even if an inductor's symmetrical terminals suggest a symmetrical construction hidden in the package, the polarity indicator on the top of the component tells a different story. Figure 2 shows the internal winding structure of Coilcraft's XAL inductor series. The flat wire winding starts at the bottom of the component and ends at the top, so one terminal ends up being much shorter than the other in the Z plane.

Furthermore, inductors with an exposed SW node on the side may perform worse than those with shielded vertical metal, as shown in Figure 3. A board designer could choose inductors with the least amount of vertical and exposed terminals to reduce EMI, but what about the orientation of the two inductor terminals and the relative effect on emissions?

Emissions Tell the Story

Low emissions performance of a board under test is a combination of IC emissions performance and layout considerations. Even with a low emissions monolithic IC, care must be taken regarding layout while also taking into account the assembly of the critical emissions components. To prove this point, we examined the orientation effects on the board of the main inductor, L1, of an LT8386 demonstration circuit (see Figure 4). In this case, the inductor manufacturer, Coilcraft, specifies the short terminal of XAL6060-series inductors with a white line on the top mark of the component. Standard CISPR 25 conducted emissions (CE) and radiated emissions (RE) tests in the EMI chamber show that the placement direction (see Figure 5) of this inductor critically affects performance.

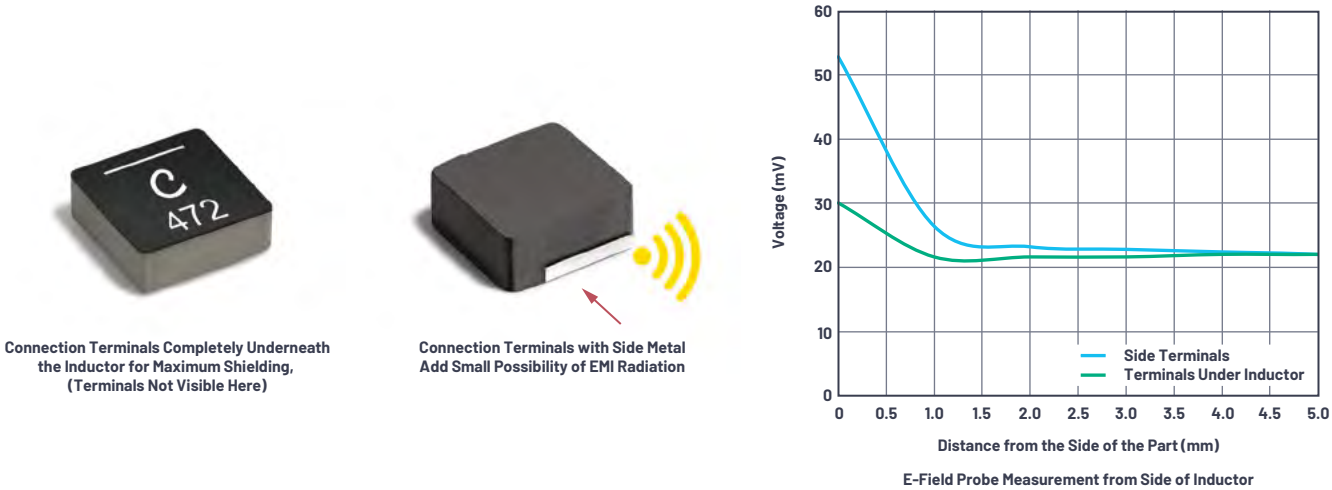

Figure 3. Pay attention to inductor terminal type on EMI-sensitive designs—not only to orientation.

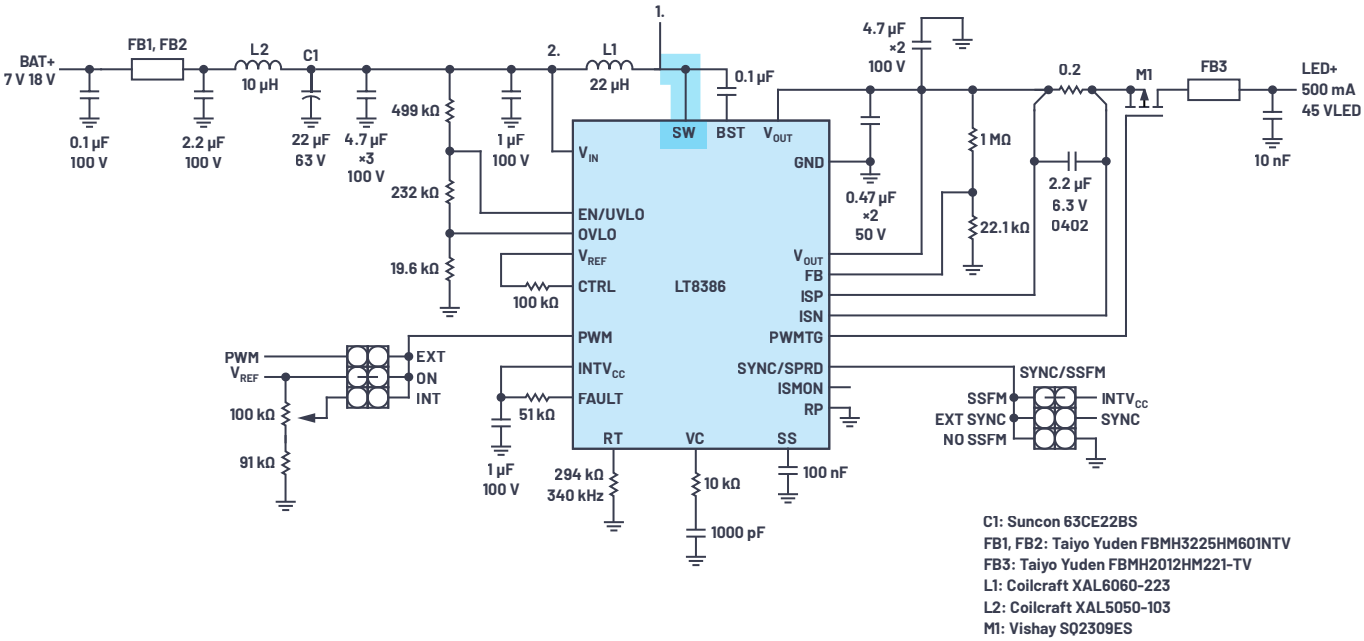

Figure 4. SW node highlighted in schematic view of DC3008A LT8386 low EMI LED driver. Place the short-side terminal at Orientation 1 and Orientation 2 to compare the complete emissions results.

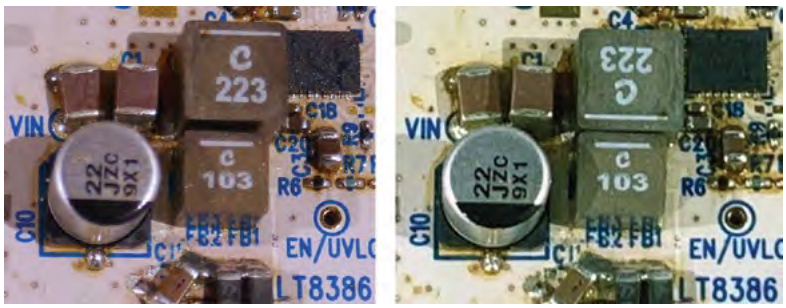

Figure 5. Coilcraft XAL6060-223MEB inductor orientation emissions testing with a DC3008A LT8386 LED driver. An L1 Orientation 1 (left) with short terminal on the SW node and L1 Orientation 2 (right) with long terminal on the SW node. Emissions results are shown in Figure 6 through Figure 8.

Figure 6, Figure 7, and Figure 8 show that the emissions performance of DC3008A is directly affected by the orientation of L1 on the demonstration circuit, with no other component changes. Specifically, low frequency RE (150 kHz to 150 MHz) and FM bands CE (70 MHz to 108 MHz) have lower EMI with Orientation 1—that is, the short-side terminal placed on the SW node. A 17 dBµV/m to 20 dBµV/m difference in the AM band cannot be ignored.

Not all inductors are created equally. The winding direction, the shape of the terminals, the shape of the terminal connections, and even the core material can vary. Strength of the H-field and the E-field with different core materials and construction differences might play a role in varying emissions amongst inductors. However, this case study reveals an area of concern, which can be used to our advantage.

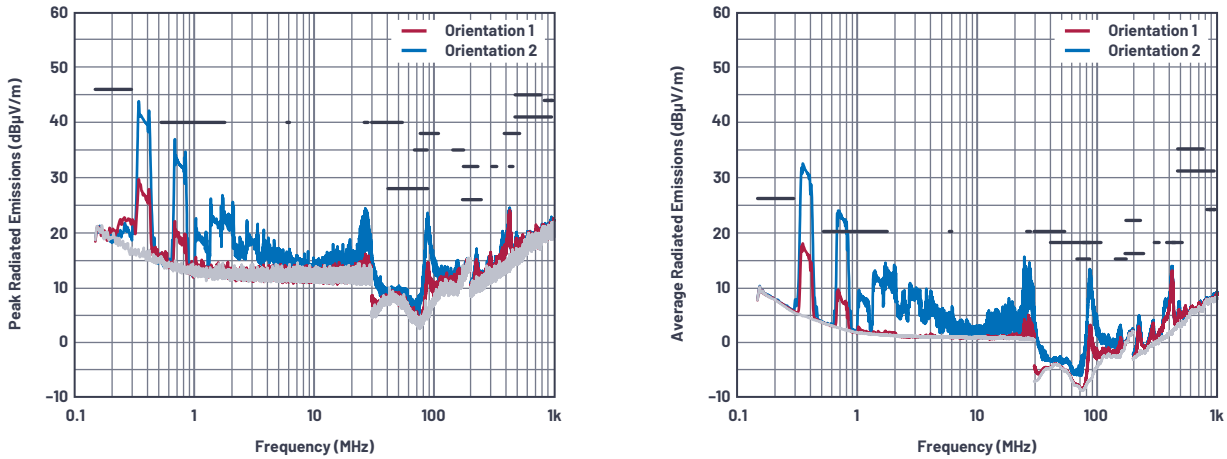

Figure 6. Radiated emissions show that the inductor orientation on DC3008A makes a significant impact on results. With the short-side terminal attached to the SW node for the smallest SW antenna (red), radiated emissions (RE) are drastically improved.

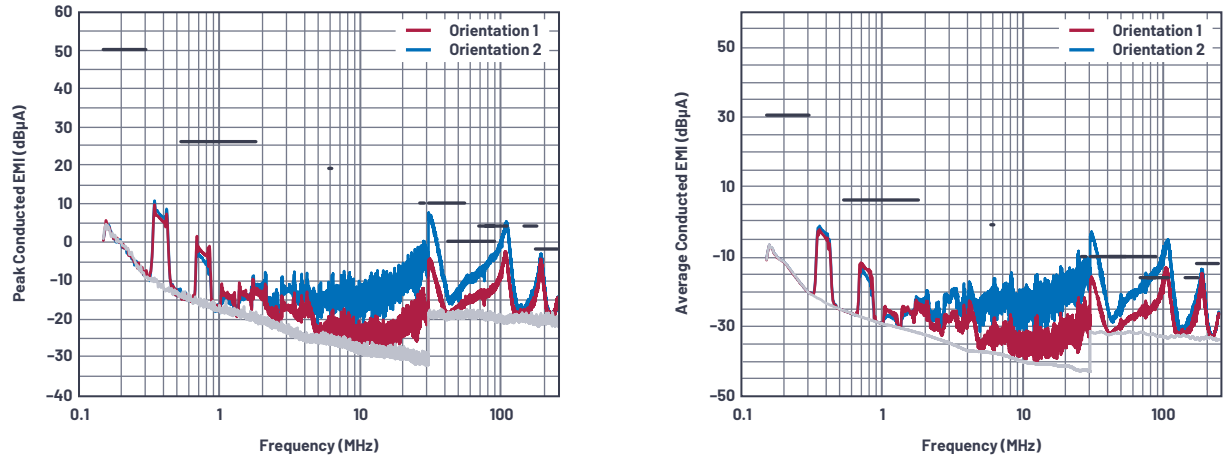

Figure 7. Current probe method conducted emissions (CE) show improvement (>3 MHz) with the short-side terminal of the inductor attached to the switch node vs. the alternative polarity.

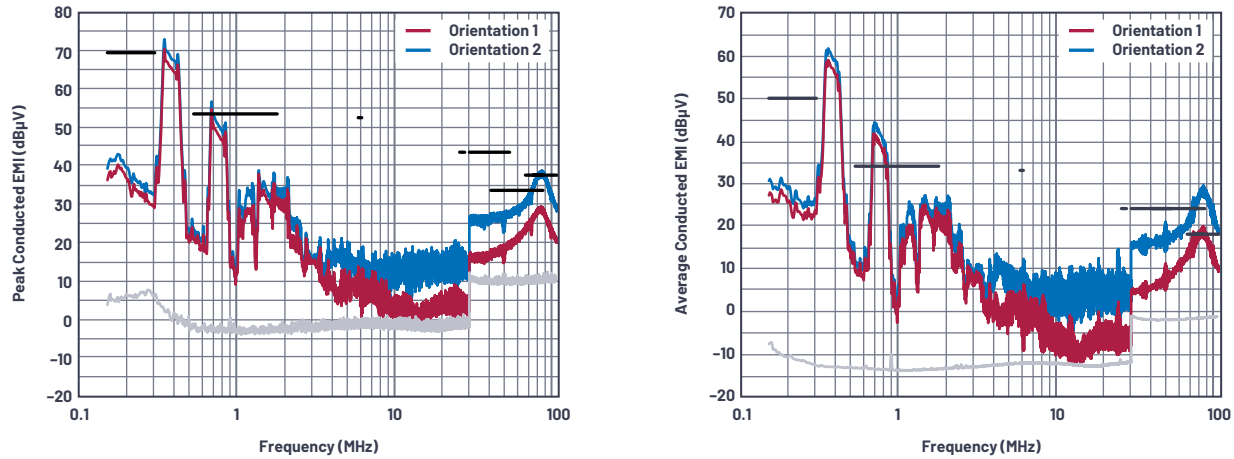

Figure 8. Voltage method conducted emissions (CE) show improvement above 3 MHz with the short-side terminal of the inductor attached to the switch node vs. the alternative polarity.

Inductors Without Polarization Indicator

Orientation is easily determined if the inductor manufacturer indicates a difference in internal terminal size with a top silkscreen mark or dot. If one of these inductors is chosen for a design, it is wise to indicate the mark on the silkscreen of the PCB, the assembly diagram, and even in the schematic. Unfortunately, some inductors have no polarization or short terminal indicator. The winding structure inside could be close to symmetrical, or there could be a known structural difference. There is no ill intent here—manufacturers may not be aware of this very particular assembly direction trade-off inherent in their product. Regardless, we suggest evaluating emissions in both orientations in a certified chamber of a selected inductor to ensure repeatable high performance measurements.

Sometimes there is no external mark, and assembly direction of the inductor is unavoidably arbitrary—yet the inductor is desirable for other parameters. For instance, Würth Elektronik's WE-MAPI metal alloy power inductors are small and efficient. They have terminals that only reside on the bottom side of the case. Each part has a dot on the top near the WE logo, but the dot is not indicated on the data sheet as a start of winding indicator (see Figure 9). Although this presents some confusion at first, the part is expected to perform the same in both assembly orientations with a rather symmetrical internal winding structure. The dot on the top of the IC therefore does not have to be indicated on the assembly silkscreen. Still, if used in an EMI-critical circuit, it might be wise to test in both directions to be sure.

Another Example: Würth WE-XHMI

We tested the DC3008A with a high performance Würth inductor whose start of winding is indicated with a dot on top of the package and in the data sheet (see Figure 10). The 74439346150 15 µH inductor is a great fit for the LT8386 form factor and current requirements. Again, for comparison with Coilcraft, emissions tests are run with this inductor mounted in both directions (see Figure 11).

The results (see Figure 12) are similar to the Coilcraft inductor. The emissions results show us that the orientation of the inductor in assembly has a significant effect on emissions. In this case, Orientation 1 in Figure 11 is clearly the best direction for lowest emissions. Lower frequency AM band (RE) and FM band (CE) emissions are clearly better with Orientation 1.

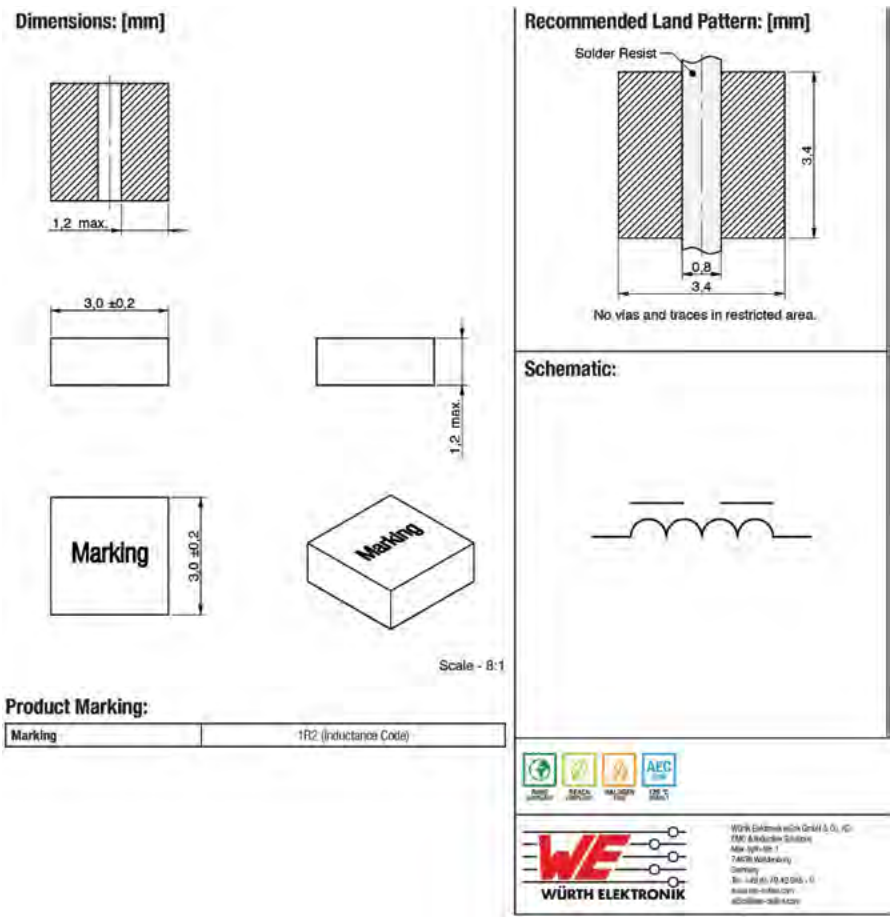

Figure 9. The WE-MAPI inductor data sheet does not indicate a start of winding dot, although there is a start of winding dot on the top marking of the component. These inductors may have no orientation-emissions effects, but one should test to be sure.

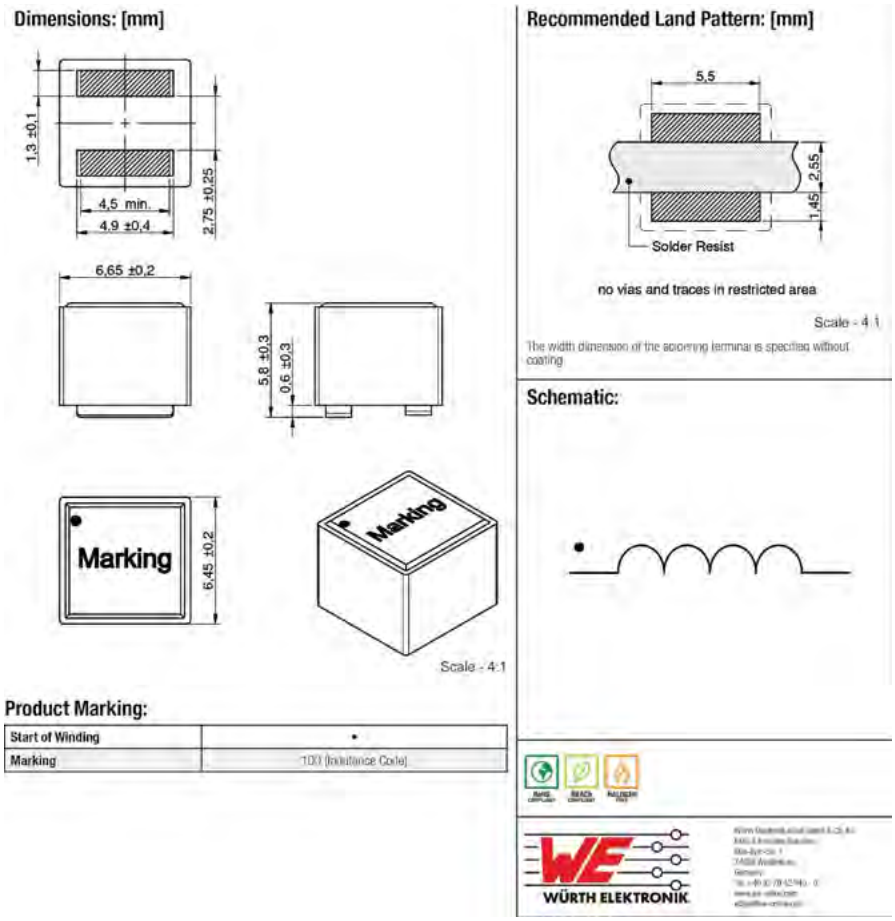

Figure 10. The start of winding for a WE-XHMI series inductor is indicated by the top-part marking.

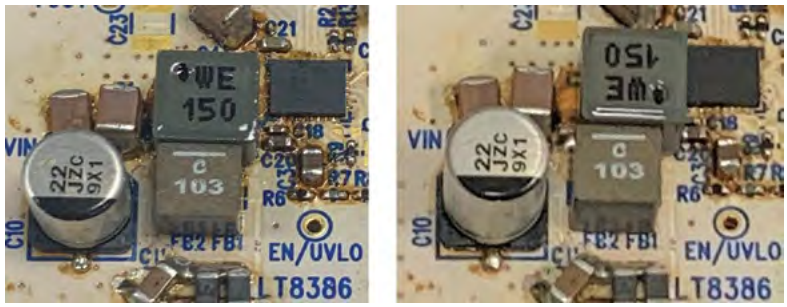

Figure 11. Würth 74439346150 ("WE 150") inductor orientation emissions testing with a DC3008A LT8386 LED driver. An L1 Orientation 1 (left) with a short terminal start of winding on the SW node and L1 Orientation 2 (right) with a long terminal on the SW node. Emissions results in Figure 12 show that the start of winding should be connected to the SW node for the best results.

2-Switch-Node Buck-Boost ICs (Results to Follow)

It is evident that inductor orientation can have an effect on emissions in a single switch-node boost LED driver. We can assume that boost voltage regulators have the same characteristic emissions results from the SW node since the power conversion and switching elements are the same in both voltage regulator and LED driver circuits.

We can also assume that buck regulators have similar SW node design priorities with regards to minimizing the antenna effect of the inductor terminals. Still, since the SW node of the buck regulator is closer to the input side of the converter, follow-up work might help determine if the effects of the inductor orientation are the same in regions of RE and CE as the boost regulator.

For 2-switch-node buck-boost converters, there is a bit of a predicament. Popular buck-boost converters such as those in the LT8390 60 V synchronous 4-switch buck-boost controller family have important low EMI features such as SSFM and small hot loop architecture. The single-inductor design creates a less clear picture of how inductor orientation might affect emissions. If the short terminal is placed on one SW node, then the long terminal acts like an antenna on the other SW node. In these designs, which orientation is best? What happens when all four switches are switching in the 4-switch operation region (V_{IN} close to V_{OUT})?

We will explore this question in a future article, where a 4-switch buck-boost controller with two SW nodes is EMI tested against inductor orientation. Food for thought: maybe there are more than two choices, 180° apart, for this topology?

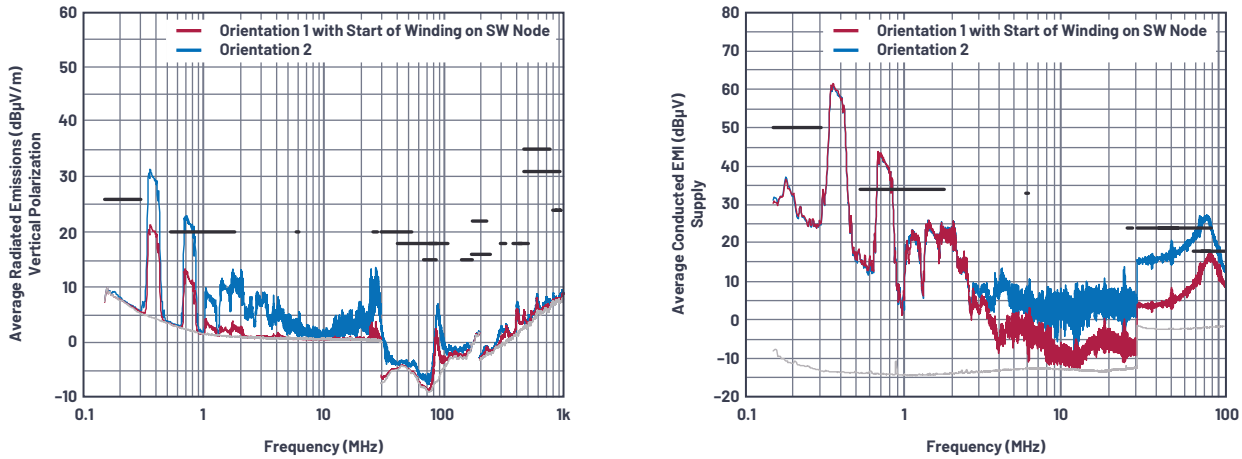

Figure 12. Radiated and conducted emissions show that the assembly orientation of Würth 74439346150 high performance inductor has a significant impact on emissions results.

Conclusion

Assembly orientation of the inductor in switching regulators does matter. When measuring emissions, note both the inductor orientation and its repeatability—be aware of any differences regarding the chosen inductor, test in both directions, and communicate clearly to board production any possible assembly pitfalls if orientation cannot be determined. Improved emissions could just be a simple 180° inductor rotation away.

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RAQ Issue 190: Adjustable, High Voltage Supply Combines Precision and Repeatability for Sensor Bias Applications

Lionel Wallace, Field Applications Engineer,
Jason Fischer, Applications Engineer, and
Ben Douts, Field Applications Engineer

Question:

Is there an easy way to create a high voltage supply for sensor bias applications?

Answer:

Sure, just use an IC with integrated precision resistors for feedback.

Introduction

An adjustable, high voltage power supply capable of high precision output can be difficult to build. Errors often result from drift over time, temperature, and variations within the production process. The resistive networks traditionally used for feedback are common error sources. In this article, a novel design utilizing an integrated circuit (IC) feedback path will be presented. This circuit is intended for sensor bias applications and provides higher precision, lower drift, greater flexibility, and even cost savings when compared to designs utilizing resistor networks for feedback.

Figure 1 illustrates the traditional approach to building an adjustable, high voltage bias circuit. A DAC is used to generate a control voltage, and an op amp is used to provide gain. The circuit in Figure 1 provides an output between ~0 V and 110 V from a control voltage ranging from 0 V to 5 V.

Since high voltage sensors are often quite capacitive, a resistor (R2) is normally used to isolate the op amp output from the load and avoid potential stability issues.

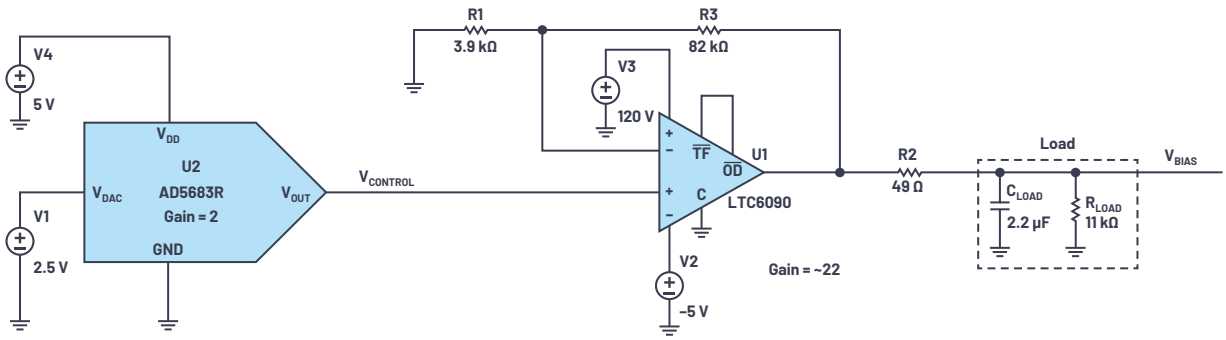

Figure 1. A traditional approach for a high voltage, adjustable bias circuit.

In some cases, these circuits work sufficiently well. When greater accuracy or more consistent long-term performance is needed, utilizing an IC to implement the feedback can be beneficial.

IC Feedback Implementation

The circuit shown in Figure 2 was configured with the following design goals in mind:

- Control voltage from 0 V to 5 V
- Output voltage adjustable from ~0 V to 110 V
- Output current >10 mA
- Initial accuracy of ±0.1 % typical
- No external precision resistors required

The circuit in Figure 2 consists of three main sections: the control voltage, an integrator, and a feedback path. The feedback is provided by an integrated circuit instead of a resistor network as described earlier.

The control voltage input range is 0 V to 5 V. The circuit gain of 22 provides an output bias voltage ranging from ~0 V (0 V × 22) to 110 V (5 V × 22). To generate the control voltage, the AD5683R was chosen. The AD5683R is a 16-bit *nano*DAC® that incorporates a 2 ppm/°C reference. Selecting the 5 V output span enables the circuit to provide a bias voltage ranging from ~0 V to 110 V in ~1.68 mV steps.

For the integrator, the LTC6090 was chosen. The LTC6090 is a high voltage op amp capable of rail-to-rail output and offering picoamp input bias current. The low input bias current is essential for achieving the high accuracy desired. Furthermore, the LTC6090 typically provides an open-loop gain of >140 dB, so system errors resulting from finite loop gain are greatly minimized.

The LTC6090 compares the feedback voltage with the control voltage and integrates the difference (that is, error), thereby adjusting the output (V_{BIAS}) to the desired setpoint. The time constant formed by R1 and C1 set the integration time and do not affect the amplifier accuracy, so precision components are not required. For testing, the load was modeled as an 11 kΩ resistor in parallel with a 2.2 µF capacitor.

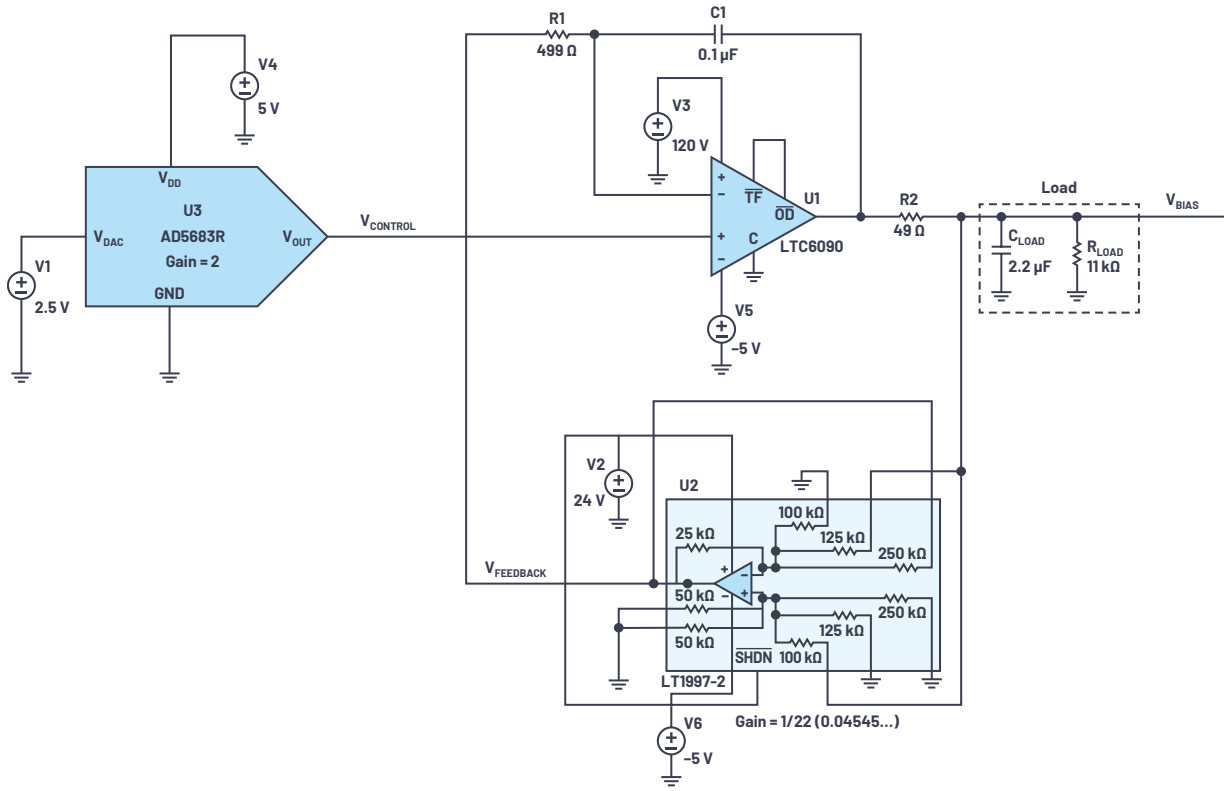

Figure 2. An LTspice® schematic for ~0 V to 110 V bias.

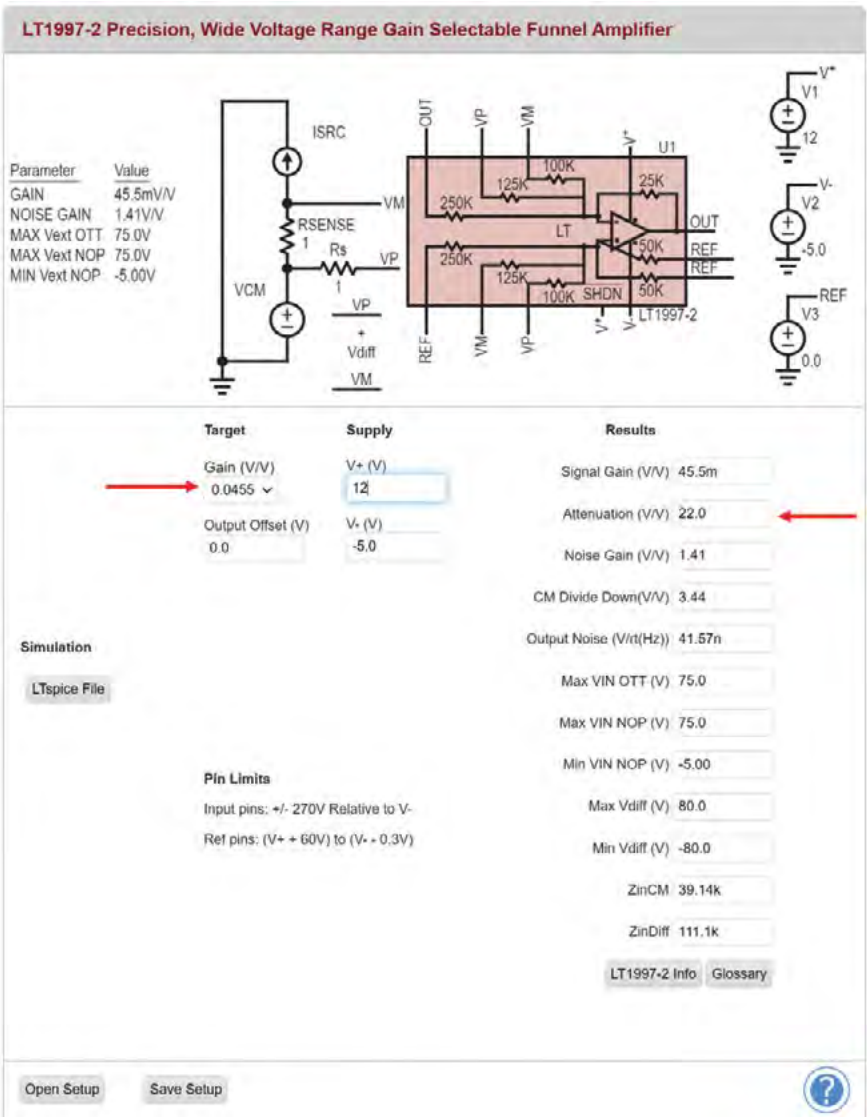

Figure 3. A screenshot from the LT1997-2 design tool with attenuation = 22.

The LT1997-2 difference amplifier provides an attenuation of 22 (gain = 0.4545...) for the feedback loop. The connections required to achieve an attenuation of 22 can be easily determined by using the online calculator for the LTC1997-2. A screenshot from the tool is shown in Figure 3.

The LT1997-2 is very flexible and allows a wide range of gain/attenuation combinations. Examples are provided in the data sheet, and the evaluation board supports many gain combinations via jumper selectable settings.

Figure 4. The LT1997-2 eval board (gain is set via jumpers and additional wire).

Test Setup

The circuit was modeled in LTspice and met the design goals. Hardware testing was facilitated via the use of the following evaluation boards:

- EVAL-AD5683R: AD5683R DAC evaluation board
- DC1979A: demo board for the LTC6090 140 V rail-to-rail output op amp (modified for testing)
- DC2551A-B: demo board for the LT1997 configurable precision amplifier (modified for testing)
- DC2275A: demo board for the LT8331 boost, 10 V ≤ V_{IN} ≤ 48 V, 120 V_{OUT} at up to 80 mA
- DC2354A: demo board for the LTC7149 buck configured as negative V_{OUT}; 3.5 V ≤ V_{IN} ≤ 55 V; V_{OUT} = –3.3 V/–5 V/adjustable to –56 V at up to 4 A

Generation of Control Voltage

The control voltage for the circuit was set using the AD5683R eval board. This board was connected via a USB port to a laptop running the Analog Devices ACE (Analysis, Control, Evaluation) software. ACE provides a simple GUI to configure the AD5683R and set the DAC output voltage. The output voltage provides the setpoint for the high voltage bias output.

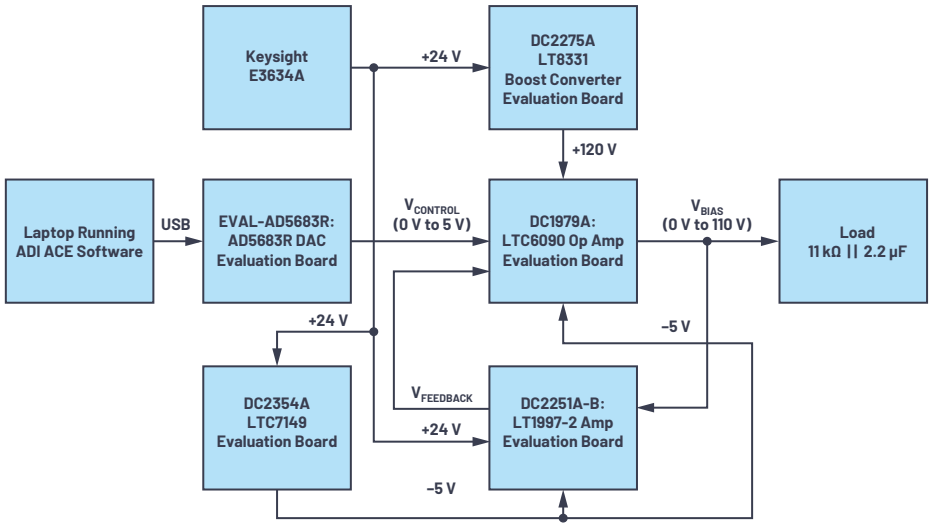

Figure 5. Block diagram of test configuration.

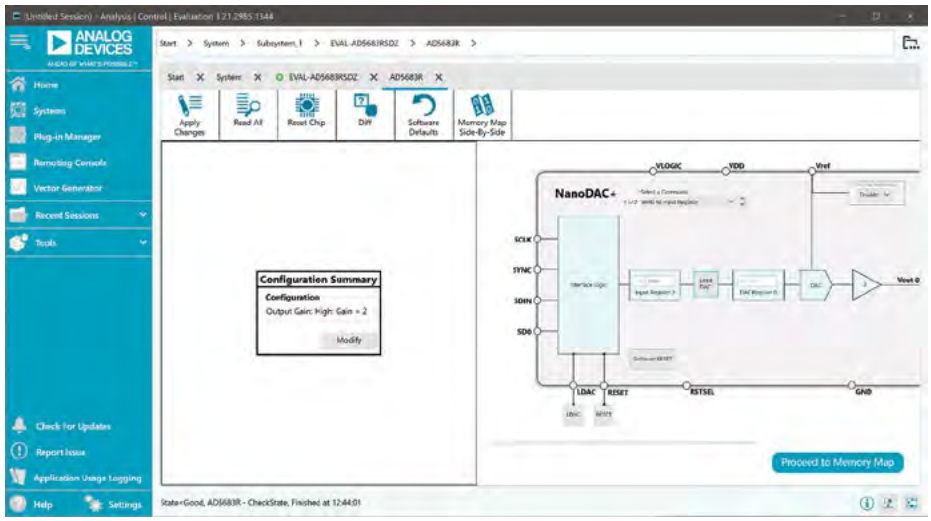

Figure 6. A screenshot of the ACE interface for the AD5683R eval board.

DC Accuracy

The measurements in Table 1 and Figure 7 were made using a Keysight 34460A DMM at 24°C ambient. The output of the AD5683R eval board was calibrated to four decimal places and controlled via ADI's ACE software. These results were from a single set of boards and do not represent min/max specifications.

Table 1. Measured Output Voltage vs. Expected Output Voltage

Control Voltage (V)	Desired Bias Voltage (V)	Measured Bias Voltage (V)	Error (%)
0.0000	0	0.0121	–
0.5000	11	11.004	0.036%
1.0000	22	22.005	0.023%
1.5000	33	33.005	0.015%
2.0000	44	44.005	0.011%
2.5000	55	55.007	0.013%
3.0000	66	66.007	0.011%
3.5000	77	77.008	0.010%
4.0000	88	88.008	0.009%
4.5000	99	99.010	0.010%
5.0000	110	110.009	0.008%

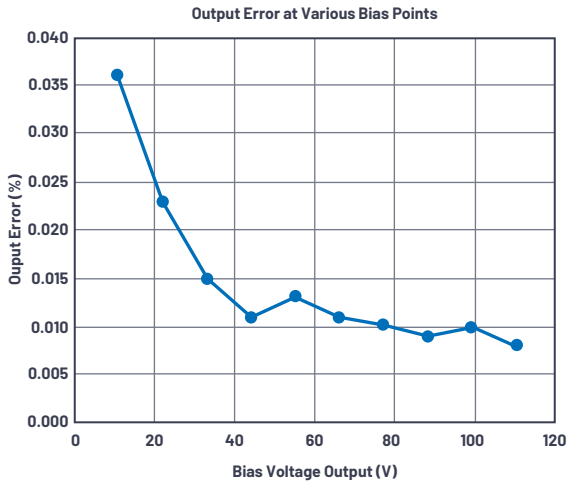

Figure 7. Output voltage error vs. bias voltage.

Notice that below ~40 V output, the error is dominated by amplifier offsets within the circuit. At low bias voltages the offsets are of greater magnitude than the gain errors. At higher bias voltages, the offsets contribute less as a percentage and the gain errors dominate. An error analysis is presented later in this article and provides more detail.

AC Response

A step function was applied to the control input for various voltages. The output and feedback voltages were measured (see Figure 8 through Figure 10). Notice that the bias voltage ramps smoothly to the desired value.

Figure 8. Step response (0 V to 1 V control input).

Figure 9. Step response (0 V to 2.5 V control input).

Figure 10. Step response (0 V to 5 V control input).

Start-Up Waveforms

The start-up waveforms for the power supplies and signals were observed. This was done to ensure that high voltage was not inadvertently applied to the bias output. The AD5683R provides a control voltage that starts at 0 V. As the power supplies ramp up, a small glitch of ~3 V was observed on the bias output. Given the high voltage nature of the bias output, this was deemed acceptable for test purposes.

If this circuit were to be used in a production system, it would be advisable to sequence the power supplies such that the control voltages were applied first with the high voltage power supply starting subsequently. This sequence would avoid the potential of high voltage spikes on the bias voltage output during the start-up process. A simple analog sequencer such as the ADM1186 would likely be sufficient to implement this function.

Figure 11. Start-up waveforms—power supplies.

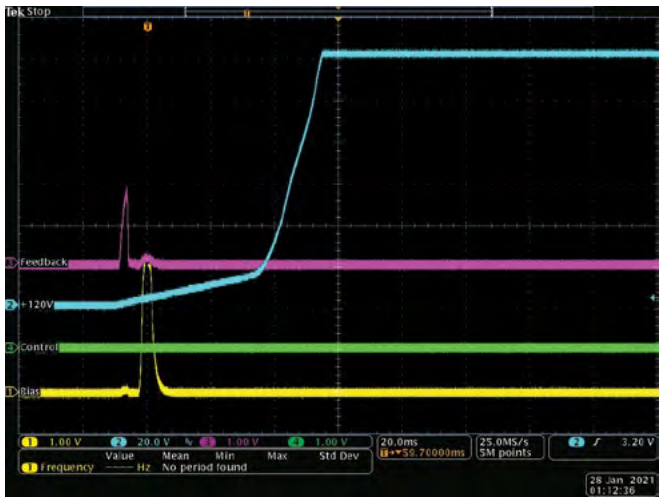

Figure 12. Start-up waveforms—signals.

Photos of Test Setup

The LTC6090 eval board was mounted to the bottom of the LT1997-2 eval board. These were the only boards that required modification for the test setup. The DAC and power eval boards were used in their stock configuration and are not shown for simplicity.

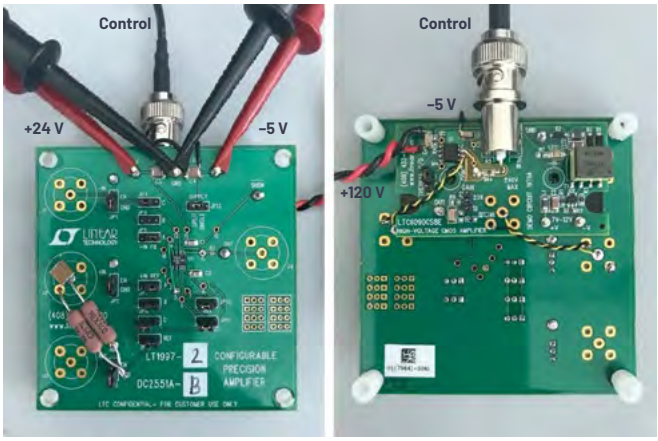

Figure 13. The LT1997-2 eval board with the LTC6090 eval board mounted on the bottom.

Error Analysis

An error analysis was performed. The predominant error sources within the circuit are shown in Table 2 along with typical and maximum values.

The maximum error at 110 V bias output was calculated to be 0.0382% or 42 mV. This includes all errors from part variation as well as variations over the full temperature range (–40°C to +125°C). The typical error at 110 V bias output was calculated to be 0.00839%, which agrees well with the measured results (0.008% or 9 mV).

A Note About Power Supplies

The hardware used during testing was powered with supplies of ±5 V, 24 V, and 120 V. Here are some additional notes on how these supply rails were chosen:

- 5 V was required for the AD5683R DAC.
  - In order to achieve 5 V output from the DAC, the power supply voltage may have to be set slightly above 5 V. Even small loads can limit the maximum output value. See Figure 38 on page 15 of the AD5683R data sheet for additional information.
- –5 V was used to allow the LTC6090 and LT1997-2 to operate with a control voltage input approaching 0 V.
  - The input common-mode range for the LTC6090 is limited to 3 V above V–.
  - The LTC7149 demo board was used for convenience to generate the –5 V rail.
    - The LTC7149 eval board is capable of up to 4 A output.
    - The circuit requires <25 mA at –5 V. A simple charge pump inverter would be sufficient. Consider the ADP5600 as an example.
- 120 V was used for V+ for the LTC6090.
  - While the LTC6090 provides rail-to-rail output, heavy loads require additional headroom for V+.
- 24 V was used as the positive supply for the LT1997-2.
  - This voltage was chosen to avoid Over-The-Top® operation. Certain performance characteristics of the LT1997-2 are degraded in the Over-The-Top region. See page 14 of the LT1997-2 data sheet for additional information.

Table 2. Output Voltage Error Analysis

	Maximum Error from Data Sheet*							
	Error (%)	Error (µV)	Error (nA)	Error at Feedback Node (µV)	Error at Bias Node (mV)		Error When Control Voltage = 1 V; Output = 22 V (%)	Error When Control Voltage = 5 V; Output = 110 V (%)
LT1997-2 Gain	0.008						0.0080	0.0080
LT1997-2 Voltage Offset		200		282	6.204		0.0282	0.0056
LT1997 I_B Offset			10	227	4.994		0.0227	0.0045
LTC6090 Offset		1000		1000	22		0.1000	0.0200
						Total Error (%):	0.1589	0.0382
	Typical Error from Data Sheet**							
	Error (%)	Error (µV)	Error (nA)	Error at Feedback Node (µV)	Error at Bias Node (mV)		Error When Control Voltage = 1 V; Output = 22 V (%)	Error When Control Voltage = 5 V; Output = 110 V (%)
LT1997-2 Gain	0.001						0.00100	0.00100
LT1997-2 Voltage Offset		20		28.2	0.6204		0.00282	0.00056
LT1997 I_B Offset			0.5	11.35	0.2497		0.00114	0.00023
LTC6090 Offset		330		330	7.26		0.03300	0.00660
						Total Error (%):	0.03796	0.00839

*Includes part variation and full temperature range
**At 25°C

Comparison of IC Feedback to Traditional Resistor Network Feedback

Let's compare a few design metrics of the traditional approach shown in Figure 1 to the IC feedback approach shown in Figure 2. For this comparison, the LT1997-2 (see Figure 14) was chosen as the IC for the feedback network. Notice that highly matched, precision resistors are embedded within the LT1997-2.

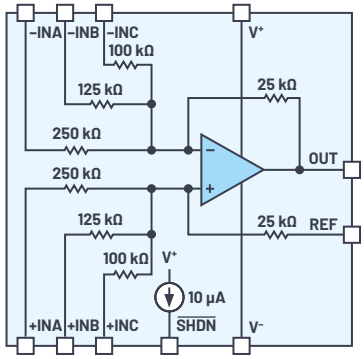

Figure 14. Block diagram of the LT1997-2.

Table 3. LT1997-2 vs. Two 1206 Discrete Precision Resistors (Note: 1206 Was Chosen for Working Voltage of 200 V)

	Discrete Resistors	LT1997-2	Comments*
Size	✔		2× (3.1 mm × 1.6 mm) vs. (4 mm × 4 mm)
Cost	✔✔✔		2 × ($0.11) vs. $3.39 (~1k price)
Resistor Precision		✔✔	0.1% vs. 0.008%
Temp Drift		✔✔	25 ppm/°C vs. 1 ppm/°C
Max Sensor Voltage		✔	200 V vs. 270 V

*RT1206BRD07150KL, 1k pricing from Digi-Key as of December 2020
LT1997-2IDF#PBF, 1k pricing from ADI website as of December 2020

Table 4. LT1997-2 vs. Metal Film Resistor Network

	Metal Film Resistor Network	LT1997-2	Comments*
Size		✔✔	(8.9 mm × 3.5 mm × 10.5 mm) vs. (4 mm × 4 mm × 0.75 mm) Resistor is through hole and 10.5 mm tall
Cost		✔✔✔	$22.33 vs. $3.76 (~500-piece price)
Resistor Precision	Tie	Tie	0.005% vs. 0.008%
Temp Drift	Tie	Tie	1.5 ppm/°C vs. 1 ppm/°C
Max Sensor Voltage	✔		350 V vs. 270 V

*Y0114V0525BV0L, 500-piece price from Digi-Key as of December 2020
LT1997-2IDF#PBF, 500-piece price from ADI website as of December 2020

Table 5. LT1997-2 vs. Silicon-Based Precision Resistor

	Silicon-Based Resistor Network	LT1997-2	Comments*
Size	✔		(3.04 mm × 2.64 mm) vs. (4 mm × 4 mm)
Cost	✔		$1.90 vs. $3.39 (~1k price)
Resistor Precision		✔	0.035% vs. 0.008%
Temp Drift	Tie	Tie	1 ppm/°C vs. 1 ppm/°C
Max Sensor Voltage		✔✔	80 V vs. 270 V

*MAX5490VA10000+, 1k pricing from Maxim website as of December 2020
LT1997-2IDF#PBF, 1k pricing from ADI website as of December 2020

While the LT1997-2 is much more expensive than two chip resistors, it provides much better performance. When compared to a metal film resistor network, the LT1997-2 provides both size and cost advantages. When compared to a silicon-based resistor network, the LT1997-2 provides advantages in precision and working voltage. Furthermore, the integration of different resistor values within the LT1997-2 is an advantage over all the competing solutions providing gain flexibility via external jumpers if desired.

Using an IC that integrates precision resistors has another advantage that may not be obvious at first. The summing junctions of the amplifier are buried within the device and are not exposed to the PCB. This protects these sensitive nodes from unwanted inputs. Also, in many gain configurations, the internal resistors are connected externally to either ground or the output. This avoids leakage paths that could affect the circuit accuracy. Leakage paths are common error sources in higher voltage circuits. See page 14 of the LTC6090 data sheet for more information on this topic.

Conclusion

Adjustable, high voltage, bias circuits have traditionally utilized op amps with resistor networks for feedback to create a precision output. While this approach is simple to understand, achieving precise, repeatable performance can be difficult. Utilizing an IC to provide feedback instead of a resistor network can provide more accurate and consistent results.

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Lionel Wallace joined Analog Devices in 2009. During his time at ADI he has held several positions across engineering and sales. Lionel currently serves as a field applications engineer based in Alabama. Lionel received his B.S.E.E. from Auburn University and M.S.E.E. from the University of Alabama Huntsville. He can be reached at lionel.wallace@analog.com.

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Ben Douts is a field applications engineer with Analog Devices in South Carolina. He has worked in several roles including test engineering and integrated circuit design, focusing on precision analog circuits and power management. Ben received his S.B.E.E. from MIT in 1998. He can be reached at benjamin.douts@analog.com.

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