HEP8225

8225-xxx

No. 87-508225-000 Revision G

HARDWARE

TECHNICAL REFERENCE

Intel® Xeon® E5-2600 Series v3 & v4

14, 12, 10, 8, and 6-Core

PROCESSOR-BASED

SHB

WARRANTY

The following is an abbreviated version of Trenton Systems' warranty policy for High Density Embedded Computing (HDEC®) products. For a complete warranty statement, contact Trenton or visit our website at www.TrentonSystems.com.

HDEC® Series board-level products manufactured by Trenton are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Systems, Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Systems' discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Systems, Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Systems, Inc. Trenton Systems, Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

In no event shall Trenton Systems, Inc. be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental or consequential damages arising out of or in connection with the performance or use of the product or information provided. Trenton Systems, Inc.'s liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Trenton Systems, Inc.

RETURN POLICY

A Return Material Authorization (RMA) number, obtained from Trenton Systems prior to return, must accompany products returned for repair. The customer must prepay freight on all returned items, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton Systems via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Gainesville, GA facility:

TRENTON Systems, Inc.
1725 MacLeod Drive
Lawrenceville, GA 30043
Attn: Repair Department

Contact Trenton for our complete service and repair policy.

TRADEMARKS

HDEC is a trademark of Trenton Systems, Inc.
IBM, PC/AT, VGA, EGA, OS/2 and PS/2 are trademarks or registered trademarks of International Business Machines Corp.
AMI and AMIBIOS are trademarks of American Megatrends Inc.
Intel, Xeon, Intel Quick Path Interconnect, Intel Hyper-Threading Technology, Intel Virtualization Technology and Intel Active Management Technology are trademarks or registered trademarks of Intel Corporation.
MS-DOS and Microsoft are registered trademarks of Microsoft Corp.
PCI Express is a trademark of the PCI-SIG
All other brand and product names may be trademarks or registered trademarks of their respective companies.

LIABILITY DISCLAIMER

This manual is as complete and factual as possible at the time of printing; however, the information in this manual may have been updated since that time. Trenton Systems, Inc. reserves the right to change the functions, features or specifications of their products at any time, without notice.

E-mail: Support@TrentonSystems.com
Web: www.TrentonSystems.com

TRENTON Systems, Inc.
1725 MacLeod Drive • Lawrenceville, Georgia 30043
Sales: (800) 875-6031 • Phone: (770) 287-3100 • Fax: (770) 287-3150

This page intentionally left blank

Table of Contents

HANDLING PRECAUTIONS

WARNING: This product has components that may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

RECOMMENDED BOARD HANDLING PRECAUTIONS

This SHB has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your HEP8225 (8225-xxx) SHB. System performance may be affected by incorrect usage of these features.

DDR4 MEMORY

There are four active DDR4 standard DIMM sockets on the board for each processor. Each standard DIMM socket can support a 32GB DIMM for a total possible DDR4 system memory capacity of 256GB. When 64GB DDR4 DIMMs become readily available, the maximum supported SHB memory capacity will increase to 512GB.

In most applications, 8GB or 16 GB DIMM sizes are sufficient providing a maximum memory capacity of 64GB and 128GB respectively. The required DIMM size will depend on the needs of the application. For many workloads, 8GB or 16GB DIMMs should be fine. For applications or benchmarks that benefit from memory capacity more than memory performance, such as TPC-C and TPC-E, there are two options. Option 1 is likely best for TPC-C since it allows a greater memory capacity.

Option 1) Use the largest DIMMs available, currently expected to be 32GB or 64GB quad rank DDR4 LRDIMMs.
Option 2) Use the largest dual rank registered DIMMs available these currently include 16GB or 32GB dual rank DIMMs.

The processor's four individual direct-connect memory channel interfaces terminate with a single in-line standard DIMM memory module socket BK0 through BK7. The System BIOS automatically detects memory type, size and speed.

Trenton recommends ECC registered DDR4-2400 standard DIMM memory modules for use on the HEP8225, and these ECC registered (72-bit) DDR4 standard DIMMs must be PC4-19200 compliant.

The SHB uses industry standard gold finger standard DIMM memory modules, which must be PC4-19200 compliant and have the following features: 288-pin, gold-plated contacts and ECC registered (72-bit) DDR4-2133 memory.

Populate all even numbers of channels per processor socket. Sub-optimal memory channel utilization may occur if only1 or 3 memory channels per processor are populated.

NOTES:

- To maximize system performance and reliability, Trenton recommends populating each memory channel with DDR4-2400 DIMMs on the HEP8225 dual-processor board.
- All memory modules must have gold contacts.

Populate the memory sockets starting with the DIMM socket closest to the CPU and work your way toward the edges of the SHB as illustrated in the chart below:

DIMM Population Order	CPU0	CPU1
1	BK1	BK5
2	BK3	BK7
3	BK0	BK4
4	BK2	BK6

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board.

PROCESSOR OPTIONS

Max. DDR4 Speed	Processor	Base Clock Speed	Cores / Threads	Cache	Long-Life Availability (5 to 7 years)	Maximum Thermal Design Power (TDP)	Operating Temperature Range*
DDR4-2400	Intel® Xeon® E5-2680 v4	2.4GHz	14 / 28	35MB	Yes	120W	0°C to 45°C
DDR4-2133	Intel® Xeon® E5-2680 v3	2.5GHz	12 / 24	30MB	Yes	120W	0°C to 45°C
DDR4-2400	Intel® Xeon® E5-2658 v4	2.3GHz	14 / 28	35MB	Yes	105W	0°C to 50°C
DDR4-2133	Intel® Xeon® E5-2658 v3	2.2GHz	12 / 24	30MB	Yes	105W	0°C to 50°C
DDR4-2400	Intel® Xeon® E5-2648L v4	1.8GHz	14 / 28	35MB	Yes	75W	0°C to 50°C
DDR4-1866	Intel® Xeon® E5-2648L v3	1.8GHz	12 / 24	30MB	Yes	75W	0°C to 50°C
DDR4-2133	Intel® Xeon® E5-2628L v4	1.9GHz	12 / 24	30MB	Yes	75W	0°C to 50°C
DDR4-1866	Intel® Xeon® E5-2628L v3	2.0GHz	10 / 20	25MB	Yes	75W	0°C to 50°C
DDR4-2133	Intel® Xeon® E5-2618L v4	2.2GHz	10 / 20	25MB	Yes	75W	0°C to 50°C
DDR4-1866	Intel® Xeon® E5-2618L v3	2.3GHz	8 / 16	20MB	Yes	75W	0°C to 50°C
DDR4-1600	Intel® Xeon® E5-2608L v3	2.0GHz	6 / 12	15MB	Yes	50W	0°C to 50°C

SATA RAID Operation

The SHB's Intel® C612 Platform Controller Hub (PCH) features Intel® Rapid Storage Technology, which enables SHB support for RAID 0, 1 and 10 implementations. To configure the SATA ports as RAID drives, you must install the Intel® RST enterprise driver software. This link takes you to version 3.2 that was tested and validated on the SHB. A later version 3.5 is also available for download, but this version has not been tested on the board. Links to both driver versions are located on Trenton's website by accessing the Downloads tab of the HEP8225 product detail web pages or the RAID Drivers section of the Technical Support page.

A Word About RAID

The Intel® C612 Platform Controller Hub supports eight SATA/600 channels on two separate controllers notated as SATA and sSATA. The Trenton HEP8225 SHB supports these channels with two ports on the SHB itself and up to six passed down to a backplane (dependent on configuration, refer to the Trenton Systems HDEC® Backplane Technical Reference for more information). The Intel® C612 Platform Controller Hub RAID arrays are limited to four drives total and arrays cannot span controllers. This results in a capability of up to two (2) RAID arrays of up to four (4) drives total.

The ports on the SHB are controlled by the SATA controller, designated P10 and P11.

A Word About PCI Express 3.0 Interfaces

PCIe 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen3, Gen2 and Gen1.1 I/O cards on the same interface link. Running a PCIe 3.0 target device such as a Gen3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the HEP8225) to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off and not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specific of your particular PCIe 3.0 implementation.

High Density Embedded Computing Backplane I/O

Today's HEP8225 configurations with Intel® Xeon® E5-2600 v3 series processors provide the following backplane I/O connectivity via the HDEC dual-density edge connector:

- 80 lanes of PCIe 3.0
- Six SATA 3.0/600 Interfaces
- 2- 10Gigabit Ethernet, 2- Gigabit Ethernet
- Ten USB Interfaces, , 4 – USB 3.0 (I/O Plate), 2 – USB 3.0 (Backplane Routing) 4 – USB 2.0 (Backplane Routing)
- 1- RS232
- Status I/O, 2- SMBus, 1- IPMB, 8- GPIO, Intruder Alert, CMOS Clear input, 4- SHB Present Detect Pins
- Power and Reset Switches and LEDs, Power Supply ON LED, 10- Additional LED output, 1- Power Good LED, HDD LED out
- System Speaker and Audio In/Out
- 8- Fan PWM and Tach interfaces

HDEC-series Backplanes

All of Trenton's HDEC® series backplane solutions can be utilized with the HEP8225. These include, but are not limited to: HDB8236, HDB8237, HDB8228, HDB8227 and HDB8229. Each of these backplane designs have different form factors and target chassis. Contact Trenton for more information on each backplane and which would perform optimally for your application, or, a custom solution tailored exactly to your needs.

BIOS

The HEP8225 feature the Aptio® 5.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. Details of the Aptio TSE are provided in the separate *HEP8225 BIOS Technical Reference* manual.

Operating Systems

Trenton's HEP8225 has been tested using a number of popular and readily available operating systems including: Microsoft Windows Server 2008 R2, Windows Server 2012 x64, Windows 7.1 x64, Windows 8.1 x64 and a number of variations of Linux including Red Hat Enterprise Linux 7.1 x64, CentOS 7.x x64 and OpenSUSE 13.1 x64. This testing process confirms the SHB's PCI Express interface and device I/O functionality. Trenton does not recommend using the Microsoft Windows XP32 SP2 or SP3 operating system due to limited functionality concerns. Contact Trenton Tech Support for additional information.

Power Connection

The HEP8225 supports soft power signals along the Advanced Configuration and Power Interface (ACPI). They are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to the *Power Connection* section in the SHB manual to determine the method that will work with your specific system design. The *Advanced Setup* chapter in the manual contains the ACPI BIOS settings.

For More Information

For more information on any of these features, refer to the appropriate sections *HEP8225 Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the HEP8225 web page.

This page intentionally left blank

Chapter 1 Specifications

Introduction

The HEP8225 is a member of the new class of High Density Embedded Computing (HDEC®) Series of products from Trenton Systems, delivering unparalleled system performance density for throughput-intensive system applications. Each Intel® Xeon® E5-2600 v4 or v3 processor option available on the HEP8225 supports forty (40) PCIe Gen3 links per CPU. This results in a total of eighty (80) PCIe interfaces available from the double-density PCI Express edge connectors on the HEP8225 for interfacing purposes on an HDEC Series system backplane. These native PCIe interfaces enable high-speed integration of a wide variety of industry standard PCI Express plug-in cards into an embedded system design with minimal data latencies.

Combining the latest Intel® Xeon® E5-2600 v4 or v3 Series processors; previously known as Broadwell-EP and Haswell-EP respectively, on the HEP8225 enables several performance improvements including additional executing cores, better TDP ratings and improved power utilization. In addition to the PCI Express 3.0 device interfaces, the HEP8225 design takes advantage of the four-channel DDR4 integrated memory controller capability built-in to each Intel® Xeon® E5-2600 v4 or v3 processor. The memory controller supports DDR4-2400 memory interface speeds.

Note: The HEP8225's actual maximum memory interface speed achieved in a specific system application is a function of the specific processor option selected.

The four memory channels per processor result in a total of eight direct access memory interfaces per HEP8225. The combination of the HEP8225's four memory channels per processor, and the utilization of eight 64GB DDR4 memory DIMMs, results in a maximum HEP8225 memory capacity of 512GB.

Video and I/O features on the HDEC boards include:

- A Graphics Processing Unit (GPU) driven with an internal x1 PCIe link and capable of supporting pixel resolutions up to 1920 x 1200 (WUXGA)
- Two (2) 10 GbE LAN interfaces on the I/O backplate.
- Two (2) 1 GbE LAN interfaces on the I/O backplate.
- Two SATA/600 ports that can support independent drives or RAID drive arrays
- Ten USB Interfaces, 4 – USB 3.0 (I/O Plate), 2 – USB 3.0 (Backplane Routing) 4 – USB 2.0 (Backplane Routing) Six (6) SATA/600 interfaces routed to the edge connector for use on a backplane

The listing below summarizes the available versions of the HEP8225 with the standard configuration:

Intel Brand Name	Cores	Embedded	Intel Product Code	Trenton Processor Part Number	Trenton Base Tab Number
Intel Xeon E5-2680 **v4**	14	Yes	CM8066002031501	26-004846-486	007
Intel Xeon E5-2680 **v3**	12	Yes	CM8064401439612	26-004846-458	018
Intel Xeon E5-2658 **v4**	14	Yes	CM8066002044801	26-004846-485	004
Intel Xeon E5-2658 **v3**	12	Yes	CM8064401545904	26-004846-459	016
Intel Xeon E5-2648L **v4**	14	Yes	CM8066002189001	26-004846-488	021
Intel Xeon E5-2648L **v3**	12	Yes	CM8064401546007	26-004846-463	022
Intel Xeon E5-2628L **v4**	12	Yes	CM8066002044903	26-004846-489	041
Intel Xeon E5-2628L **v3**	10	Yes	CM8064401547200	26-004846-464	043
Intel Xeon E5-2618L **v4**	10	Yes	CM806600tbd	26-004846-491	065
Intel Xeon E5-2618L **v3**	8	Yes	CM8064401610301	26-004846-465	066
Intel Xeon E5-2608L **v4**	8	Yes	CM806600tbd	26-004846-493	081
Intel Xeon E5-2608L **v3**	6	Yes	CM8064402033500	26-004846-466	083

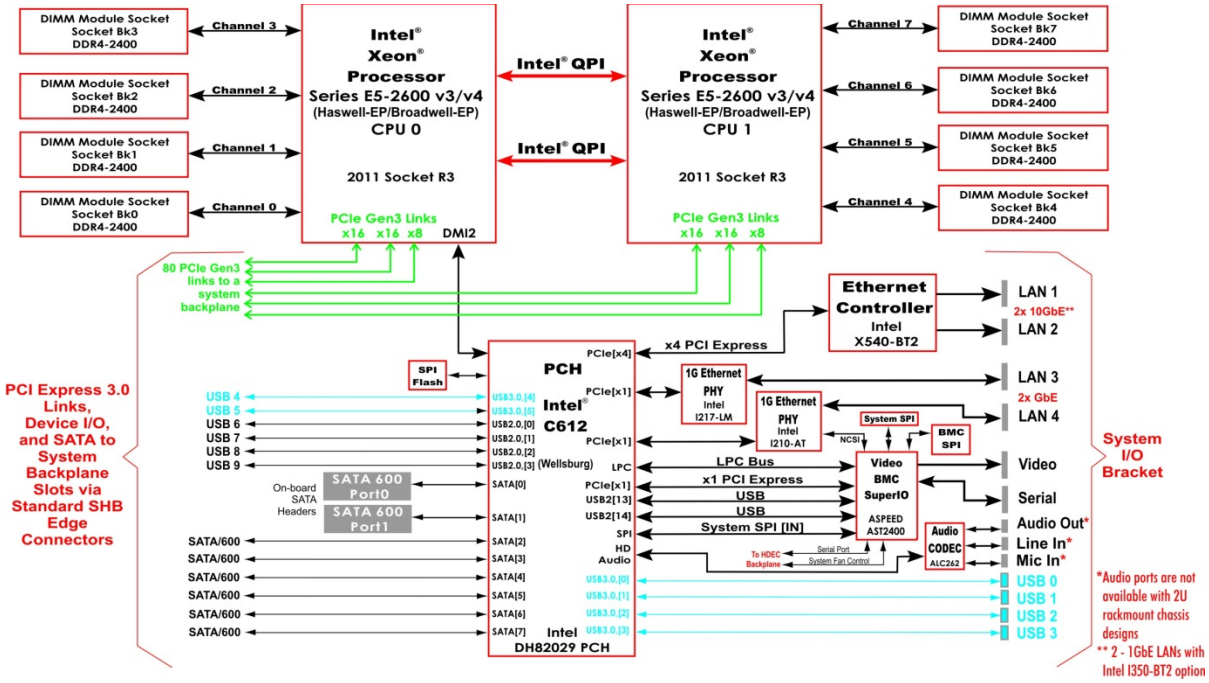
NOTE: **v4** *indicates a Broadwell-EP processor option and* **v3** *indicates Haswell-EP*

Additional processors and configurations may be available. Contact Trenton for the latest ordering information.

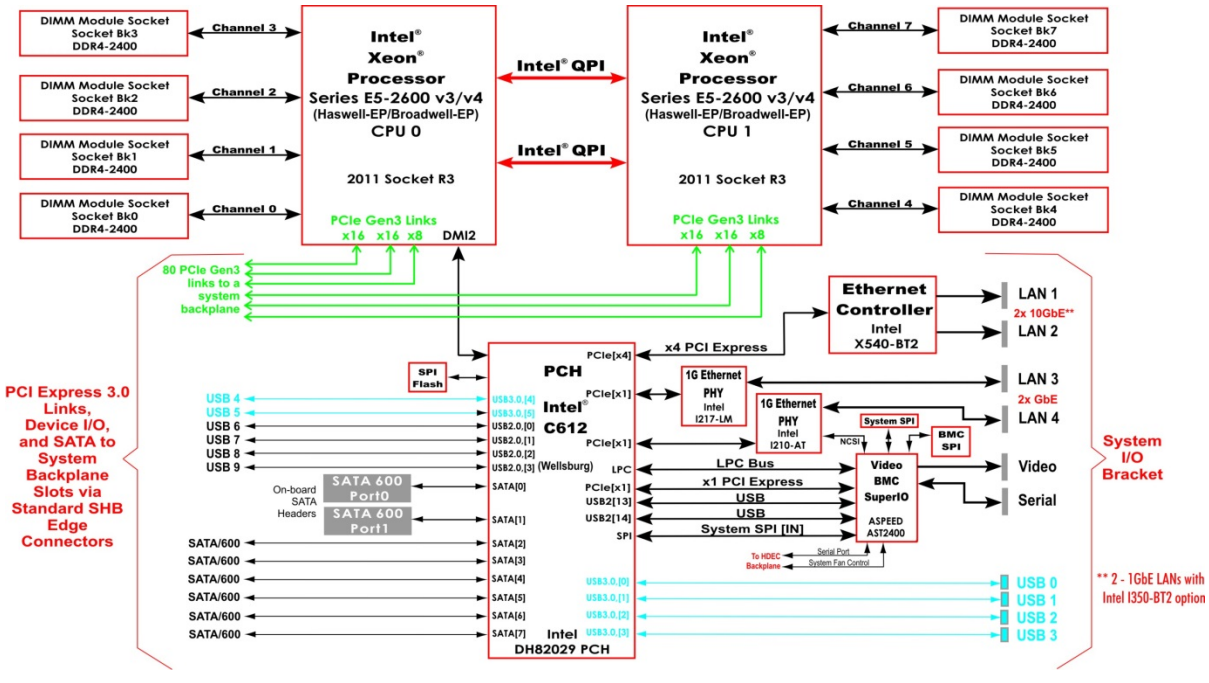
Board Features

- Intel® Xeon® E5-2600 v4 Series Processors (Broadwell-EP
- Intel® Xeon® E5-2600 v3 Series Processors (Haswell-EP)
- Intel® C612 Platform Controller Hub (Wellsburg)
- Direct PCI Express® 3.0 links into the Intel® Xeon® E5-2600 Series Processors
- HEP8225 provides a total of 80 lanes of PCI Express for off-board system integration
- Direct DDR4-2400 Memory Interfaces into the Intel® Xeon® E5-2600 Series Processors
- Eight DDR4 DIMM sockets capable of supporting up to 512GB of system memory
- Video interface utilizing ASPEED AST2400 SuperIO Graphics Processing Unit
- Two 10GbE LAN interfaces available on the SHB's I/O plate
- Two 10/100/1000Base-T Ethernet LAN interfaces available on the SHB's I/O plate
- Two on-board SATA/600 ports support independent SATA storage devices that may be configured to support RAID 0, 1 or 10 implementations
- Six pass-through SATA/600 ports support independent SATA storage devices that may be configured to support RAID 0, 1 or 10 implementations
- Six Universal Serial Bus (USB 3.0) interfaces
- Four Universal Serial Bus (USB 2.0) interfaces
- Full PC compatibility

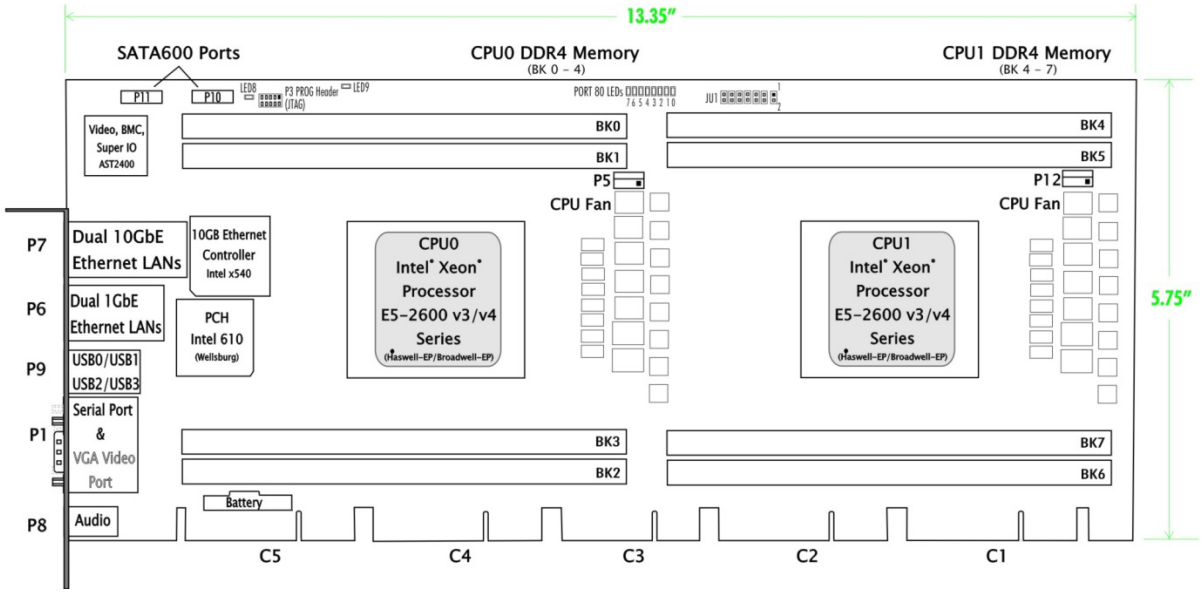
HEP8225 (8225-xxx) – Dual-Processor SHB Block Diagram—Audio Ports Populated



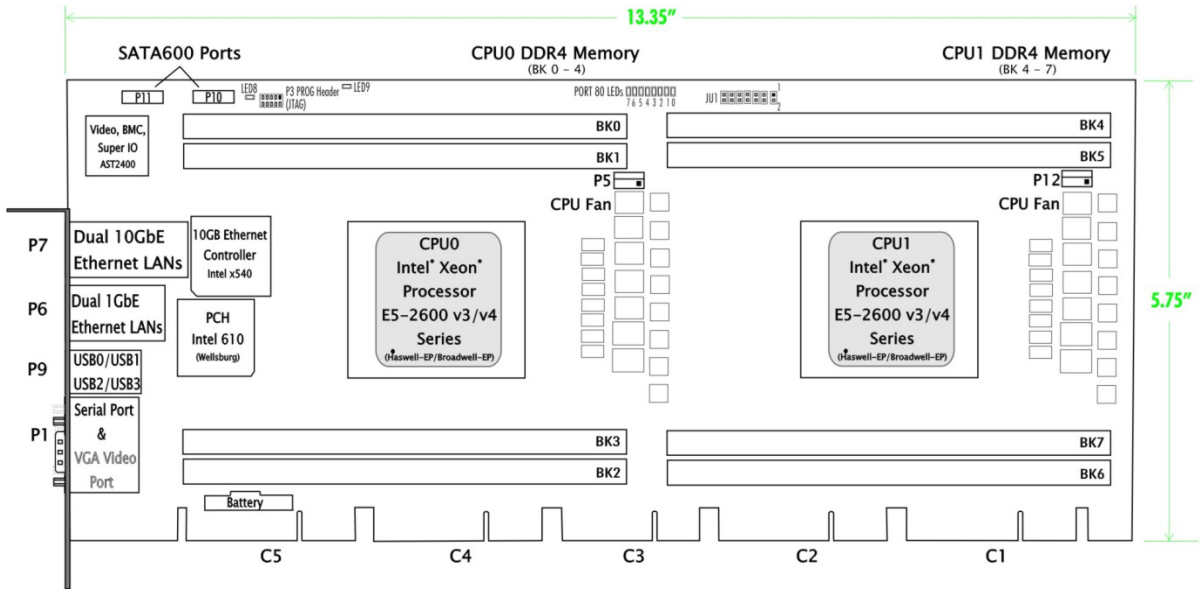
HEP8225 (8225-xxx) – Dual-Processor SHB Block Diagram—Audio Ports Not Populated



HEP8225 (8225-xxx) – Dual-Processor SHB Layout Diagram—Audio Ports Populated



HEP8225 (8225-xxx) – Dual-Processor SHB Layout Diagram—Audio Ports Not Populated



Processors

- Intel® Xeon® E5-2600 v4 Series Processors (Broadwell-EP) or
- Intel® Xeon® E5-2600 v3 Series Processors (Haswell-EP)

Platform Controller Hub (PCH)

Intel® C612 (Wellsburg)

Serial Interconnect Interface

PCI Express® 3.0, 2.0 and 1.1 compatible

Data Path (max speed supported*)

DDR4-2400 Memory - 72-bit (per channel)
* Processor dependent

Serial Interconnect Speeds

PCI Express 3.0 – 8.0GHz per lane (with proper PCIe 3.0 root complex to the target card tuning and optimization)
PCI Express 2.0 – 5.0GHz per lane
PCI Express 1.1 - 2.5GHz per lane

Intel® Quick Path Interconnect Between CPUs

The Quick Path Interconnect enables processor-to-processor resource sharing and fast data transfers between CPUs. The Intel® QPI speed between CPUs in a dual-processor HEP8225 configuration is a function of the specific processors used on the board as illustrated in the following table.

Processor	Intel® Quick Path Interconnect (QPI) Speed
Intel® Xeon® E5-2680 v4 Intel® Xeon® E5-2680 v3 Intel® Xeon® E5-2658 v4 Intel® Xeon® E5-2648L v4 Intel® Xeon® E5-2648L v3	9.6GT/s
Intel® Xeon® E5-2628L v4 Intel® Xeon® E5-2628L v3 Intel® Xeon® E5-2618L v4 Intel® Xeon® E5-2618L v3	8.0GT/s
Intel® Xeon® E5-2608L v4 Intel® Xeon® E5-2608L v3	6.4GT/s

Intel® Direct Media Interface 2 (DMI2) Between Processor and Intel® C612 PCH

This x4 PCIe 2.0 interface provides the data communication path between the PCH and processor. On a dual-processor, HEP8225 the CPU0 connects directly to the PCH and the CPU1 feeds its information to the PCH via QPI link between processors and the CPU0 DMI2 link.

Memory Interface

Three DDR4-2400MHz memory channels per processor provide a peak data transfer rate of 2400 MT/s per channel when using DDR4 PC4-19200 DIMMs ***and*** the Intel® Xeon® E5-2680 v4 processors.

DMA Channels

The SHB is fully PC compatible and the Intel® C612 PCH used on the SHB provides seven independently programmable DMA channels. Channels 0–3 are hardwired to 8-bit, count-by-byte transfers, and channels 5–7 are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers.

Interrupts

The Intel® C612 PCH incorporates the functionality of two 8259 interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts are: system timer, keyboard controller, serial ports, mouse, and the DMA channels. In addition, this interrupt controller can support the PCI based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line.

BIOS (Flash)

The Aptio® 5.x BIOS from American Megatrends Inc. (AMI) resides in the HDEC board's SPI flash devices. The BIOS features built-in advanced CMOS setup for the SHB's operational parameters plus management menus for configuring peripherals and other system configuration parameters. The BIOS may be upgraded from a USB thumb drive storage device by pressing **<Ctrl> + <Home>** immediately after reset or power-up with the USB device installed in drive A. Contact Trenton Technical Support for more information on the latest BIOS revision for your system board. Custom BIOSs are also available, contact Trenton for more information.

Operating Systems

Trenton's HEP8225 has been tested using a number of popular and readily available operating systems including: Microsoft Windows Server 2008 R2, Windows 7, Windows 8, Windows 2012 Server, Windows 10 Preview and a number of distributions of Linux, including Red Hat. This testing process confirms the SHB's PCI Express interface and device I/O functionality. Trenton does not recommend using the Microsoft Windows XP operating system due to limited functionality concerns. Contact Trenton Tech Support for additional information and specific compatibility information.

Cache Memory

The Intel® Xeon® E5-2600 v3 and v4 series processors offer different cache memory capacities. The table below summarizes the cache memory capacities for selected processors available for use with the HEP8225.

Processor	Cache Memory Capacity
Intel® Xeon® E5-2680 v4 Intel® Xeon® E5-2658 v4 Intel® Xeon® E5-2648L v4	35MB
Intel® Xeon® E5-2628L v4 Intel® Xeon® E5-2680 v3 Intel® Xeon® E5-2658 v3 Intel® Xeon® E5-2648L v3	30MB
Intel® Xeon® E5-2618L v4 Intel® Xeon® E5-2628L v3	25MB
Intel® Xeon® E5-2608L v4 Intel® Xeon® E5-2618L v3 Intel® Xeon® E5-2640 v3	20MB
Intel® Xeon® E5-2608L v3	15MB

DDR4 Memory & SHB Memory Population Rules

Trenton recommends ECC registered DDR4-2133 memory modules for use on the HEP8225. Unbuffered ECC DDR4 DIMMs are also supported, however, you cannot mix the ECC registered and unbuffered ECC memory types on the same board.

Each processor on a HEP8225 supports 4 channels of memory. These DIMM modules must be compatible with the PC4-19200 standard. The maximum possible memory interface speed obtained depends on the specific Intel® Xeon® E5-2600 v3 or v4series processors used on the board and other board configuration options listed in the notes section below.

NOTES:

- To maximize system performance and reliability, Trenton recommends populating each memory channel with DDR4-2400 DIMMs on the HEP8225 dual-processor board.
- All memory modules must have gold contacts.
- Low-voltage (DDR4L) DIMMs are supported, but are costly and supply may be limited. Contact Trenton for more details.

Populate the memory sockets starting with the DIMM socket closest to the CPU and work your way toward the edges of the SHB as illustrated in the chart below:

DIMM Population Order	CPU0	CPU1
1	BK1	BK5
2	BK3	BK7
3	BK0	BK4
4	BK2	BK6

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board.

Universal Serial Bus (USB)

The SHB supports six super-speed USB 3.0 ports. Four of the interfaces are located on the back of the SHB I/O bracket, while two are passed through the edge connector to a header on the backplane. In addition, four USB 2.0 interfaces are passed to the backplane.

Video Interface

The SHB features a Graphics Processing Unit (GPU) onboard the ASPEED AST2400 with 8MB of video memory. The GPU is driven by a x1 PCIe link from the SHB's Intel® 610 PCH. This combination of features enables the SHB's video port; located on the board's I/O plate, to support pixel resolutions up to 1920 x 1200 (WUXGA).

PCI Express Interfaces

Eighty links of PCI Express 3.0 x16 are available from the dual-Haswell-equipped HEP8225 at 40 lanes per processor. PCI Express automatic link negotiation and bifurcation are implemented and previous PCIe link speeds, Gen 1.1 and 2.0, are also supported. PCIe's scalability allows for cards with fewer electrical lanes to function in slots that are mechanically larger, e.g., a x1 card in a x16 slot. The reverse is not possible, as a x16 card will not physically fit into a smaller x1, x4, x8 slot. The PCIe link will automatically negotiate between the processor and the card for the fastest possible link speed.

The HDEC SHB connector utilizes groups of pins, numbered C1 through C5. The center connector, C3, is utilized for power and system functions while the two x16 and one x8 PCIe links from each processor are routed to C1, C2 and C4, C5, respectively. Additionally, the HDEC standard allows for an additional eight lanes of PCIe, expected to be supported by future Intel processor designs. Additional information on the HDEC Series SHB/backplane connection methodology can be found in "An Implementation Guide for High Density Embedded Computing" available at http://www.trentonsystems.com.

A Word about PCI Express 3.0 Interfaces

PCIe 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen3, Gen2 and Gen1.1 I/O cards on the same interface link. Running a PCIe 3.0 target device such as a Gen3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the HEP8225 to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off or not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specific of your particular PCIe 3.0 implementation.

Ethernet Interfaces – 2, 1GbE and 2, 10GbE, Standard Configuration

The HEP8225 supports four Local Area Network Ethernet interfaces. Two are standard 10/100/1000Base-T Gigabit Ethernet ports, one supplied by an Intel I217-LM Ethernet PHY, the other by an ASPEED AST2400 SuperIO chip. The remaining interfaces are 10GbE, provided by an Intel X540-BT2 controller, supplied by 4 dedicated PCI Express lanes. All of the ports are located on the system I/O bracket.

The main components of the I/O bracket Ethernet interfaces are:

- Intel® I217-LM for 10/100/1000-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCIe interface.
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connectors on the SHB's I/O bracket for direct connection to the network. The connectors require category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cables for a 100-Mb/s network connection or category3 (CAT3) or higher UTP 2-pair cables for a 10-Mb/s network connection. Category 5e (CAT5e) or higher UTP 2-pair cables are recommended for a 1000-Mb/s (Gigabit) network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

Software drivers are supplied for most popular operating systems. Contact Trenton for information on alternative Ethernet configurations such as 4, 1GbE.

SATA/600

There are eight Serial ATA (SATA) interfaces available on the HEP8225 board. Two SATA ports are on the SHB. Six SATA/600 interfaces are routed to the edge connector of the SHB for use on a SATA-equipped HDEC® backplane. All of the SATA interfaces are driven with a built-in SATA controller from the Intel® C612 Platform Controller Hub (PCH). The board's SATA ports can support eight independent SATA storage devices such as hard disks and CD/DVD-RW devices at data transfer rates up to 600MB per second on each port. The board's PCH features the Intel® Rapid Storage Systems functionality, which allows a third BIOS-selectable SATA controller configuration that enables either two or four-drive RAID array configurations capable of supporting RAID 0, 1 and 10 implementations.

The SATA controller has three BIOS selectable modes of operation located under the Advanced/SATA Configuration menu with a legacy (i.e. IDE) mode using I/O space, an AHCI mode using memory space and a RAID mode.

Watchdog Timer (WDT)

The HEP8225 provides a programmable Watchdog Timer with 7 programmable timeout periods ranging from 32msec to 32 seconds. When enabled the WDT will generate a system reset. WDT control is supplied via the Intel® C612 Platform Controller Hub (PCH) General Purpose IO pins. The GPIO_LVL2 register controls the states of GPIO signals that select the timeout period. The C612's GPIO_LVL2 register also provides the WDT's enable/disable function. This 32-bit register is located within GPIO IO space. The GPIO_BASE IO address is determined by the values programmed into the C612's LPC Bridge PCI configuration at offset 48-4B(h).

GPIO Bit Definitions:

Watchdog Timer Enable (WDT_EN#)
Watchdog timer enable\disable functionality is controlled by GPIO47. Clearing bit 16 of the GP_LVL2 register enables the WDT. The GP_LVL2 register is located at IO address GPIO_BASE + offset 38(h). The power-on default for this bit is a "1" which disables WDT functionality. Setting this bit to a "0" enables the WDT at the pre-selected interval.

Watchdog Select 0 (WDT_S0)
The state of this bit in conjunction with WatchDog Select 1 will select the WDT time out period. This function is controlled by GPIO36 and the state of this bit is determined by bit 4 of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST the inverted state of this bit is reflected on Port80, LED0. If this bit is set to a "1" the LED is off, if set to a "0" the LED is on. See Table 1 for WDT interval selection.

Watchdog Select 1 (WDT_S1)
The state of this bit in conjunction with WatchDog Select 0 will select the WDT time out period. This function is controlled by GPIO37 and the state of this bit is determined by bit 5 of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST the inverted state of this bit is reflected on Port80, LED1. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on. See Table 1 for WDT interval selection.

WatchDog Select 2 (WDT_S2)
The state of this bit in conjunction with WatchDog Select 2 will select the WDT time out period. This function is controlled by GPIO38 and the state of this bit is determined by bit 6 of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST the inverted state of this bit is reflected on Port80, LED1. If this bit is set to a "1" the LED is off, if set to a "0" the LED is on. See Table 1 for WDT interval selection.

Watchdog_ Input (WDT_IN)
When the WDT is enabled this bit must be toggled (0 -> 1 or 1->0) within the selected watchdog timeout period, failure to do so will result in a system reset. This function is supported by the GPIO54 bit and its state is controlled by bit 22 of the GP_LVL2 register which is at IO address GPIO_BASE + offset 38(h). The inverted state of this bit is reflected on Port80, LED7. If this bit is set to a "1" the LED is off, if set to a "0" the LED is on.

Watchdog Timer (WDT - continued)

Watchdog Timeout Period Selections:

WDT_EN# (GPIO47)	WD_S2 (GPIO38)	WD_S1 (GPIO37)	WD_S0 (GPIO36)	Watchdog Timeout Period
1	X	X	X	Disabled
0	0	0	0	32 msec
0	0	0	1	128 msec
0	0	1	0	512 msec
0	0	1	1	1 sec
0	1	0	0	4 sec
0	1	0	1	8 sec
0	1	1	0	32 sec
0	1	1	1	Disabled

The Watchdog Timer may require initialization prior to usage. GPIOs 47, 36, 37, 38, 54 are required to be configured as outputs. While these GPIOs default to outputs at power-on, care should be taken to insure they have not been altered prior to WDT usage. These GPIOs are configured to outputs by clearing bits 4, 5, 6 and 22 of the GP_IO_SEL2 register at GPIO_BASE + offset 34(h) to a "0".

After initialization is completed (if required) the Watchdog timer period is selected by the WDT_S2, WD_SELS1 and WDT_S0 bits. Once the timeout period has been programmed the WDT is then "enabled" by clearing the WDT_EN# bit. To avoid the WDT from generating a system reset the WDT_IN bit must be toggled within the timeout period.

Programming Example: Enable WDT with 1-second timeout period

Note: *When writing to any of the WDT controlling GPIO bits the remaining bits of the selected GP_LVL2 register should remain unchanged.*

Write bit 16 of GP_LVL2 to 1	pre-condition GPIO47 for WDT disable
Write bits 6, 5, 4 of GP_LVL2 to 0, 1, 1,	set Watchdog timeout period to 1 sec
Write bit 16 of GP_LVL2 to 0	enable Watchdog timer

At this point the bit 22 of GP_LVL2 (GPIO71) must be toggled within the 1 sec. timeout period or the WDT will expire resulting in a system reset.

Power Fail Detection

A hardware reset may be issued when monitored voltages on the SHB drop below a specified nominal low voltage limit. In addition, the HDEC system host board is capable of generating an SMI# on the de-assertion of the Power Good signal from the backplane. This allows a processor to sense an impending power failure with the system power supply being responsible for maintaining the +12V, +5V and 3.3V rails in tolerance for the period of time necessary to service the SMI# interrupt. The monitored voltages and their nominal low limits are listed below.

Monitored Voltage	Power Source	Usage	Nominal Low Limit		Comment
12V	External Power Supply		10.2V	+/- 2%	Fixed
5V	External Power Supply		4.63V	+/-2.5%	Fixed
3.3V	External Power Supply		2.88V	+/- 2.5%	Fixed
1.5V	On-board Regulator	Chipset	1.35V	+/- 4.5%	Fixed
1.05V	On-board Regulator	Processor	0.88V	+/- 3.5%	Fixed
BMC_VCCore	On-board Regulator	BMC	1.47V	+/- 2.5%	Fixed
BMC_DDR	On-board Regulator	BMC	1.19V	+/- 2.5%	Fixed
CPUx_VCCDDR	On-board Regulator	Processor/Memory	1.16V	+/- 3.5%	Fixed
CPUx_VTTDDR	On-board Regulator	Processor/Memory	0.58V	+/-3.5%	Fixed
CPU_VCCIO	On-board Regulator	Processor	(VCCIO *0.88)	+/-3.5%	VCCIO: 1.05V Haswell/0.95V Broadwell.
CPUx_VCCORE	On-board Regulator	Processor	1.6V-1.82V		Value dynamically determined by processor, dependent on system load and configuration

Battery

A built-in lithium battery is provided for ten years of data retention for CMOS memory.

CAUTION: There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Power Requirements HEP8225

Power Requirements				
Typical Values --Static Desktop (Idle) with 64GB of system memory				
CPU	**Intel® No.**	**5v**	**12v**	**3v**
2.4GHz	E5-2680 v4	4.69A	5.84A	2.43A
2.5GHz	E5-2680 v3	4.30A	5.62A	2.28A
2.3Ghz	E5-2658 v4	3.73A	4.63A	2.59A
2.2Ghz	E5-2658 v3	4.35A	5.41A	2.28A
1.8Ghz	E5-2648L v4	3.55A	4.58A	2.42A
1.8Ghz	E5-2648L v3	4.24A	5.24A	2.29A
1.9Ghz	E5-2628L v4	4.65A	3.14A	2.45A
2.0Ghz	E5-2628L v3	4.23A	5.18A	2.30A
2.2GHz	E5-2618L v4	3.43A	3.19A	2.20A
2.3GHz	E5-2618L v3	4.36A	4.56A	3.06A
2.0GHz	E5-2608L v3	3.80A	3.52A	2.61A
Typical Values --100% Stress State with 64GB of system memory				
CPU	**Intel® No.**	**5v**	**12v**	**3v**
2.4GHz	E5-2680 v4	5.20A	27.56A	2.92A
2.5GHz	E5-2680 v3	5.28A	27.67A	2.79A
2.3Ghz	E5-2658 v4	4.14A	24.32A	2.68A
2.2Ghz	E5-2658 v3	5.08A	24.81A	2.77A
1.8Ghz	E5-2648L v4	4.01A	17.95A	2.59A
1.8Ghz	E5-2648L v3	4.88A	18.20A	2.59A
1.9Ghz	E5-2628L v4	5.07A	17.32A	2.93A
2.0Ghz	E5-2628L v3	4.73A	18.16A	2.60A
2.2GHz	E5-2618L v4	4.06A	17.39A	2.78A
2.3GHz	E5-2618L v3	4.79A	14.10A	3.21A
2.0GHz	E5-2608L v3	4.10A	12.51A	2.93A

CAUTION: Trenton recommends an EPS type of power supply for systems using high-performance processors. The power needs of backplane option cards, high-performance processors and other system components may result in drawing 20A of current from the +12V power supply line. If this occurs, hazardous energy (240VA) could exist inside the system chassis. Final system/equipment suppliers must provide protection to service personnel from these potentially hazardous energy levels.

Stand-by voltages may be used in the final system design to enable certain system recovery operations. In this case, the power supply may not completely remove power to the system host board when the power switch is turned off. Caution must be taken to ensure that incoming system power is completely disconnected before removing the system host board.

Temperature/Environment

Operating Temperature: 0-50° C. with the standard cooling solution and 350LFM of continuous airflow
0-45° C. when using two Intel® Xeon® E5-2680 v4 or v3 processors in a HEP8225 SHB configuration with the standard cooling solution and 350LFM of continuous airflow. Processors with TDP ratings of 120W will have a maximum HEP8225 board operating temperature of 45° C.

Air Flow Requirement: 350LFM continuous airflow

Storage Temperature: - 40º C. to 70º C.

Humidity 5% to 90% non-condensing

Mechanical

The SHB's overall dimensions are 13.345" (33.858cm) L x 5.750" (14.605cm) H. The standard cooling solution used on the HEP8225 SHBs enables placement of option cards approximately 2.975" (75.57mm) away from the top component side of the SHB. Some system integration applications using chassis such as 2U rackmount computers require lower profile cooling solutions. A low profile heat sink option is available for the HEP8225 board that allows option card placements of 1.550" (39.37mm) from the topside of the board. A low profile cooling solution usually results in a 25-30% reduction in a system's maximum operating temperature rating. Contact Trenton Systems for more information on cooling solution options for the HEP8225 system host board.

Jumpers & LEDs

The setup of the configuration jumpers on the SHB is described below. An asterisk (*) indicates the default value of each jumper.

NOTE: Jumper JU1 is a dual-row, 14-pin jumper. Each position controls the operation of a specific SHB implementation.

JU1	**CMOS Clear**
Pins	Install on pins 1 and 2 to operate.*
1 – 2	Install on pins 3 and 4 to clear.
and	
3 – 4	**NOTE:** To clear the CMOS, power down the system and install the JU1 jumper on pins 3 and 4. Wait for at least two seconds, move the jumper back to pins 1 and 2 and turn the power on. Clearing CMOS on the HEP8225 will not result in a checksum error on the following boot. If you want to change a BIOS setting, you must press DEL or the F2 key during POST to enter BIOS setup after clearing CMOS.

JU1	**Management Engine (ME) Recovery**
Pins	No jumper installed on pins 5 and 6 is the normal SHB operating mode.*
5 – 6	Install jumper on pins 5 and 6 for one power-up cycle to force a management engine update

JU1	**Clear Password**
Pins	No jumper installed on pins 7 and 8 is the normal SHB operating mode.*
7 – 8	Install jumper on pins 7 and 8 for one power-up cycle to reset the password to the default (null password).

JU1	**BIOS Recovery**
Pins	No jumper installed on pins 9 and 10 is the normal SHB operating mode.*
9 – 10	Install jumper on pins 9 and 10 to force a Top Block Swap (Alternate Boot Block).

JU1	**Flash Descriptor Security**
Pins	No jumper installed on pins 11 and 12 enables the Flash Descriptor Security.*
11 – 12	Install jumper on pins 11 and 12 to disable Flash Descriptor Security.

JU1	**SPI Voltage Enable (Factory Use Only)**
Pins	No jumper installed on pins 13 and 14 is the normal SHB operating mode.*
13 – 14	Installing a jumper on pins 13 and 14 to allows SPI factory programming via a clip on programmer.

CAUTION: Installing this jumper is required for certain factory operations. Field installation of a jumper in JU1 pin locations 13 and 14 may result in unintended system operation.

Jumpers & LEDs (continued)

P6 **1Gb Ethernet LEDs**

The I/O bracket houses the two RJ-45 network connectors for Ethernet LAN3 and LAN4. Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

LED/Connector	Description
Activity LED	Green LED indicates network activity. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets).
Off	No current network transmit or receive activity
On (solid)	Indicates a valid link established, but no network activity.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	Green/Yellow bi-color LED identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors).
Off	Indicates a valid link at 10-Mb/s.
On (green)	Indicates a valid link at 100-Mb/s.
On (yellow)	Indicates a valid link at 1000-Mb/s or 1-Gb/s.
RJ-45 Network Connectors	The RJ-45 network connector requires a Connectors category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection.

P7 **10Gb or 1Gb Ethernet LEDs**

The I/O bracket also contains two upper RJ-45 network connectors that indicate either a maximum Ethernet connection speed of 10Gb or 1Gb on LAN1 and LAN2. With the HEP8225 configured with an Intel® Ethernet Controller X540 Ethernet controller the P7 ports are capable of 10GbE operations. An alternate HEP8225 configuration is available that enables a maximum LAN speed of 1GbE on the P7 LAN connectors when the HEP8225 SHB is configured with an Intel® Ethernet Controller I350-AM2.

Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

Activity LED	**Yellow LED indicates network activity. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets).**
Off	No current network transmit or receive activity
On (solid)	Indicates a valid link established, but no network activity.
On (flashing)	Indicates network transmit or receive activity.

Speed LED – 10GbE Port Configuration	**Green/Orange bi-color LED identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors).**
Off	Indicates a valid link at 100-Mb/s.
On (orange)	Indicates a valid link at 1000-Mb/s or 1-Gb/s.
On (green)	Indicates a valid link at 10000-Mb/s or 10-Gb/s.

Speed LED – 1GbE Port Configuration	**Green/Orange bi-color LED identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors).**
Off	Indicates a valid link at 10-Mb/s.
On (green)	Indicates a valid link at 100-Mb/s.
On (orange)	Indicates a valid link at 1000-Mb/s or 1-Gb/s.

RJ-45 Network Connectors	The RJ-45 network connector requires a Connectors category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection.

LED8

LED/Connector	**Description**
OFF	Indicates the normal board operation.

At the present time an LED8 ON condition indicates one of the following error conditions:

Two (2) Blinks/sec	=	CATERR issue
One (1) Blink/sec	=	Machine Check issue
ON Solid	=	CPU Thermal Trip
One (1) Blink/Two (2) sec	=	DDR Memory Thermal Event

Additional LED conditions may be available to narrow down the specific fault condition. Contact Trenton for additional details.

LED9

LED/Connector	**Description**
Off	Indicates normal board operation.
On (Solid)	LED ON condition indicates an issue with the CPU or DDR memory voltage regulators. Additional LED conditions may be available to narrow down the specific fault condition. Contact Trenton for additional details.

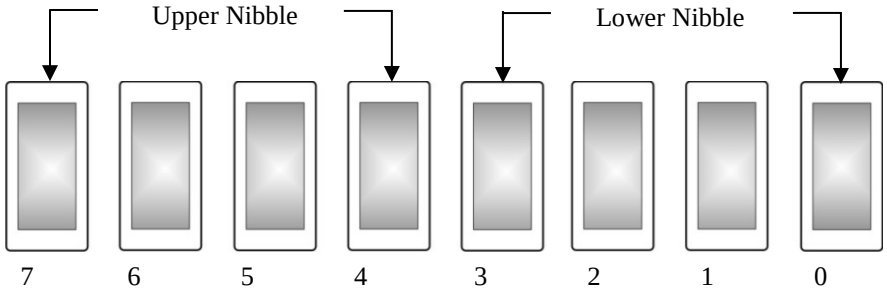
POST Code LEDs 0 - 7

As the POST (Power On Self-Test) routines are performed during boot-up, test codes are displayed on Port 80 POST Code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7). Refer to the board layout diagram for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. Specific test codes are listed in Appendix A - BIOS Messages section of the HEP8225 Technical Reference Manual. After a normal POST sequence, the LEDs are off (00h) indicating that the SHB's BIOS has passed control over to the operating system loader typically at interrupt INT19h. The chart is from Appendix A and can be used to interpret the LEDs into hexadecimal format during POST.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



HEP8225 POST Code LEDs

System BIOS Setup Utility

The HEP8225 features the Aptio® 5.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. The TSE setup utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- Intel RCSetup
- Security
- Boot

Each of these options allows you to review and/or change various setup features of your system. Details of the Aptio TSE are provided in the separate *HEP8225 BIOS Technical Reference* manual. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the HEP8225 page.

Connectors

NOTE:
A connectors' square solder pad located on the bottom side of the PCB indicates pin 1.

P6 – Dual 10/100/1000Base-T Ethernet Connector – LAN3 and LAN4

RJ-45/Dual connector, Pulse #JG0-101NL
Each individual RJ-45 connector is defined as:

PIN	SIGNAL	PIN	SIGNAL
1A	L3_MDI0n	1B	L4_MDI0n
2A	L3_MDI0p	2B	L4_MDI0p
3A	L3_MDI1n	3B	L4_MDI1n
4A	L3_MDI1p	4B	L4_MDI1p
5A	L3_MDI2n	5B	L4_MDI2n
6A	L3_MDI2p	6B	L4_MDI2p
7A	L3_MDI3n	7B	L4_MDI3n
8A	L3_MDI3p	8B	L4_MDI3p
9A	VCC_1.8V	9B	VCC_1.8V
10A	GND_A	10B	GND_b

P1A – Right Angle Stacked Connector - Video

DB15 HD video, Kycon # K42X-E9P/E15S-A4N

PIN	SIGNAL	PIN	SIGNAL
1	Red	9	+5V
2	Green	10	Gnd
3	Blue	11	NC
4	NC	12	EEDI
5	Gnd	13	HSYNC
6	Gnd	14	VSYNC
7	Gnd	15	EECS
8	Gnd		

P1B – Right Angle Stacked Connector - Serial

DB9 serial, Kycon # K42X-E9P/E15S-A4N

PIN	SIGNAL	PIN	SIGNAL
1	Data Carrier Detect	6	Data Set Ready
2	Receive Data	7	Request To Send
3	Transmit Data	8	Clear To Send
4	Data Terminal Ready	9	Ring Indicator
5	Signal Grid		

DB15 video connector is to the left and has female sockets
DB9 serial connector is to the right and has male pins

P9 – Quad USB 3.0 Stacked Connector, Type A

Four USB connectors, Foxconn #UEA1112C-QHD6-4F

PIN	P9A USB0 SIGNAL	PIN	P9B USB1 SIGNAL
A1	+5V-USB0	B1	+5V-USB1
A2	USB P0-	B2	USB P1-
A3	USB P0+	B3	USB P1+
A4	Gnd-USB0	B4	Gnd-USB1
A5	USB RXN0	B5	USB RXN1
A6	USB RXP0	B6	USB RXP1
A7	Gnd-USB0	B7	Gnd-USB1
A8	USB TXN0	B8	USB TXN1
A9	USB TXP0	B9	USB TXP1

PIN	P9C USB2 SIGNAL	PIN	P9D USB3 SIGNAL
C1	+5V-USB2	D1	+5V-USB3
C2	USB P2-	D2	USB P3-
C3	USB P2+	D3	USBP3+
C4	Gnd-USB2	D4	Gnd-USB3
C5	USB RXN2	D5	USB RXN3
C6	USB RXP2	D6	USB RXP3
C7	Gnd-USB2	D7	Gnd-USB3
C8	USB TXN2	D8	USB TXN3
C9	USB TXP2	D9	USB TXP3

Note:
1 – P9A is USB0 and located on the left side of the I/O plate directly above the VGA video port. P9B is USB1, P9C is USB2 and P9D is USB3 located on the right side of the I/O bracket farthest from the board and above the serial port.

P10, P11 – SATA III 600 / SATA II 300 Ports

7 pin vertical connector with latch, Molex #67800-8005

PIN	SIGNAL	PIN	SIGNAL
1	Gnd	5	RX-
2	TX+	6	RX+
3	TX-	7	Gnd
4	Gnd		

Notes:
1 – P10 = SATA0 interface, P11 = SATA1 interface

Connectors (continued)

P5 and P12 – CPU Fan Power Connectors

4 pin single row header, Molex # 47053-1000

PIN	SIGNAL
1	Gnd
2	+12V
3	Fan Tach
4	PWM Control Signal

Note:
1 – P5 is the fan connector for CPU0 and P11 is for CPU1

P8 - Audio Port*

3 position audio, Foxconn #JA13331-N20B-4F

SOCKET COLOR	SIGNAL
Light Blue	Line In
Lime	Line Out
Pink	Mic

*Audio port P8 is not populated for board versions that are integrated into 2U rackmount computer chassis

P7 – Dual 10GbBase-T Ethernet Connector – LAN1 and LAN2 - (Optional)

RJ-45/Dual 10GbE connector, MagJack #JG0-101NL
Each individual RJ-45 connector is defined as follows:

Upper/Right PIN	SIGNAL	Lower/Left PIN	SIGNAL
1	L1_MDI_DP0	1	L2_MDI_DP0
2	L1_MDI_DN0	2	L2_MDI_DN0
3	2.5V_X540	3	2.5V_X540
4	L1_MDI_DP1	4	L2_MDI_DP1
5	L1_MDI_DN1	5	L2_MDI_DN1
6	2.5V_X540	6	2.5V_X540
7	L1_MDI_DP2	7	L2_MDI_DP2
8	L1_MDI_DN2	8	L2_MDI_DN2
9	2.5V_X540	9	2.5V_X540
10	L1_MDI_DP3	10	L2_MDI_DP3
11	L1_MDI_DN3	11	L2_MDI_DN3
12	2.5V_X540	12	2.5V_X540
13	L1_MDI_DP4	13	L2_MDI_DP4
14	L1_MDI_DP4	14	L2_MDI_DP4

Note1: The 10GbE LAN ports are the upper two connectors on the board's I/O bracket.
Note2: Some configurations of the HEP8225 system host board may not include the P7, dual LAN 10GbE connector.

This page intentionally left blank

Chapter 2 PCI Express® Reference

Introduction

PCI Express® is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the system host board (SHB) and PCI Express option cards.

PCI Express option cards may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification. Because of this design, PCI, PCI-X and PCI Express option cards can co-exist in the same system.

PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector.

PCI Express Links

Several PCI Express channels (lanes) can be bundled for each expansion slot, leaving room for stages of expansion. A link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. A x1 slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth, counting bandwidth in both directions, is 500MB/s (full-duplex).

The number and configuration of an SHB's PCI Express links is determined by specific component PCI Express specifications. In PCI Express Gen1 the bandwidths for the PCIe links are determined by the link width multiplied by 250MB/s and 500MB/s, as follows:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	250MB/s	500MB/s
x4	1GB/s	2GB/s
x8	2GB/s	4GB/s
x16	4GB/s	8GB/s

In PCI Express Gen2 the bandwidths for the PCIe links are doubled as compared to PCIe Gen1.1 as shown below:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	500MB/s	1GB/s
x4	2GB/s	4GB/s
x8	4GB/s	8GB/s
x16	8GB/s	16GB/s

PCI Express Links (continued)

PCI Express 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen3, Gen2 and Gen1.1 I/O cards on the same interface link. In PCI Express Gen3 the bandwidths for the PCIe links are doubled as compared to PCIe Gen2 as shown below:

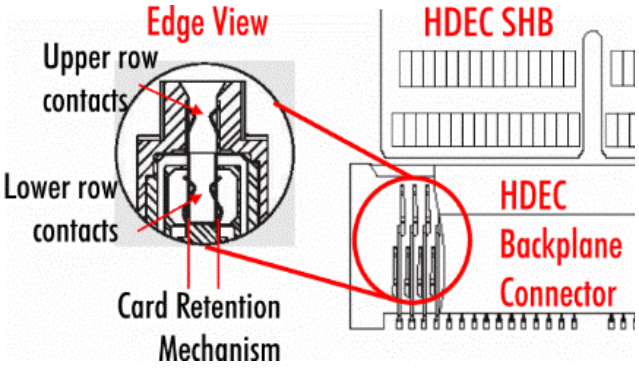
Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	1GB/s	2GB/s
x4	4GB/s	8GB/s
x8	8GB/s	16GB/s
x16	16GB/s	32GB/s

Running a PCIe 3.0 target device such as a Gen3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the HEP8225) to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off and not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specific of your particular PCIe 3.0 implementation.

Scalability is a core feature of PCI Express. Some chipsets allow a PCI Express link to be subdivided into additional links, e.g., a x8 link may be able to be divided into two x4 links. In addition, although a board with a higher number of lanes will not function in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) because the connectors are mechanically and electrically incompatible, the reverse configuration will function. A board with a lower number of lanes can be placed into a slot with a higher number of lanes (e.g., a x4 board into a x16 slot). The link auto-negotiates between the PCI Express devices to establish communication.

High Density Embedded Computing (HDEC) System Host Board Connection

The HDEC® Series of backplanes and system host boards were designed with the goal of bringing the very latest in high-throughput innovations provided by server-class Intel® processors to bear on mission-critical industries. In addition, the individual components were designed to fit most current industry-standard form factors for servers, workstations and rugged-environment computing without sacrificing reliability, longevity or performance, all while providing unrivaled flexibility in systems integration.



The above diagram illustrates the double-density PCIe card edge fingers and double-density SHB slot connectors utilized in a typical HDEC Series backplane. The HEP8225's backplane connector system consists of five interfaces, notated C1 through C5, form the backbone of the HDEC® system, allowing one system host board per backplane SHB slot to communicate with a single backplane with far greater datathroughput than previous standards. Other benefits of the HDEC® standard include eighty lanes of full

PCIe 3.0 support, six SATA/SAS 600 ports, six USB 2.0 ports, RS232 interface, and PS/2 mouse and keyboard support. In kind, the backplane provides full power and internal I/O support to the System Host Board(s) through the HDEC® connector, reducing Mean Time to Repair (MTTR), easing cable routing, and ensuring optimal thermal efficiency.
Connector C1 contains PCI-Express I/O and a Present pin, Connector C2 contains PCI-Express I/O, Connector C3 contains PCI-Express I/O, Present pins and the PCI-Express reference clocks. Connectors C4 and C5 contain the additional input and output functions. C4 handles power, Ethernet, SMBus, and System Fan control while C5 handles USB, SATA, Serial, Audio, LED, GPIO, fan, miscellaneous control signals and a present pin.

The HDEC® connector consists of four Samtec BEC5 200 connectors for data transmission and 1 Samtec BEC5 160 connector for power connections.

Additional features of the HDEC® SHB interface standard include:
- Intruder Alert function from backplane
- System Host Board detection
- Speaker out to backplane
- Audio Out to backplane
- Line In from backplane
- Microphone In from backplane
- RS232 to/from backplane
- CMOS clear input from backplane
- Eight (8) fan PWM output to backplane
- Eight (8) fan Tach input from backplane
- Three (3) fan PWM input to SHB
- Three (3) fan tach output from SHB
- Eight (8) GPIO Pins to/from backplane
- Ten (10) additional LED output to backplane
- Optional configuration data EEPROM on backplane

This page intentionally left blank

Chapter 3 HEP8225 System Power Connections

Introduction

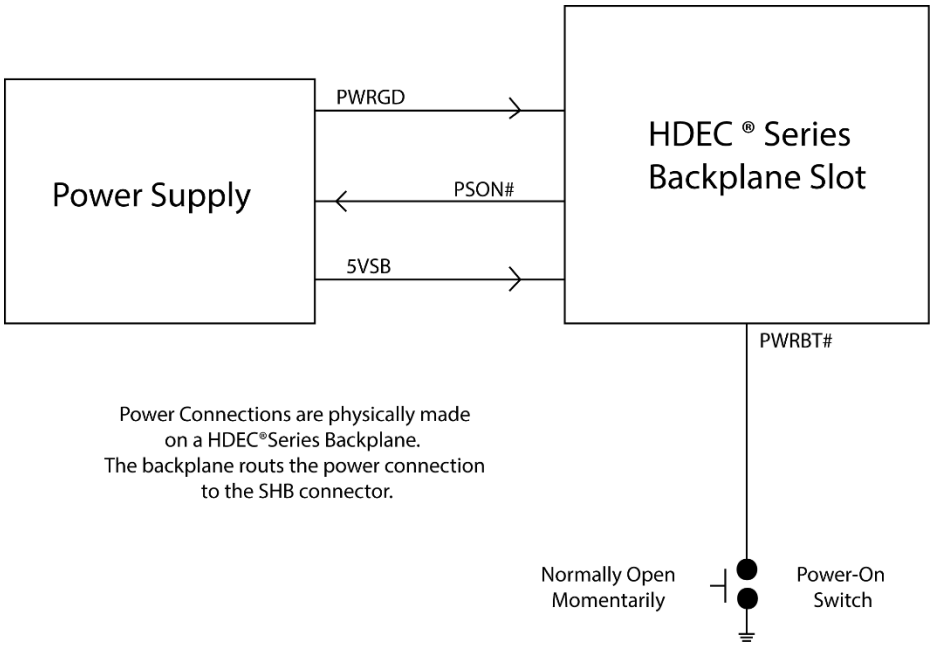
To improve system MTTR (Mean Time to Repair), the HDEC® specification defines enough power connections to the SHB's edge connectors to eliminate the need to connect auxiliary power to the SHB. All power connections are made on the backplane. The connectors on a backplane must have an adequate number of contacts that are sufficiently rated to safely deliver the necessary power to drive these high-performance SHBs. Trenton's HDEC® EPS and +12V connectors that are compatible with ATX/EPS power supply cable harnesses and provide multiple pins capable of delivering the current necessary to power high-performance processors.

The HDEC® specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). Trenton SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. Refer to the General ACPI Configuration section of the *Advanced Setup* chapter in this manual for information on ACPI BIOS settings.

When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

Power Supply and SHB Interaction

The following diagram illustrates the interaction between the power supply and the processor. The signals shown are PWRGD (Power Good), PSON# (Power Supply On), 5VSB (5 Volt Standby) and PWRBT# (Power Button). The +/- 12V, +/-5V, +3.3V and Ground signals are not shown.



PWRGD, PSON# and 5VSB are usually connected directly from an ATX or EPS power supply to the backplane. The PWRBT# is a normally open momentary switch that can be wired directly to a power button on the chassis.

CAUTION: In some EPS systems, the power may appear to be off while the 5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton HDEC® backplane monitors the 5VSB power signal; "green" indicates that the 5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

ACPI Connection

The diagram on the previous page shows how to connect an ACPI compliant power supply to the HEP8225. The following table shows the required connections that must be made for soft power control to work.

Signal	Description	Source
+12	DC voltage for those systems that require it	Power Supply
+5V	DC voltage for those systems that require it	Power Supply
+3.3V	DC voltage for those systems that require it	Power Supply
+5VSB	5 Volt Standby. This DC voltage is always on when an ATX or EPS type power supply has AC voltage connected. 5VSB is used to keep the necessary circuitry functioning for software power control and wake up.	Power Supply
PWRGD	Power Good. This signal indicates that the power supply's voltages are stable and within tolerance.	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply.	SHB/Backplane
PWRBT#	Power Button. A momentary normally open switch is connected to this signal. When pressed and released, this signals the SHB to turn on a power supply that is in an off state. If the system is on, holding this button for four seconds will cause the SHB's chipset to shut down the power supply. The operating system is not involved and therefore this is not considered a clean shutdown. Data can be lost if this situation occurs.	Power Button

This page intentionally left blank

Chapter 4 HDEC Series Backplane Usage

Introduction

Trenton HDEC® Series systems represent a fundamental shift in how high-density embedded computing is implemented. Providing a full 80 lanes of PCI Express® 3.0, when equipped with a dual-processor system host board, and HDEC® presents great opportunity in TCO and SWaP optimization to several sectors including, Military, Big Data, Graphical Computing and Oil/Gas exploration.

Models

NOTE: In the chart below, the descriptions of the PCI Express slots include the electrical link rate of the slots, not the mechanical size, which is always a full-size, x16 slot.

Released HDEC® Backplanes	**HDB8237**	**HDB8228**	**HDB8236**	**HDB8227**
Format	Full-size/Quad-Segment	Midsize	Small/"Shoebox"	Small/ "Butterfly"
Number of PCIe 3.0 Card Slots	4@x16, 1 per segment	4@x16, 4@x4	4@x16, 1@x8	4@x16
Number of USB 2.0	2 per segment	6	2	2
Number of SATA/600	4 per segment	6	4	5
Target System Chassis	4-in-1 5U Rackmount	4U Rackmount	Custom & 2-in-1 5U Rackmount	2U Rackmount
HDEC® Backplanes Under Development	**HDB8229/HDB8259**	**HDB8230**	**HDB8231**	**HDB8238**
Format	Large/Single-Segment	Midsize	Large/Single-Segment	Midsize
Number of PCIe 3.0 Card Slots	4@x16, 10@x8	5@x16, 1@x8, 2@x4	2@x8, 16@x4	10@x8
Number of USB 2.0	6	6	6	6
Number of SATA/600	6	6	6	6
Target System Chassis	4 or 5U Rackmount	4U Rackmount	4 or 5U Rackmount	4U Rackmount

Features

•More PCI Express links (5x aggregate bandwidth increase)
•Faster network interfaces
•Lower data latencies
•More device and I/O support
•Expanded PCIe Plug-in card support
•Increased adaptability
•COTS option card economies of scale
•Multiple systems (with segmented and shoebox backplanes)
•Fast MTTR (mean time to repair

Note: The HDB8259 is functionally equivalent to the HDB8229 backplane in terms of the form factor and card slot arrangement. The difference is that the HDB8259 supports I^2C bus isolation on each option card slot. I^2C bus isolation is a must have in certain GPU applications using the Tesla K20, K40, or K80 GPU Accelerator cards from NVIDIA.

This page intentionally left blank

Appendix A BIOS Messages

Introduction

A status code is a data value used to indicate progress during the boot phase. These codes are outputted to I/O port 80h on the SHB. Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Status codes are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

[1] Analogous to "bootblock" functionality of legacy BIOS
[2] Analogous to "POST" functionality in legacy BIOS

BIOS Beep Codes

The Pre-EFI Initialization (PEI) and Driver Execution Environment (DXE) phases of the Aptio BIOS use audible beeps to indicate error codes. The number of beeps indicates specific error conditions.

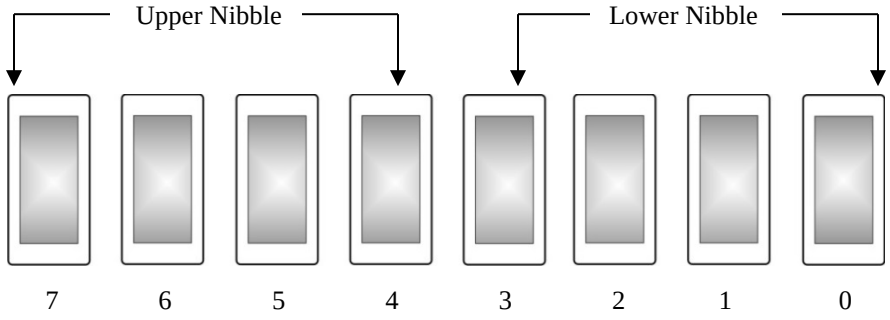
BIOS Status POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, in between the upper DIMM slots. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the HEP8225. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



HEP8225 POST Code LEDs

Upper and Lower POST Code Displays

In addition to the seven LEDs onboard the HEP8225, certain HDEC backplanes have provisions for two (2) seven-segment LED displays. These displays can be used for faster POST code interpretation and real-time monitoring of the POST process. This system consists of two displays, designated LEDs 9 and 10, which will output the hex values of the lower and upper nibbles, respectively. The POST codes displayed are interpreted in the same manner as the hex values displayed by the seven-LED display system.

Status Codes

Status Code Range	Description
0x01 - 0x0B	SEC execution
0x0C - 0x0F	SEC errors
0x10 - 0x2F	PEI execution up to and including memory detection
0x30 - 0x4F	PEI execution after memory detection
0x50 - 0x5F	PEI errors
0x60 - 0x8F	DXE execution up to BDS
0x90 - 0xCF	BDS execution
0xD0 - 0xDF	DXE errors
0xE0 - 0xE8	S3 Resume (PEI)
0xE9 - 0xEF	S3 Resume Errors (PEI)
0xF0 - 0xF8	Recovery (PEI)
0xF9 - 0XFF	Recovery Errors (PEI)

Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not Used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading.
0x03	North Bridge initialization before microcode loading.
0x04	South Bridge initialization before microcode loading.
0x05	OEM initialization before microcode loading.
0x06	Microcode loading.
0x07	AP initialization after microcode loading.
0x08	North Bridge initialization after microcode loading.
0x09	South Bridge initialization after microcode loading.
0x0A	OEM initialization after microcode loading.
0x0B	Cache initialization.
SEC Error Codes	
0x0C - 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found.
0x0F	Microcode not loaded.

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started.
0x11	Pre-memory CPU initialization is started.
0x12	Pre-memory CPU initialization (CPU module specific).
0x13	Pre-memory CPU initialization (CPU module specific).
0x14	Pre-memory CPU initialization (CPU module specific).
0x15	Pre-memory North Bridge initialization is started.
0x16	Pre-memory North Bridge initialization (North Bridge module specific.)
0x17	Pre-memory North Bridge initialization (North Bridge module specific.)
0x18	Pre-memory North Bridge initialization (North Bridge module specific.)
0x19	Pre-memory South Bridge initialization is started.
0x1A	Pre-memory South Bridge initialization (South Bridge module specific.)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific.)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific.)
0x1D - 0x2A	OEM pre-memory initialization codes.
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading.
0x2C	Memory initialization. Memory presence detection.
0x2D	Memory initialization. Programming memory timing information.
0x2E	Memory initialization. Configuring memory.
0x2F	Memory initialization. (other)
0x30	Reserved for ASL (see ASL status Codes section below)
0x31	Memory installed.
0x32	CPU post-memory initialization is started.
0x33	CPU post-memory initialization. Cache initialization.
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization.
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection.
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization.
0x37	Post-Memory North Bridge initialization is started.
0x38	Post-Memory North Bridge initialization (North Bridge Module Specific).
0x39	Post-Memory North Bridge initialization (North Bridge Module Specific).
0x3A	Post-Memory North Bridge initialization (North Bridge Module Specific).
0x3B	Post-Memory South Bridge initialization is started.
0x3C	Post-Memory South Bridge initialization (South Bridge Module Specific).
0x3D	Post-Memory South Bridge initialization (South Bridge Module Specific).
0x3E	Post-Memory South Bridge initialization (South Bridge Module Specific).
0x3F - 0x4E	OEM post memory initialization codes.
0x4F	DXE IPL is started.

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed.
0x51	Memory initialization error. SPD reading has failed.
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected.
0x54	Unspecified memory initialization error.
0x55	Memory not installed.
0x56	Invalid CPU type or speed.
0x57	CPU mismatch.
0x58	CPU self-test failed or possible CPU cache error.
0x59	CPU micro-code is not found or micro-code update is failed.
0x5A	Internal CPU error.
0x5B	Reset PPI is not available
0x5C - 0x5F	Reserved for Future AMI error codes.
S3 Resume Progress Codes	
0xE0	S3 Resume is started (S3 Resume PPI is called by the DXE IPL)>
0xE1	S3 Boot Script execution.
0xE2	Video repost.
0xE3	OS S3 wake vector call
0xE4 - 0xE7	Reserved for Future AMI error codes.
S3 Resume Error Codes	
0xE8	S3 Resume failed.
0xE9	S3 Resume PPI not found.
0x3A	S3 Resume Boot script error.
0xEB	S3 OS wake error.
0xEC - 0xEF	Reserved for Future AMI error codes.
Recovery Progress Codes	
0xF0	Recovery condition trigged by firmware (Auto recovery).
0xF1	Recovery condition triggered by user (Forced recovery).
0xF2	Recovery process started.
0xF3	Recovery firmware image is found.
0xF4	Recovery firmware image is loaded.
0xF5 - 0xF7	Reserved for Future AMI progress codes.
Recovery Error Codes	
0xF8	Recovery PPI is not available.
0xF9	Recovery capsule is not found.
0xFA	Invalid recovery capsule.
0xFB - 0xFF	Reserved for Future AMI error codes.

PEI Beep Codes

# of Beeps	Description
1	Memory not installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice).
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume Failed
7	Reset PPI is not available

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started.
0x64	CPU DXE initialization is started. (CPU module specific).
0x65	CPU DXE initialization is started. (CPU module specific).
0x66	CPU DXE initialization is started. (CPU module specific).
0x67	CPU DXE initialization is started. (CPU module specific).
0x68	PCI host bridge initialization.
0x69	North Bridge DXE initialization is started.
0x6A	North Bridge DXE SMM initialization is started.
0x6B	North Bridge DXE initialization (North Bridge module specific.)
0x6C	North Bridge DXE initialization (North Bridge module specific.)
0x6D	North Bridge DXE initialization (North Bridge module specific.)
0x6E	North Bridge DXE initialization (North Bridge module specific.)
0x6F	North Bridge DXE initialization (North Bridge module specific.)
0x70	South Bridge DXE initialization is started.
0x71	South Bridge DXE SMM initialization is started.
0x72	South Bridge devices initialization.
0x73	South Bridge DXE initialization (South Bridge module specific.)
0x74	South Bridge DXE initialization (South Bridge module specific.)
0x75	South Bridge DXE initialization (South Bridge module specific.)
0x76	South Bridge DXE initialization (South Bridge module specific.)
0x77	South Bridge DXE initialization (South Bridge module specific.)
0x78	ACPI module initialization.
0x79	CSM initialization.
0x7A - 0x7F	Reserved for future AMI DXE codes
0x80 - 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started.

0x91	Driver connecting is started.
0x92	PCI Bus initialization is started.
0x93	PCI Bus Hot Plug Controller Initialization.
0x94	PCI Bus Enumeration.
0x95	PCI Bus Request Resources.
0x96	PCI Bus Assign Resources.
0x97	Console Output devices connect.
0x98	Console input devices connect.
0x99	Super IO initialization.
0x9A	USB initialization is started.
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E - 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready to Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP begin
0xB1	Runtime Set Virtual Address MAP end
0xB2	Legacy Option Rom Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM setting)
0xB8 - 0xBF	Reserved for future AMI codes
0xC0 - 0xCF	OEM BDS initialization codes

DXE Error Codes

0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources.
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset Protocol is not available

DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D - 0x2A	OEM pre-memory initialization codes
0x3F - 0x4E	OEM PEI post memory initialization codes
0x80 - 0x8F	OEM DXE initialization codes
0xC0 - 0xCF	OEM BDS initialization codes