Technical Description

D770

D770 remote is a universal remote, which is mainly focus on SAT top box. It can send IR signal or RF signal. The condition to send RF signal is under SAT mode. At the rest modes, it will only send IR signal.

This remote contains a small RF transmitter, which includes a crystal resonator Y101, oscillator Q101, amplitude shift keying of the carrier Q102, and loop antenna L101. The modulating signal is generated within the microprocessor.

Q5 only drives CR3 diode to send IR signals.

The U1, MCU works at SLEEP status when no keys are pressed. MCU will wake up and send IR or RF signal when any keys are pressed.

Development Features

Table 1 lists the features of ZiLOG®'s Crimzon™ ZLP32300 family members.

Table 1. Features

Device	OTP (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Crimzon™ ZLP32300	4, 8, 16, 32	237	32, 24 or 16	2.0V–3.6V
Note: *General purpose				

- Low power consumption–6mW (typical)
- Three standby modes:
  - STOP—2μA (typical)
  - HALT—0.8mA (typical)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors
  - Port 1: 0–3 pull-up transistors
  - Port 1: 4–7 pull-up transistors
  - Port 2: 0–7 pull-up transistors
  - EPROM Protection

– WDT enabled at POR

Note: The mask option pull-up transistor has a *typical* equivalent resistance of 200 KΩ ±50% at V_{CC}=3 V and 450 KΩ ±50% at V_{CC}=2 V.

General Description

The Crimzon™ ZLP32300 is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Crimzon™ ZLP32300 architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Crimzon™ ZLP32300 offers a new intelligent counter/timer architecture with 8-bit and
16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: All signals with an overline, "$\overline{\ }$", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

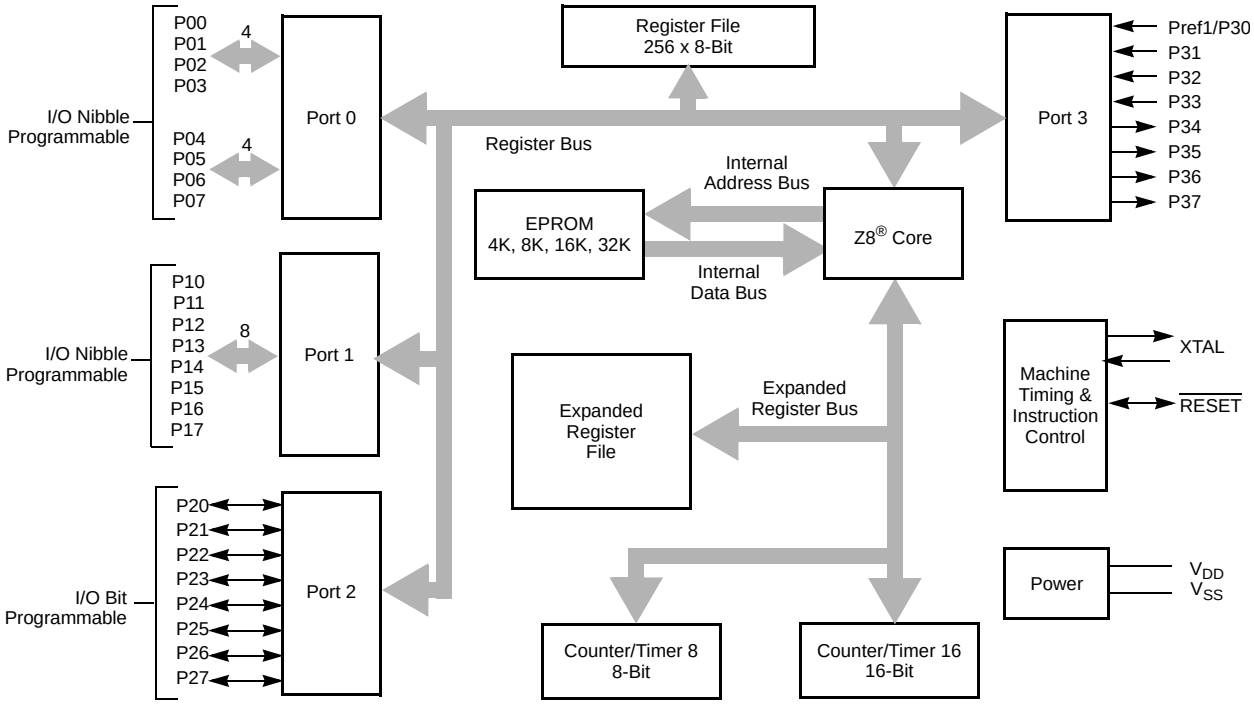

Figure 1. Functional Block Diagram

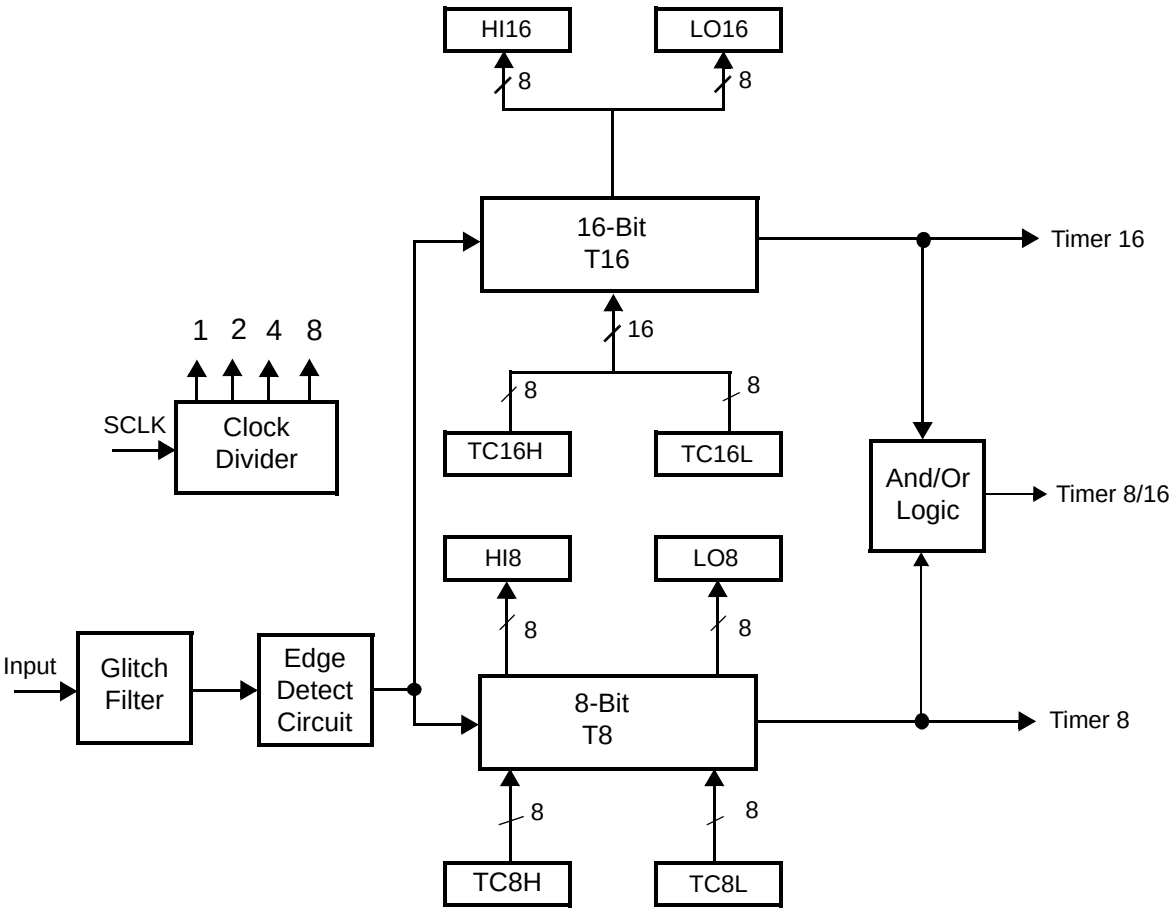

Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOC versions are illustrated in Figure 5, Figure 6, and described in Table 5.